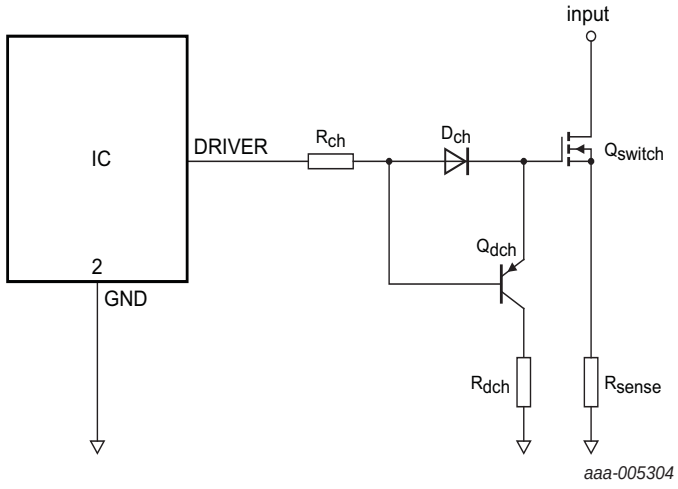
7. PCB layout considerations

A good layout is an important part of the final design. It minimizes many kinds of disturbances and makes the overall performance more robust with less risk of EMI. Guidelines for the improvement of the layout of the PCB are as follows:

- Separate large signal grounds from small signal grounds (see Figure 28). A triangular symbol indicates small signal grounds. All other ground symbols are related to large signal grounds
- Make the print area within the indicated large signal loops (see Figure 28) as small as possible. Each indicated large signal loop has its own color. Make the copper tracks as short and wide as possible
- The connection between both MOSFETs (PFC and flyback) and the IC driver outputs must be as short as possible (green line in Figure 28). Use wide tracks. Increase the distance between the copper tracks and/or preferably using a separate guided ground track for both connections minimizes the coupling between the PFCDRIVER and FBDRIVER. A circuit diagram according to Figure 27 can be added in case it is impossible to locate the MOSFET and IC close to each other.
- The power ground and small signal ground are only connected with one short copper track (make this track as short and as wide as possible). Preferably it should become one spot (connection between ground 4a and ground 6a, shown as a green line in Figure 28)
- Use a ground shield underneath the IC, connect this ground shield to the GND pin of the IC
- Connect all series connected resistors that are fixed to an IC pin as close as possible to that pin
- Connect heatsinks which are connected to the component nearest corresponding ground signal. Make this connection as short as possible. Connect the heatsink of diode bridge BD1 to ground 1, Q1 to 4 and Q2 to 4b. In typical applications, all three components are often mounted on a single heatsink. If so, make one wide copper track that connects all three grounds to each other. Also combine in this copper track ground 2
- Connect the grounds of 6b to each other
- Make a local "star ground" from ground 6a, 6b, 6c, and 7. Ground 6a is the middle of the star and is connected to the GND pin (the ground of the IC)
- Grounds marked 7 do not have to be a star ground
- Place the Y-capacitor across grounds 1 and 8. Use one copper track, separated from all others for this connection. Alternatively in a typical application setup, use the heatsinks connection copper track for this purpose.
- Place C4, C15, C23 and C22 (in order of priority) as close as possible to the IC. Reduce coupling between the PFC switching signals (PFC driver and PFCAUX) and the flyback sense signals (FBSENSE and FBCTRL) as much as possible. The coupling reduction minimizes the risk of electromagnetic interference and audible noise
- Figure 28 shows an overview of the hierarchy of the different grounds at the bottom

- Connect the anode of the TL431 (ground 8) to ground 9 using one special separate connecting copper track. Minimize all other currents in this special track. Make the connection as close as possible to the output
- Place the TEA1792 close to the power MOSFET Q4
- Connect the ground of the TEA1792 directly to a wide and short copper track to the source of Q4
- Connect the series resistor R32 directly between the drain of Q4 and the V_{CC} pin of the IC. Use a separate copper track for this purpose
- Make the connection between MOSFET Q4 and the TEA1792 driver pin as short as possible (green line in Figure 28). Use a guided ground track
- Make the connection between R50 and SWDET of the TEA1703 as short as possible and place the resistor close to the IC

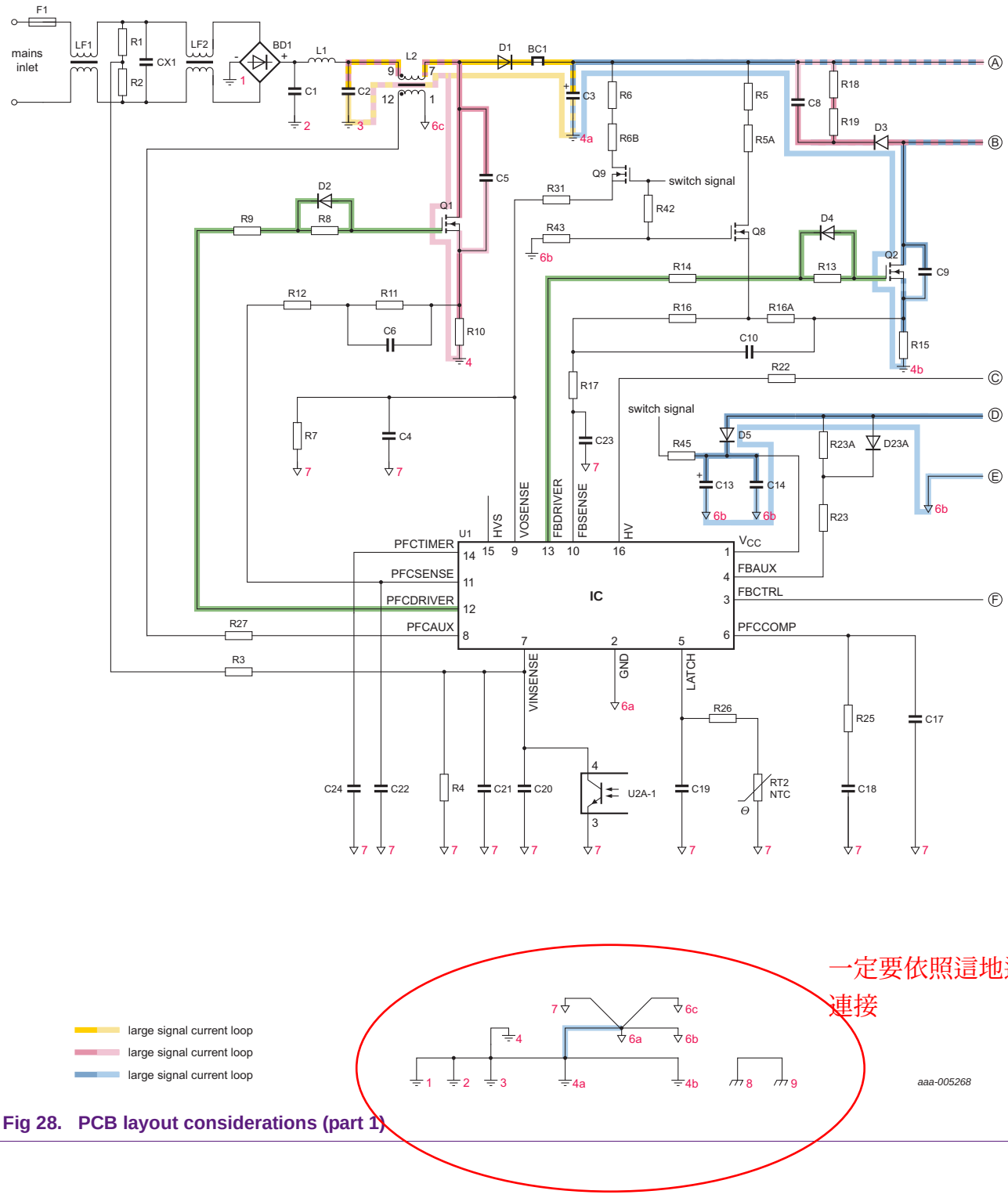
Remark: It is recommended to use the circuit shown in Figure 27 when the distance between the IC drive output and corresponding MOSFET are relatively large.



Transistor is mounted close to the MOSFET with wide and short tracks.

See Section 7for the layout rules.

Fig 27. Switching off the MOSFET when the distance between IC and MOSFET is large



一定要依照這地迴路規則連接

Fig 28. PCB layout considerations (part 1)

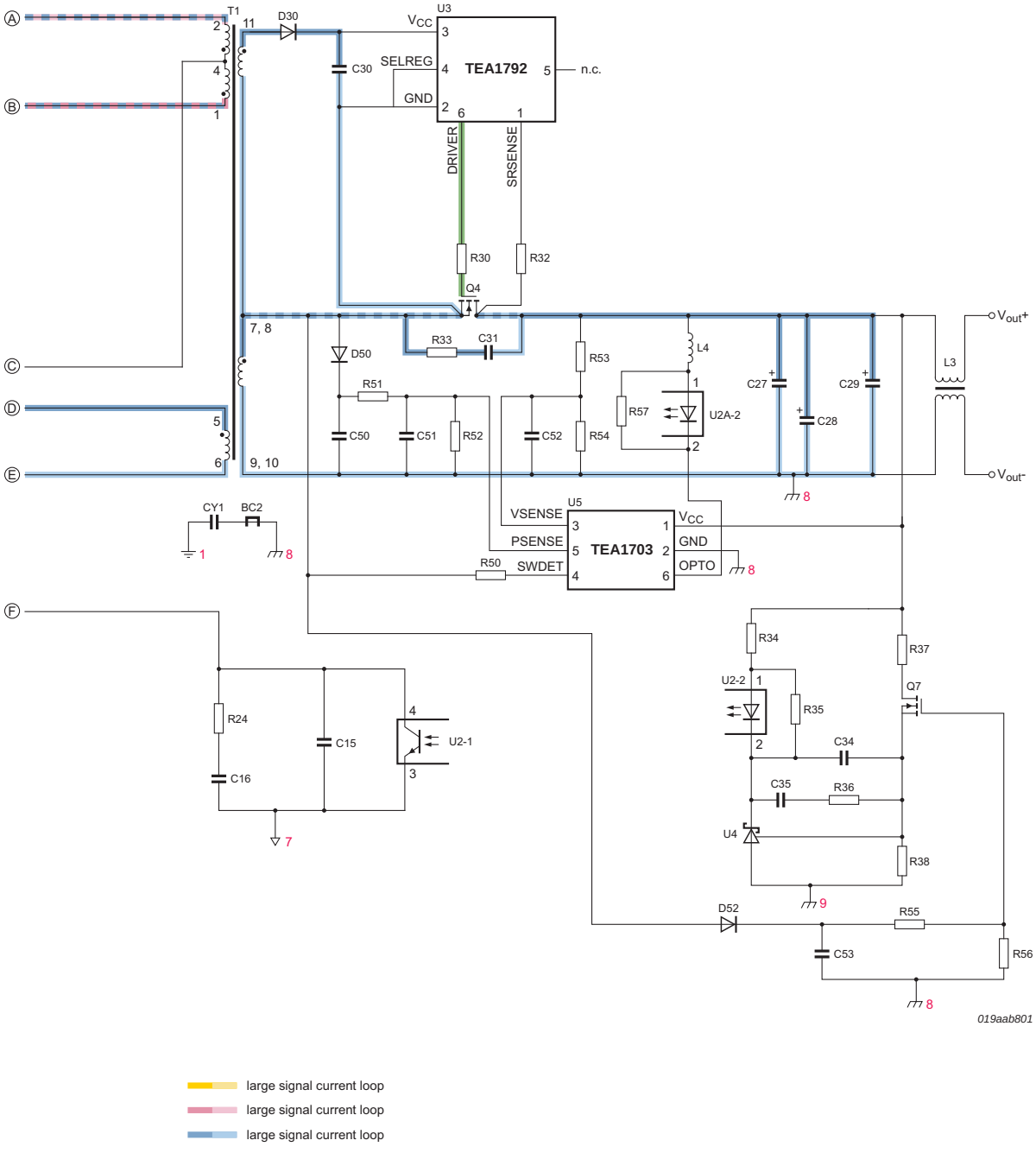


Fig 29. PCB layout considerations (part 2)