



Engineering Test Report

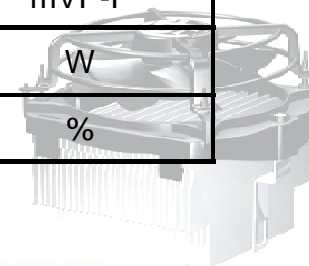
Design of 5V@1.5A ; 9V@1.5A ; 12V1.1A Quick Charge Charger with ACT4455 and FT-150 (Quick Charge 2.0 Interface IC)

Features:

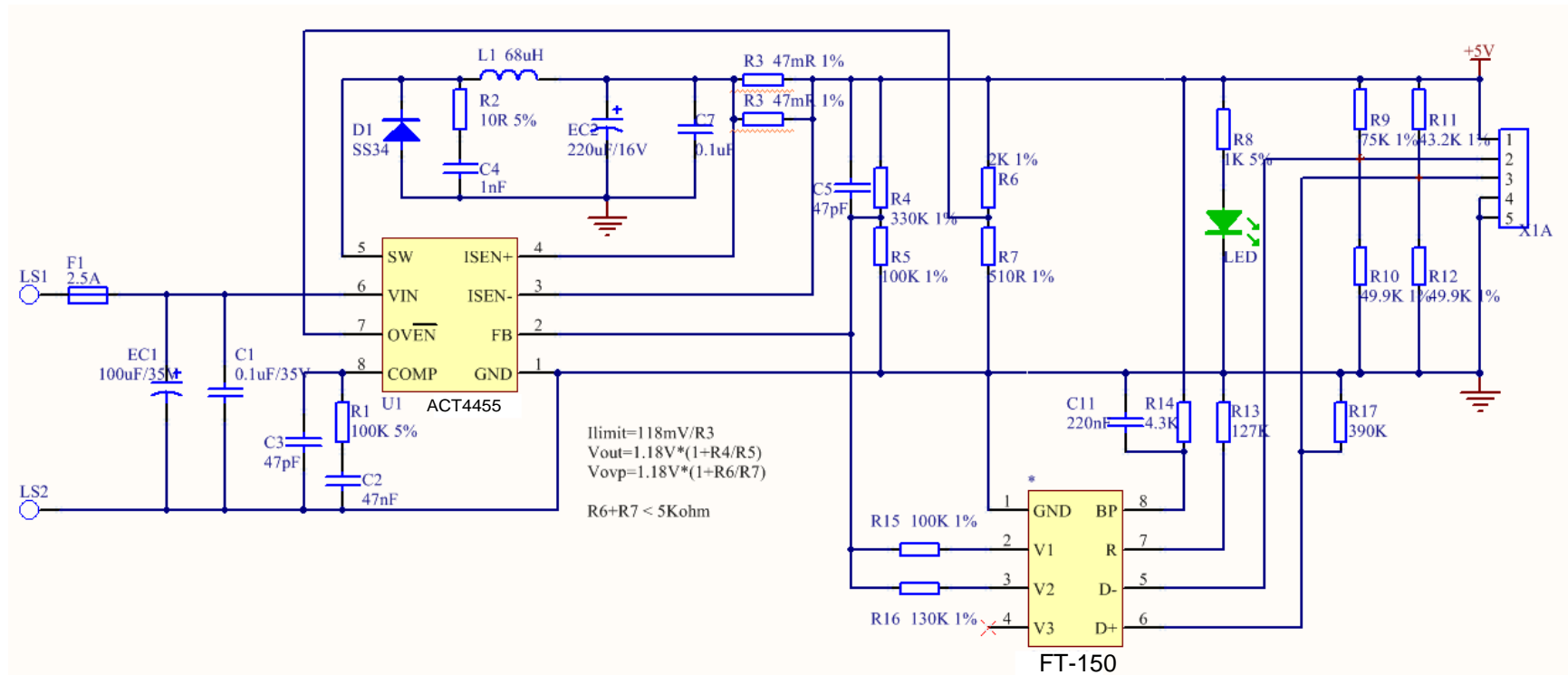
- ACT4455 Duty ratio:0% to 100% PWM control
- With 100% Duty, Output equal Input voltage.
- 40V Input Voltage Surge
- Qualcomm Quick Charge QC2.0 Compliance;
- Programmable Cable Compensation
- Complete System and Output Protections (SCP, OCP, OVP, OTP).

1. Power Supply Specification

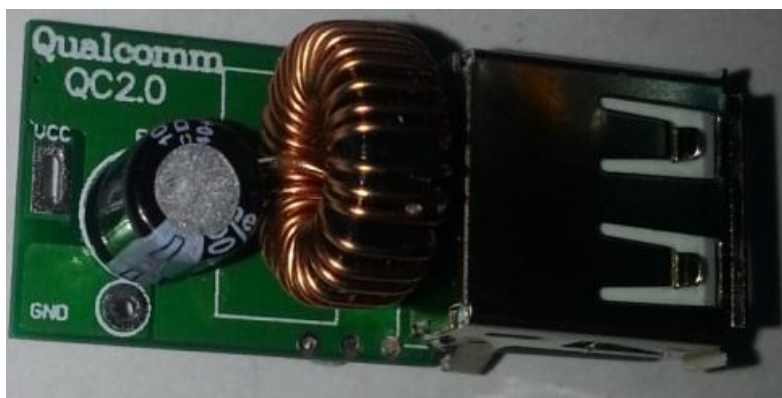
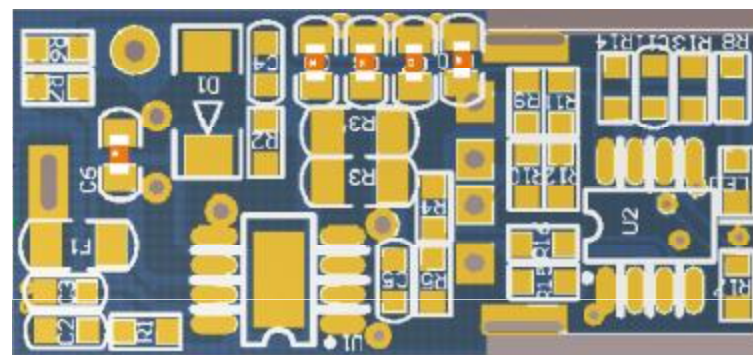
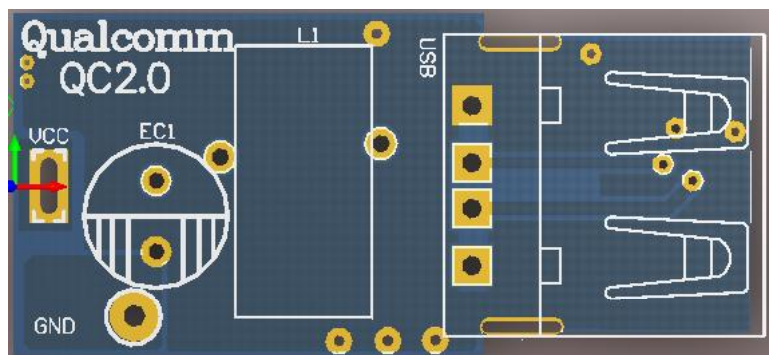
Description	Symbol	Min	Typ	Max	Units
INPUT					
Voltage	VIN	12		36	VAC
Output					
Output Voltage (5V)	VOUT	4.75	5.2	5.25	V
Output Current (5V)	IOUT	2			A
Output Ripple Voltage (5V)	VRIPPLE			100	mVP-P
Output Voltage (9V)	VOUT	8.55	9	9.45	V
Output Current (9V)	IOUT	1.5			A
Output Ripple Voltage (9V)	VRIPPLE			100	mVP-P
Output Voltage (12V)	VOUT	11.4	12	12.6	V
Output Current (12V)	IOUT	1.1			A
Output Ripple Voltage (12V)	VRIPPLE			100	mVP-P
Continuous Output Power	POUT		13.5		W
Average Efficiency	η		90		%



2. Schematic



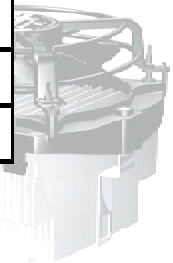
3. EV Board



4. Cable compsation, Ripple % Efficiency Measurement

OUTPUT_5V

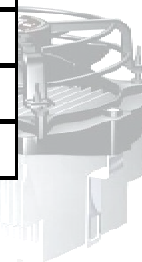
V _{IN} (VDC)	V _{IN} (V)	I _{IN} (mA)	V _{OUT} (V)	I _{OUT} (mA)	V _{RIPPLE} (mV)	P _{OUT} (W)	η (%)
12	12.73	<1	5.08	0	8.9	0.00	
	12.73	214	5.12	500	20	2.56	93.97%
	12.67	440	5.16	1000	21.4	5.16	92.56%
	12.4	930	5.23	2000	23.6	10.46	90.70%
	12.31	1149	5.28	2400	25.8	12.67	89.59%
24	24.38	<1	5.08	0	10.5	0.00	
	24.25	117	5.13	500	23.6	2.57	90.40%
	24.18	235	5.17	1000	24.8	5.17	90.98%
	23.87	488	5.25	2000	30	10.50	90.14%
	24.01	597	5.28	2400	33.2	12.67	88.41%
30	30.45	<1	5.08	0	10.8	0.00	
	30.37	95	5.14	500	24.8	2.57	89.08%
	30.22	191	5.18	1000	26	5.18	89.74%
	30.13	394	5.26	2000	31.6	10.52	88.62%
	30.08	480	5.29	2400	34.3	12.70	87.93%



4. Cable compstation, Ripple % Efficiency Measurement

OUTPUT_9V

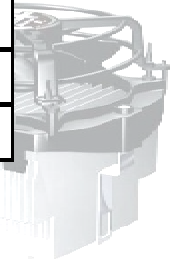
V _{IN} (VDC)	V _{IN} (V)	I _{IN} (mA)	V _{OUT} (V)	I _{OUT} (mA)	V _{RIPPLE} (mV)	P _{OUT} (W)	η (%)
12	12.93	<1	8.98	0	10.4	0.00	
	12.56	368	9	500	22.4	4.50	97.36%
	12.36	757	9.05	1000	25.6	9.05	96.72%
	12.12	1175	9.09	1500	24.8	13.64	95.74%
	11.92	1616	9.14	2000	26.4	18.28	94.90%
24	24.65	<1	8.97	0	12.8	0.00	
	24.42	196	9.02	500	36.8	4.51	94.23%
	24.31	394	9.06	1000	46.8	9.06	94.59%
	24.17	600	9.08	1500	48.1	13.62	93.92%
	24.01	811	9.13	2000	56.8	18.26	93.78%
30	30.67	<1	8.98	0	14.4	0.00	
	30.38	159	9.03	500	38.4	4.52	93.47%
	30.37	319	9.08	1000	46.4	9.08	93.72%
	30.25	484	9.11	1500	48.8	13.67	93.33%
	30.12	654	9.14	2000	60	18.28	92.80%



4. Cable compsation, Ripple % Efficiency Measurement

OUTPUT_12V

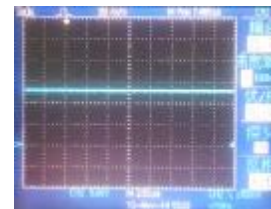
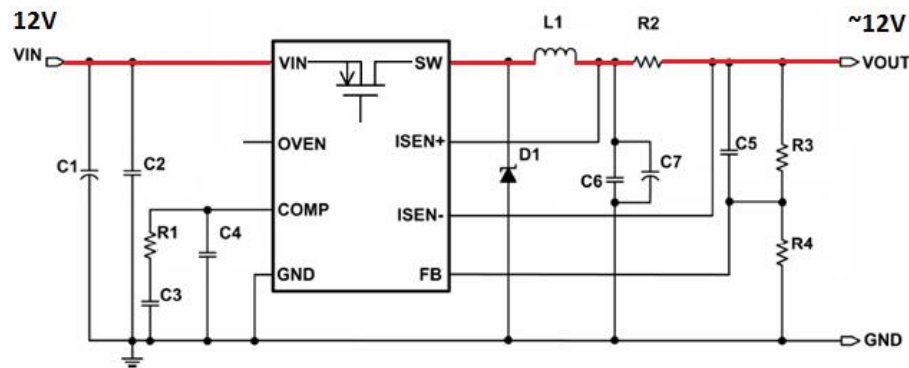
V _{IN} (VDC)	V _{IN} (V)	I _{IN} (mA)	V _{OUT} (V)	I _{OUT} (mA)	V _{RIPPLE} (mV)	P _{OUT} (W)	η (%)
12	12.73	2	11.96	0	14.4	0.00	
	12.7	481	12	500	36.8	6.00	98.2%
	12.55	977	12.04	1000	24.8	12.04	98.2%
	12.63	1071	12.05	1100	38.2	13.26	98.0%
	12.86	1930	12.13	2000	45.6	24.26	97.7%
24	25	1	11.98	0	10.4	0.00	
	24.7	255	12.01	503	48.8	6.04	95.9%
	24.56	513	12.05	1000	51.2	12.05	95.6%
	24.52	564	12.06	1100	56	13.27	95.9%
	24.27	1052	12.12	2000	67.2	24.24	94.9%
30	30.66	1	12	0	12.3	0.00	
	30.38	209	12.03	500	57.8	6.02	94.7%
	30.29	418	12.06	1000	65.4	12.06	95.3%
	30.22	462	12.07	1100	66.4	13.28	95.1%
	30.01	855	12.13	2000	81.6	24.26	94.5%



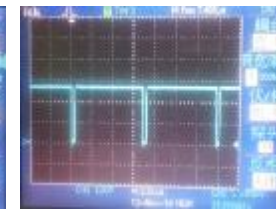
4. 12V Output Dropout 150mV@ 1A

Dropout 测试值:

Vin(V)	Vout(V)	Loading(A)	Dropout(mV)
11.98	11.96	0	10mV
11.97	11.82	1	150mV
11.96	11.66	2	300mV



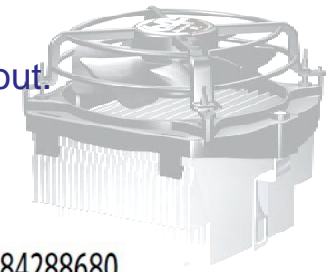
ACT4455
100%Duty



Competitor
90% Duty

备注:

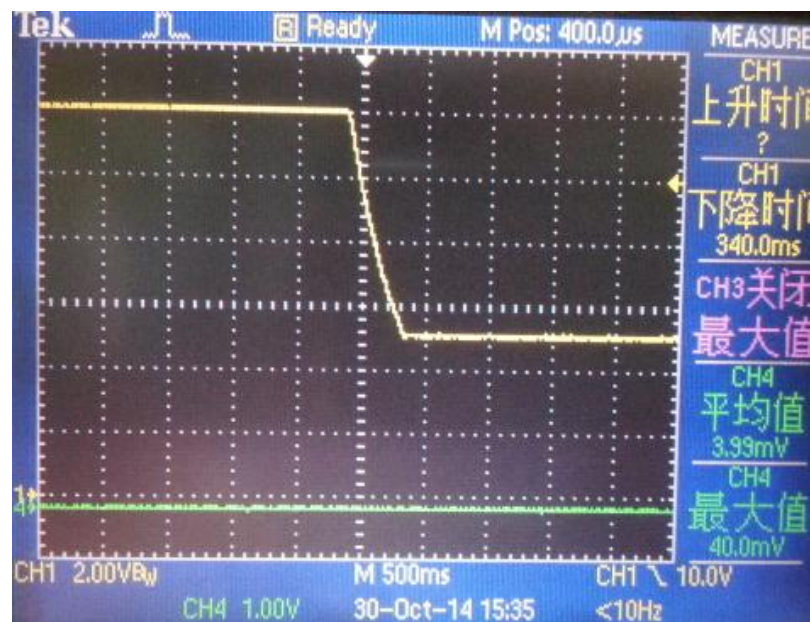
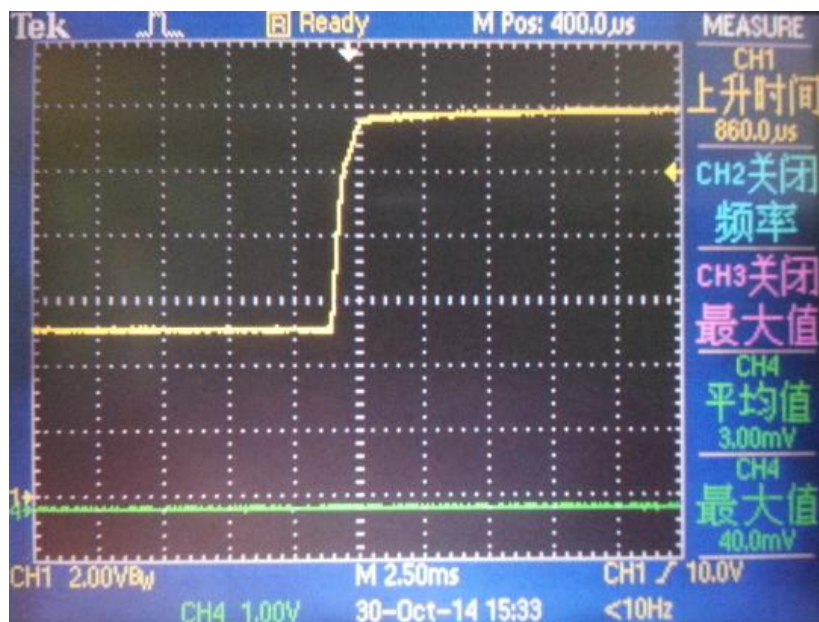
- 1.电压12V输入时可12V电压输出.
- 2.因 ACT4455在100% Duty时, IC内MOS处于一直导通状态, Vin输入会直通到Vout.
- 3.满载输出时, 只通路中PMOS / 电感L1 / 限流电阻R2及PCB走线等阻抗的压降, 总阻抗<150mΩ.
- 4.目前竞争者产品无法直通.



5. Voltage Transition-A

Test conditions:

- Output at No_Load
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals

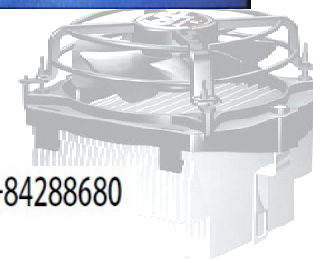


Output: 5V à 12V no load

深圳市坪山新区坪环街道坪环工业城德昌东街8号

电话: 0755-28823348

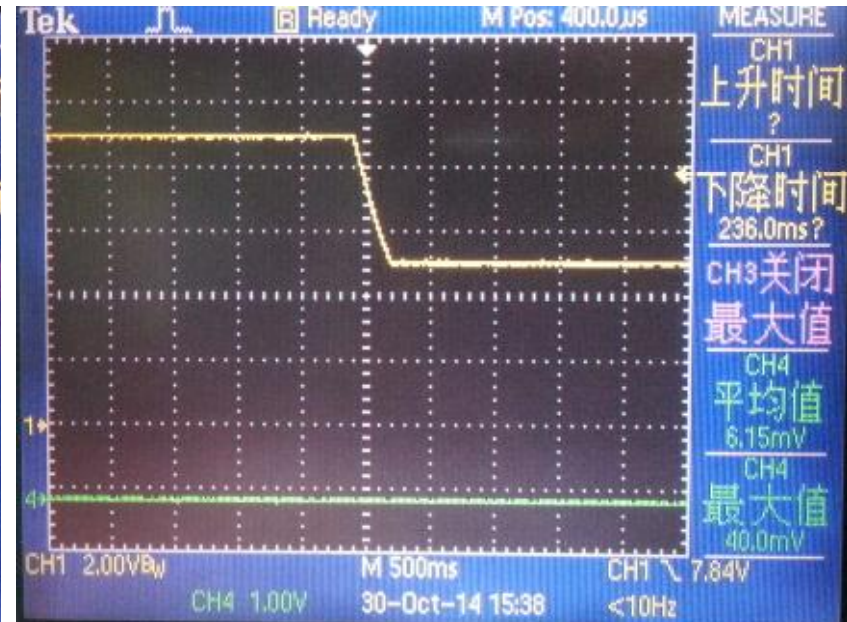
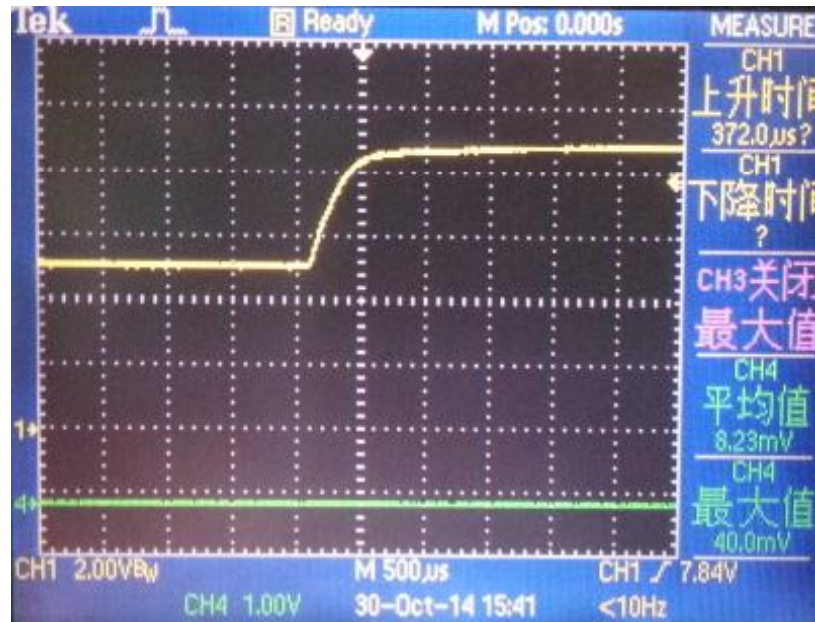
传真: 0755-84288680



5. Voltage Transition-B

Test conditions:

- Output at No_Load
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals

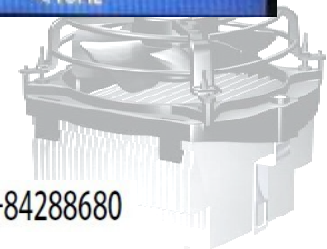


Output: 5V → 9V no load

深圳市坪山新区坪环街道坪环工业城德昌东街8号

电话: 0755-28823348

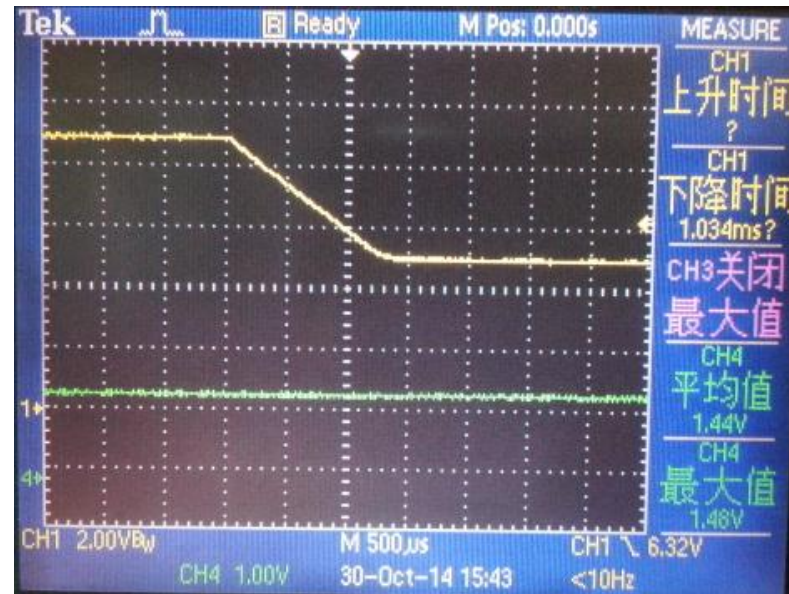
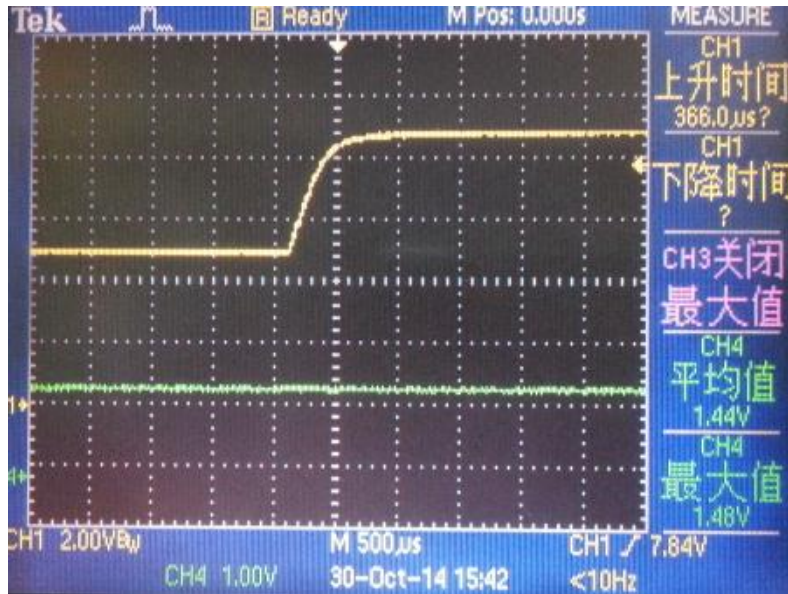
传真: 0755-84288680



5. Voltage Transition-C

Test conditions:

- Output at 1.5A (9V Full Load)
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals

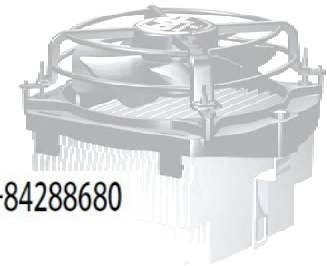


Output: 5V → 9V 1.5A Full load

深圳市坪山新区坪环街道坪环工业城德昌东街8号

电话: 0755-28823348

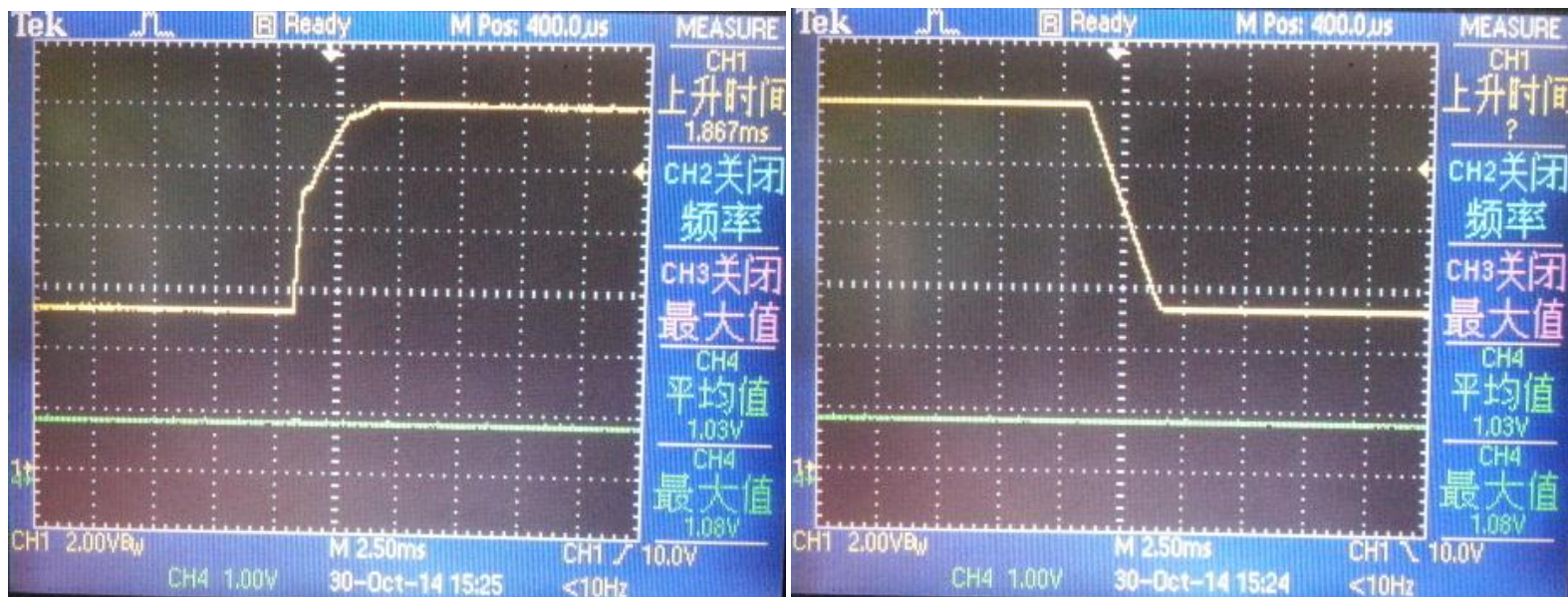
传真: 0755-84288680



5. Voltage Transition-D

Test conditions:

- Output at 1.1A (12V Full Load)
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals

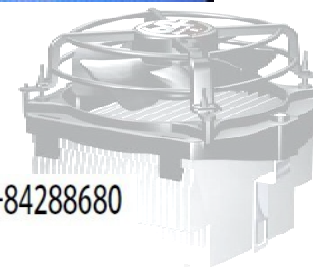


Output: 5V à 12V 1.1A Full load

深圳市坪山新区坪环街道坪环工业城德昌东街8号

电话: 0755-28823348

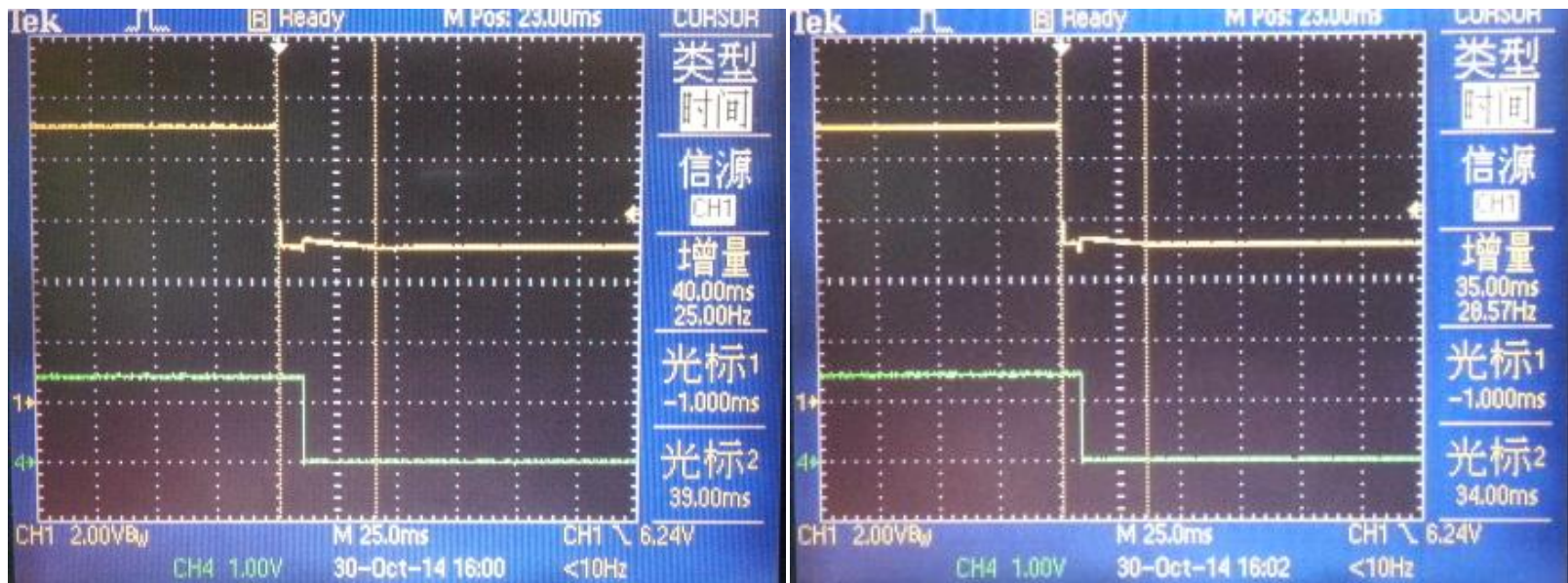
传真: 0755-84288680



6. Output Settling to 5V

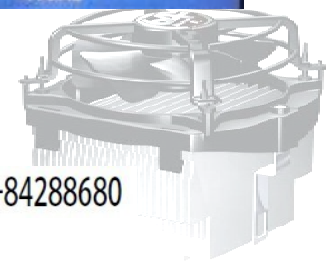
Test conditions:

- Output at 9V@ 1.5A and Switch to 5V@ 0A
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals, then unplug the USB
- Total Output capacitance is 100uF



Vin:12V

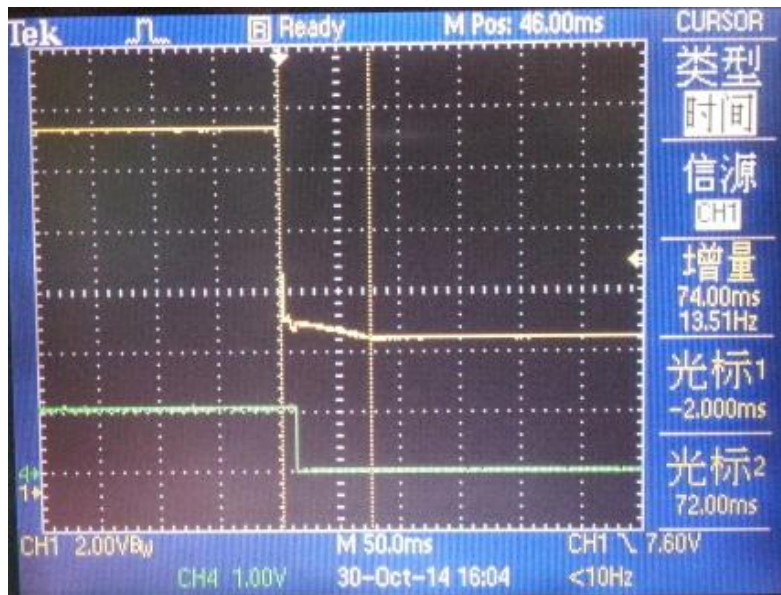
Vin:24V



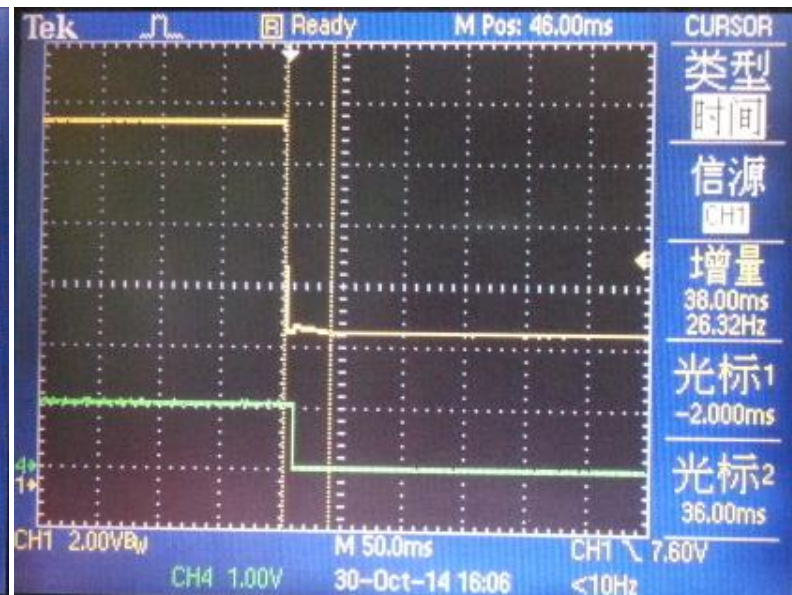
6. Output Settling to 5V

Test conditions:

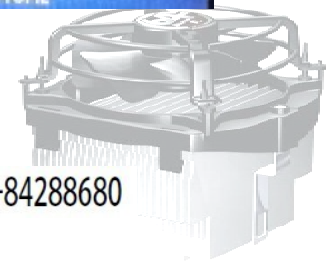
- Output at 12V@ 1.1A and Switch to 5V@ 0A
- Output voltage selected by QC2.0 Interface IC via D+ & D- signals, then unplug the USB
- Total Output capacitance is 100uF



Vin:12V



Vin:24V



8. QC 2.0 Test Setup (HVDCP Simulator with E-Load)

