AN4468
Application note

500 W fully digital AC-DC power supply based on the STM32F334 microcontroller

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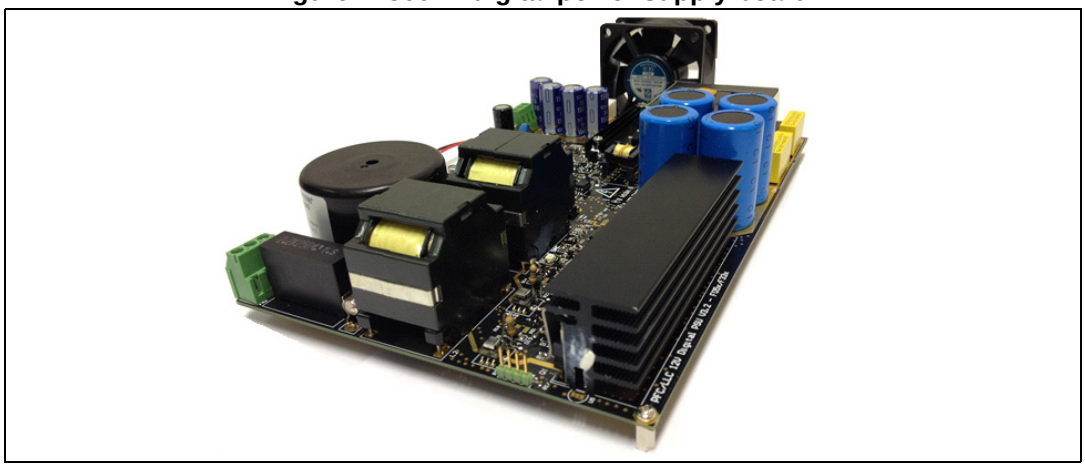
Introduction

AC-DC converters designed for a wide variety of applications, from computer adapters to server and telecom systems, require high efficiency over the entire load range of operation and across the universal mains input voltage range. Given the demand for more efficient, smaller adapters, their design is becoming more challenging and new conversion approaches, rather than the standard designs based on analog ICs, have been investigated. In particular, while the standard approach is based on the use of a boost type PFC and a regulation stage, both of which controlled using analog PWM regulators, the new, fully digital approach relies on the use of microcontrollers to control both the PFC and the DC-DC stage. This approach is increasingly being used for high density, high efficiency power electronics systems.

Figure 1. 500 W digital power supply board.



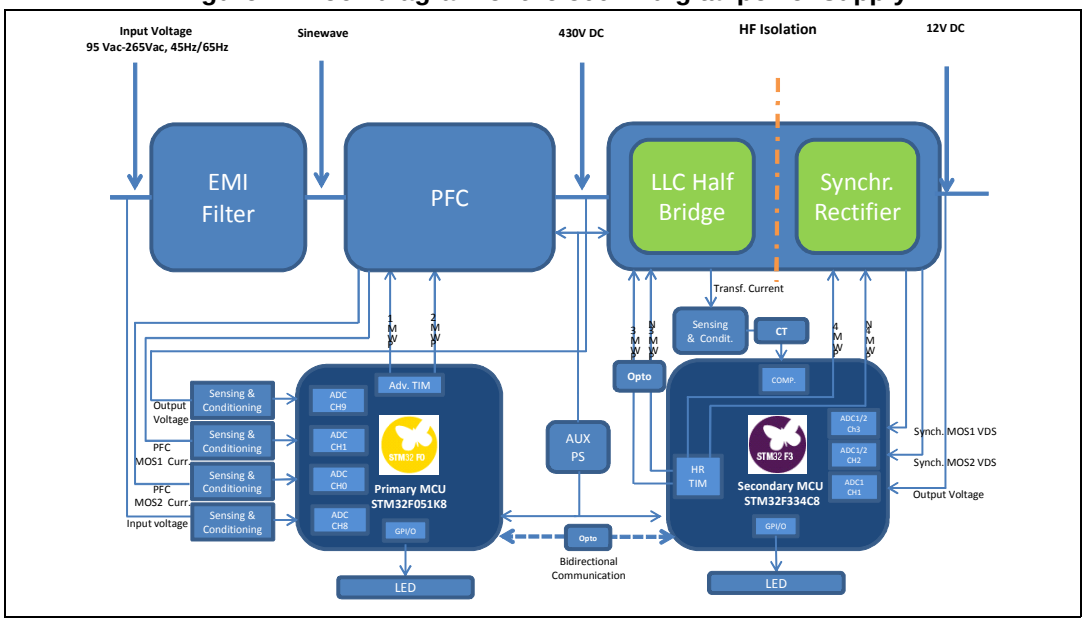
This application note focuses on the design of a 500 W AC-DC switch mode power supply with full digital control based on the STM32 family of microcontrollers. The system consists of two power stages: an input semi-bridgeless power factor corrector (SBPFC) controlled by an STM32F051K8 and a regulation stage implemented with an LLC half-bridge with synchronous rectification (SR), controlled by an STM32F334C8 microcontroller. The operating principles, main features and design choices are discussed. Details regarding the main components used for the implementation of both the power and control stages are also provided.

Contents

1 System overview

The block diagram of the 500 W digital AC-DC converter is shown in *Figure 2*. A two-stage architecture is generally implemented in this type of application.

Figure 2. Block diagram of the 500 W digital power supply



The first block, from left to right, is the EMI filter. In a standard AC-DC topology, the EMI filter is connected to the input of a diode bridge rectifier, which is then connected to the input of a PFC stage. However, this 500 W AC-DC implementation uses the so-called bridgeless PFC topology which has the advantage of lower conduction losses and higher efficiency by eliminating the need for the diode rectifier stage. This choice also has the advantage of reducing component count with respect to a standard PFC.

The input stage is typically controlled using an outer voltage loop for bus voltage regulation and an inner control loop to shape the current according to a sinusoidal waveform. The outer loop adjusts the current reference in order to maintain a regulated bus voltage independently from the load or input voltage variations. The output isolation and regulation stage is implemented using a half-bridge LLC topology operated with constant duty cycle and variable frequency control.

The DC-DC stage performs voltage step-down using an HF transformer with a primary-to-secondary turns ratio chosen to maintain good efficiency and regulation in the entire operating range. The transformer is supplied with a square wave voltage generated by the primary side active switches. On the secondary side this voltage waveform is rectified and then smoothed by the output filter. While on the primary side switching losses are reduced thanks to zero voltage switching (ZVS), on the secondary side synchronous rectification (SR) is used to ensure low conduction losses. The overall effect of these design choices is high system efficiency, in line with the stringent requirements of the power supply industry.

The system is controlled by two microcontrollers from the STM32 product family. On the primary side, an STM32F051K8 controls the bridgeless PFC by sampling the current of the two MOSFETs, the input AC voltage and the output bus voltage. Two control signals, PWM1 and PWM2, are then generated to drive two power switches. On the secondary side, an

STM32F334C8 microcontroller samples the output voltage and adjusts the frequency of the LLC bridge control signals to ensure stable operation in the overall load range. In addition, two channels of the ADC are used to sample the rising and falling edges of the drain-to-source voltage of the SR MOSFETs. The two microcontrollers exchange information about the status of the input and output power stage via bidirectional serial communication.

Both the power stage and control stage are supplied by an offline flyback circuit which provides a suitable regulated voltage to the microcontrollers, the gate drive ICs and signal conditioning circuits.

Table 1 summarizes the main specifications of the 500 W digital power supply.

Table 1. 500 W AC-DC converter specifications

Parameter	Value
Input AC voltage	95 V AC up to 264 V AC
Input AC frequency	45 Hz up to 65 Hz
Output voltage	12 V DC
PFC output voltage	430 V DC
Output power	500 W
PFC switching frequency	60 kHz
DC-DC switching frequency	70 kHz up to 130 kHz
HF transformer isolation	4 kV
Peak efficiency	93.2%
Cooling	Forced air cooling
Input short-circuit protection	10 A fuse
Output short-circuit protection	Managed by STM32F334C8
Input under/overvoltage	Managed by STM32F051K8
Input under/overfrequency	Managed by STM32F051K8
Bus DC under/overvoltage	Managed by STM32F051K8
Output under/overvoltage	Managed by STM32F334C8
Overtemperature protection	Managed by STM32F051K8 (primary) and STM32F334C8 (secondary)

The converter accepts universal input voltage and produces a 12 V regulated output. The continuous power rating of the unit is 500 W. Natural convection is used up to 300 W. Above this power level a cooling fan is activated to provide forced air cooling. The ambient operating temperature range is 0 ºC to 50 ºC.

The intermediate high-voltage DC bus is regulated at 430 V by the PFC which draws sinusoidal input current from the AC input maintaining high power factor and low current total harmonic distortion (THDI%). The LLC circuit converts this high DC voltage to low DC voltage proving isolation (4 kV) by means of an HF transformer, and high efficiency thanks to ZVS. Input and output current and voltage protection are also provided together with overtemperature protection.

2 Bridgeless PFC stage

2.1 Operating principle

The bridgeless PFC is a high efficiency topology characterized by the absence of the diode bridge rectifier and by the use of only two semiconductors in the current conduction path during any operating interval. The basic scheme of the bridgeless PFC boost converter is shown in *Figure 3*. The boost inductor is connected directly to the input AC source and split between line and neutral connection. Each inductor is connected to the drain of a power MOSFET and to the anode of a fast switching diode. The cathodes of the two diodes are connected to the output filter capacitor which is then parallel connected to the load.

The operation of this circuit is very similar to that of a standard PFC. More in detail, during the positive half-cycle of the input voltage, the boost converter composed of L1, M1, D1 and C1 is active, while during the negative half-cycle of the input voltage the boost converter composed of L2, M2, D2, and C2 is active.

Although this circuit has a reduced component count and higher efficiency compared to traditional PFC topologies, it has some drawbacks which limit its use in such a configuration. The main one is that the AC source is not referenced to the PFC ground. As a consequence, some difficulties in input voltage and inductor current sensing are introduced. Common mode EMI filtering can also be an issue related to this circuit.

A variant of the bridgeless PFC, known as semi-bridgeless PFC, is characterized by the addition of two diodes, D3 and D4, is shown in *Figure 4*. The purpose of these diodes is to keep the negative phase connected to the PFC ground, thus resolving the EMI filtering issue mentioned above for the bridgeless topology.

Figure 3. Basic scheme of a bridgeless PFC converter.

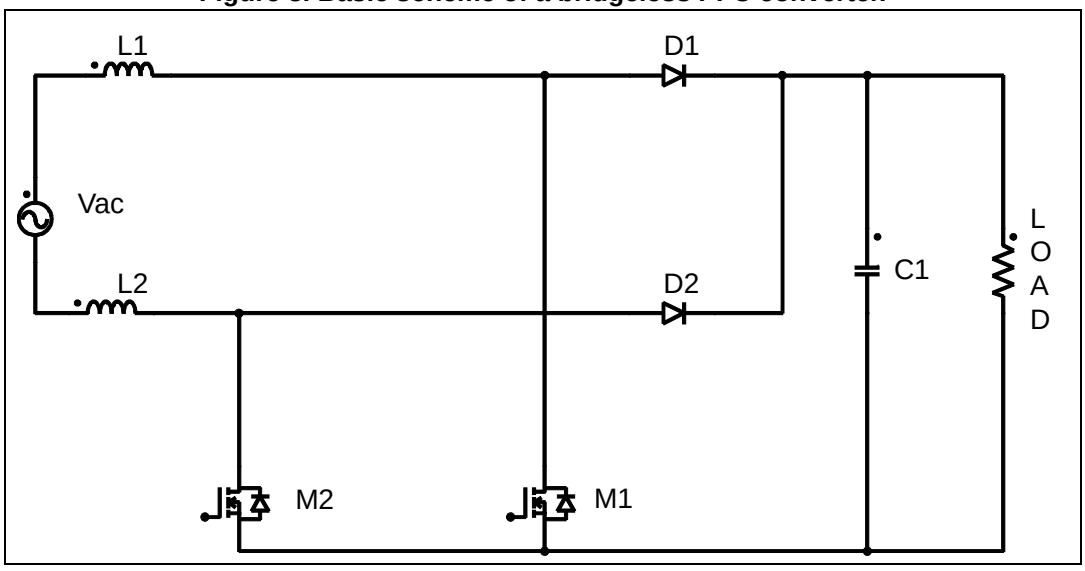
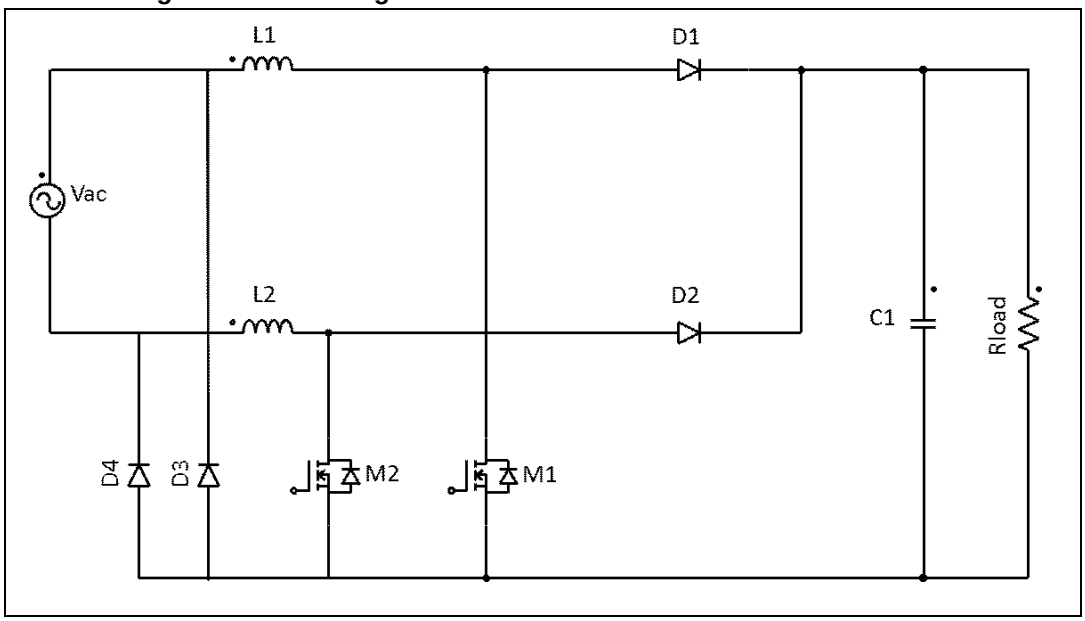


Figure 4. Semi-bridgeless PFC with addition of diodes D3 and D4

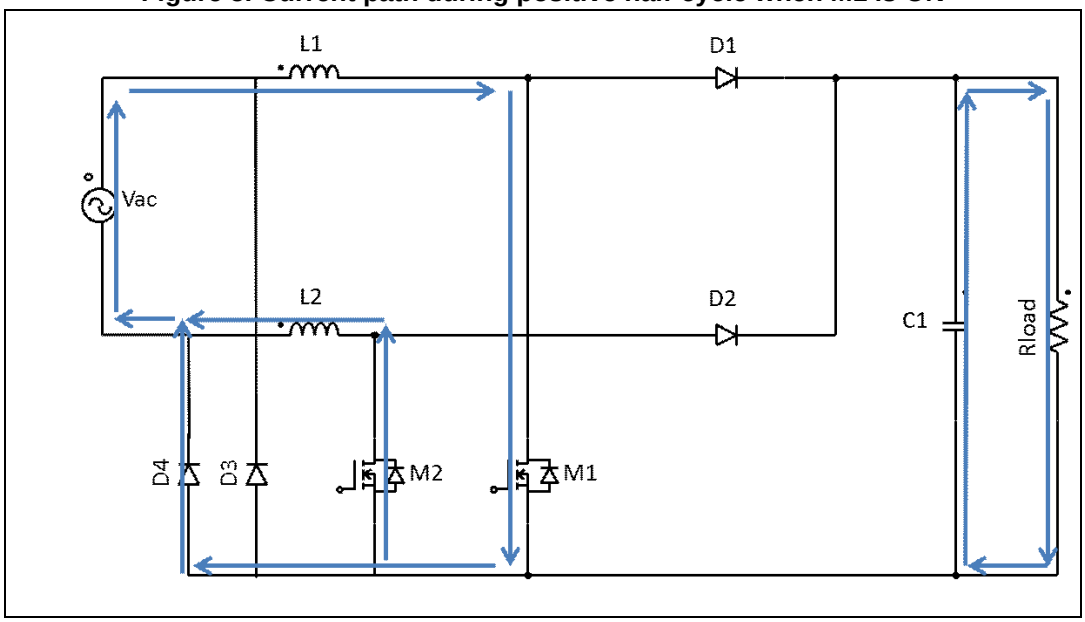


The operating principle is briefly described as follows:

- During the positive half-cycle

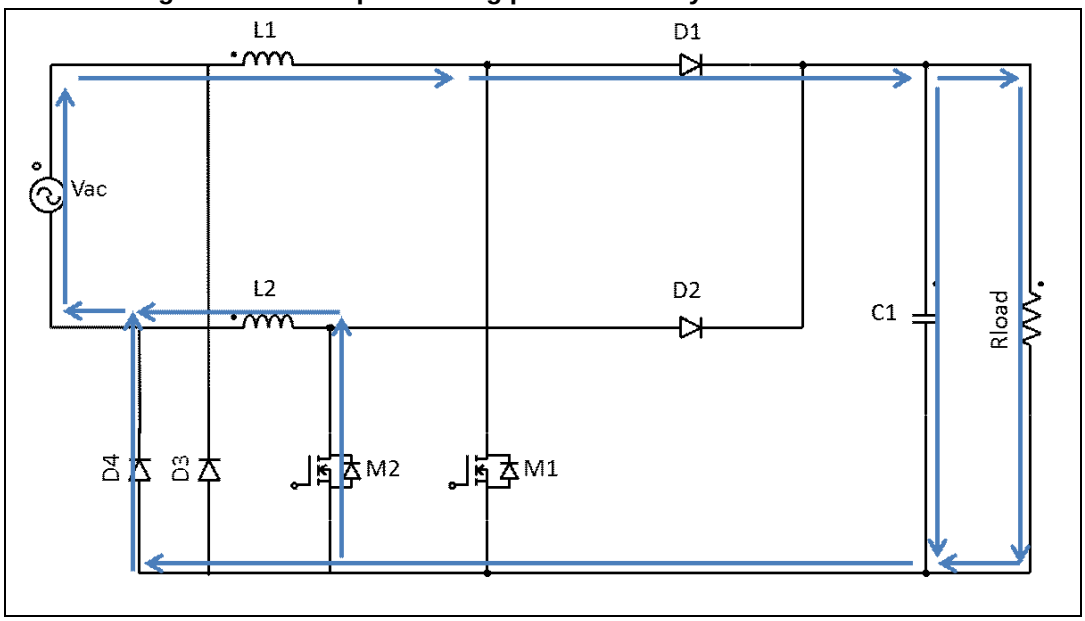
1. The input voltage diode D3 is off and D4 conducts the current returning to the source. MOSFET M1 is switched ON and OFF while MOSFET M2 is idle.

Figure 5. Current path during positive half-cycle when M1 is ON



2. When MOSFET M1 is ON the current flows as highlighted in *Figure 5*.
3. When MOSFET M1 is OFF the current flows as highlighted in *Figure 6*.

Figure 6. Current path during positive half-cycle when M1 is OFF

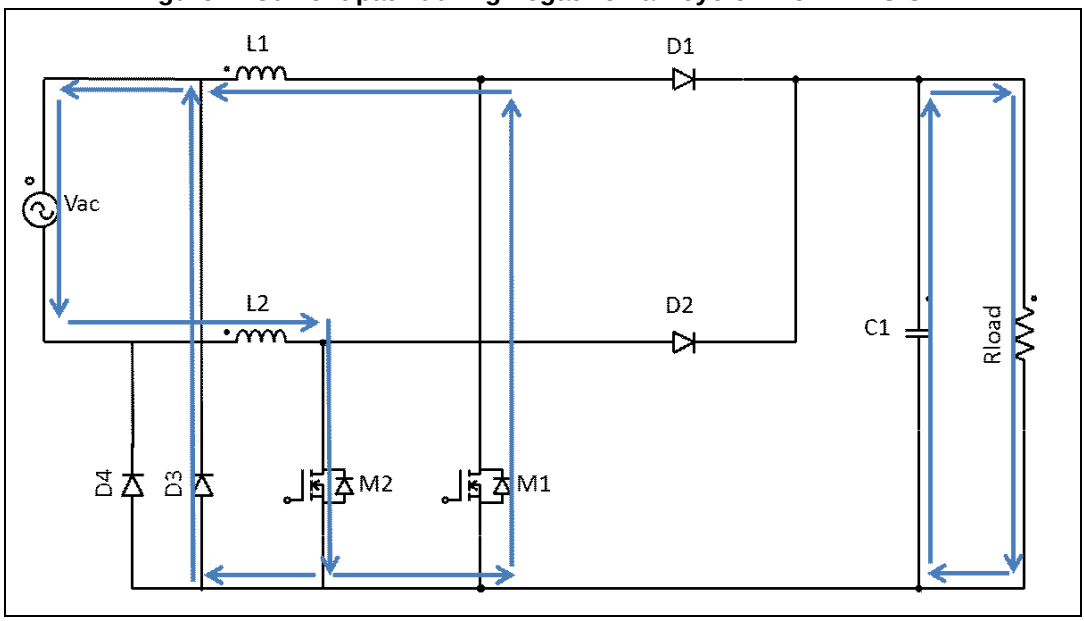


4. The return path of current is offered by the parallel of diode D4 and the body diode of M2.

- During the negative half-cycle of the input voltage:

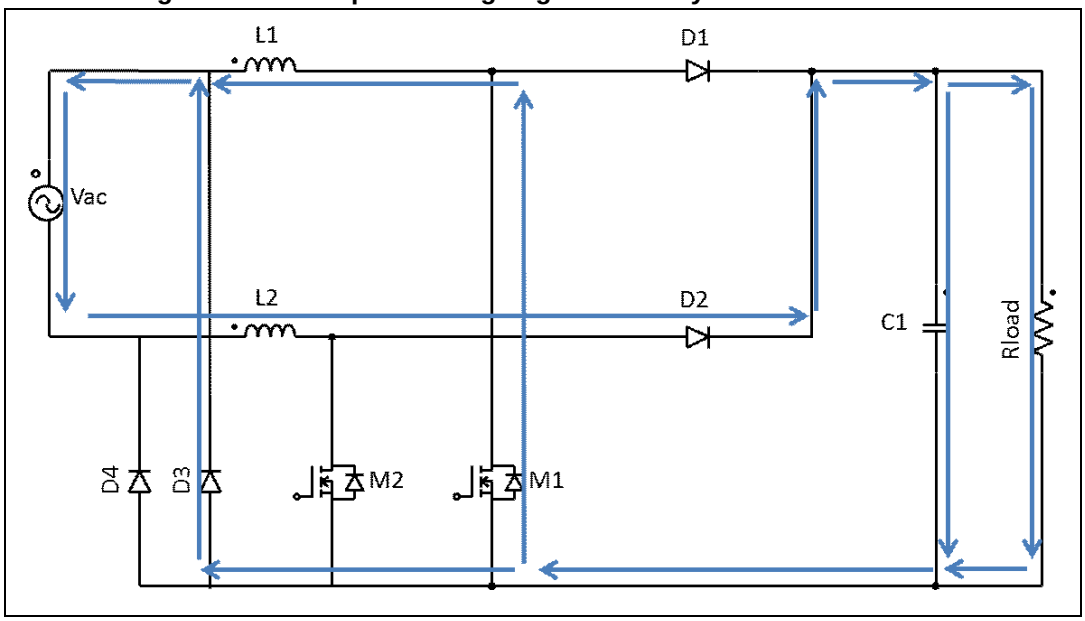
1. Diode D4 is OFF and diode D3 conducts the current returning to the source. In this case M2 is switched ON and OFF while M1 is idle.
2. When M2 is ON current flows as shown in *Figure 7*.

Figure 7. Current path during negative half-cycle when M2 is ON.



3. When M2 is OFF, the current flows as shown in *Figure 8*

Figure 8. current path during negative half-cycle when M2 is OFF



4. The return path of the current is offered by the parallel of diode D3 and the body diode of M1.

Note that in the previous analysis it has been supposed that during the positive and negative half-cycles one of the two MOSFETs is switching and the other is idle. There are actually two additional control strategies besides the one mentioned above.

In the first, during the positive half-cycle of the input voltage M1 is switched ON and OFF while M2 is kept ON. During the negative half-cycle of the voltage, M2 is switched ON and OFF while M1 is kept ON. This control strategy allows the return current to flow across the channel of the MOSFET rather than across the body diode and, therefore, some improvement in efficiency is possible.

In the second, both MOSFETs are controlled synchronously, with the same PWM signal applied to each gate. Again, the benefit is lower power dissipation when current flows through the MOSFET during the return phase. In addition, only one driver can be used for both MOSFETS.

Due to these advantages, the PFC topology chosen for the 500 W digital power supply implementation described in this application note is the semi-bridgeless PFC with synchronous control.

2.2 Semi-bridgeless PFC design

The practical implementation of the proposed 500 W bridgeless boost PFC rectifier is detailed in this section. The converter is designed to operate in DCM. In low and medium power applications, discontinuous and critical conduction mode are often used to obtain numerous benefits such as reduced switching losses, low diode reverse recovery current and small inductor size.

The PFC was designed starting from the specifications shown in *Table 2*.

Table 2. Specifications of the 500 W Bridgeless PFC

Parameter	Value
Input AC voltage	90 V AC up to 264 V AC
Input AC frequency	45 Hz up to 65 Hz
Output voltage	12 V DC
PFC output voltage	430 V DC
Output power	500 W
PFC switching frequency	60 kHz
Efficiency	>95%

The design steps are reported as follows:

- Maximum input RMS current value

Considering the minimum input voltage and the minimum desired converter efficiency, the maximum RMS value of the input current can be calculated.

Equation 1

$$I_{in\_RMS\_max} = \frac{P_{out}}{\eta \cdot V_{in\_RMS\_min}} = 5{,}84\text{A}$$

- Maximum input peak current value

Equation 2

$$I_{in\_pk\_max} = \sqrt{2} \cdot I_{in\_RMS\_max} = 8{,}24\text{A}$$

- Boost inductor value

The inductance value of the two input chokes has to be carefully selected in order to ensure DCM operation across the universal input voltage range and load range. This is guaranteed if the inductor is selected according to equation 3:

Equation 3

$$L < \frac{M-1}{4 \cdot M^3} \cdot R \cdot T = 95uH$$

Where $M=V_{out}/V_{in}$ is the converter voltage gain, $R=V_{out}^2/P_{out}$ is the load resistance and T is the switching period. Note that in equation 3 the minimum value of peak input voltage has been considered for the calculation of the value of the input inductors.

Two 100 µH, 10 A RMS inductor chokes, characterized by a 33 mΩ DC resistance have been selected for this application. The peak-current rating of the inductor must be well above the expected peak current of the converter to avoid core saturation. A gapped ferrite with core material characterized by low core losses at the design switching frequency of 60 kHz has been used.

- Inductor peak current

The inductor peak current can be calculated with equation 4:

Equation 4

$$I_{Lpeak} = \frac{Vin\_pk_{min}}{L} \cdot t_{on\_max} = 18{,}9A$$

Equation 5

$$D_{max} = \frac{t_{on\_max}}{T_s} = 0.9$$

Where it is assumed that the duty cycle is limited to a maximum of 0.9

- Power MOSFET selection

The choice of power semiconductors is fundamental to meet the efficiency requirements of the application. In a boost PFC, when the switch is on the current is equal to the inductor current. The peak current calculated in equation 4 is also the peak current of the switch. When the switch is off, the drain-to-source voltage is the output voltage. Therefore, the MOSFET is selected with a rated voltage greater than the output voltage and rated current greater than the maximum inductor current. Since the boost PFC operated in DCM is mainly affected by conduction losses, it is very important to use a power MOSFET with low drain-to-source resistance in order to ensure high efficiency. The output voltage of the device value is chosen according to equation 6:

Equation 6

$$Vds_{mos} > 1.3 \cdot V_{out} > 559V$$

To meet the design requirements, the STP57N65M5 N-channel power MOSFET has been used for M1 and M2. This device is characterized by a minimum breakdown voltage of 650 V and a maximum on resistance of 63 mΩ at 25 °C. The total gate charge is 98 nC.

- Rectifier diodes selection

The average diode current can be calculated as:

Equation 7

$$I_D = \frac{P_{out}}{V_{out}} = 1.16A$$

Two STPSC1006D 600 V, 10 A diodes are used as rectifier diodes. The forward voltage drop at 1.16 A is about 0.75 V at T_J=150 °C.

- Output capacitor selection

The output capacitor bank value is selected to limit the output voltage ripple to 1% of the nominal output voltage. Equation 8 has been chosen to define the value of the output capacitor bank:

Equation 8

$$C_{out} = \frac{P_{out}}{2\omega\Delta V_0 V_0} = 430uF$$

Where ω is the mains angular frequency and ΔV_0 is the output voltage ripple. Four 450 V, 100 uF electrolytic capacitors from Vishay have been parallel connected on the PFC output. In addition, a 600 V, 560 nF ceramic capacitor with low ESR and ESL is connected in parallel to the each electrolytic capacitor.

- Input filter capacitors

The need for a high power factor introduces a limit on the maximum capacitance that can be placed across the line. The maximum capacitance is a function of how much phase shift that can be tolerated. This phase shift angle can be calculated using equation 9.

Equation 9

$$\Theta = tan^{-1}\left(\frac{\omega \cdot Vin_{max} \cdot C_{in}}{I_{in}}\right)$$

Choosing C_{in}=3 uF the total displacement is 7°.

- Current sensing

The current flowing across each power switch is sensed by means of CTs. These are placed between the inductor and the MOSFET. Due to this placement, only the rising part of the inductor current is available to the control algorithm. The current signal is always sampled at the mid-point of the gate control PWM. Then, the current samples could be digitally corrected in order to calculate the average inductor current. In fact, contrary to the CCM case, when the PFC is in DCM the current sensed at the mid-point of the MOSFET triangular current waveform is no longer equal to the inductor average current.

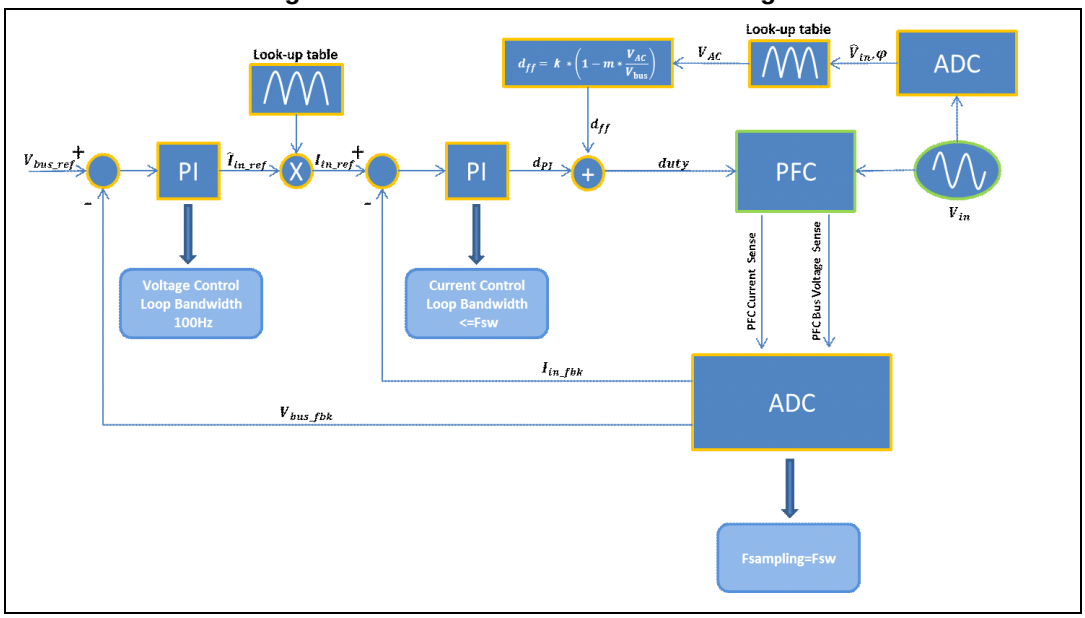
The CT must withstand the peak current calculated in equation 4. The selected current sense transformer is the 53040C from Murata. This is characterized by a magnetizing turns ratio of 40.

2.3 PFC control algorithm

This section contains an overview of the PFC digital average current-mode control method in discontinuous conduction mode (DCM). This control method allows good input current shaping in terms of harmonic distortion (low THD) and synchronization with input voltage (PF close to one). The proposed control technique estimates the average value of the inductor current in each switching cycle. The average inductor current can be precisely estimated by the digital controller modifying the sampling instant within the switching period and calculating a correction factor. Sampling the inductor current more than once in a switching cycle, with a high-performance A/D converter, also helps to achieve a precise average inductor current estimation.

The control is implemented by means of a conventional current sensing circuit and a 32-bit microcontroller, the STM32F051K8 from the STM32 family, which features a fast 12-bit A/D converter. As in traditional average current mode control implementations, this algorithm uses two control loops: an outer voltage loop, performed at 100 Hz providing the regulation of the bus voltage output at the reference value (430 V) and an inner current loop, performed at 20 kHz, to ensure that the input current follows a sinusoidal reference in phase with the input voltage. While the voltage control is achieved with a single linear regulator, the current control is based on a PI controller plus a feed-forward controller.

Figure 9. PFC control scheme block diagram



A block diagram of the control scheme is shown in *Figure 9*. The average inductor current is forced to follow the reference current, which is proportional to a rectified sinusoidal voltage synchronized to the input voltage and reconstructed by a lookup table, so that unity power factor is achieved. The lookup table provides the sinusoidal values in a [0°, 90°] range with 1.15 fixed-point format (1 bit for the integer part and 15 bits for the decimal part), with the amplitude given by the output of the voltage PI regulator.

The STM32 microcontroller calculates the duty cycle in every three switching cycles based on the error between the feedback current and the reference current values. The two switches are then controlled with these duty cycle values to achieve unity power factor and sinusoidal input current waveform. The whole digital average current mode control includes:

1. bus voltage and MOSFETs current sampling
2. voltage error calculation
3. voltage PI regulation
4. reference current calculation
5. current error calculation
6. current PI regulation
7. duty cycle feed-forward generation
8. final duty cycle computation.

The final calculated duty cycle value is therefore composed of two terms: an open loop, feed-forward term, which depends on the instantaneous input and output voltage values, and a closed loop term which depends on the applied load. The input voltage value of the feed-forward term is obtained by means of the same lookup table used to calculate input voltage amplitude and phase. This choice is effective for noise reduction and for compensation of sampling delays.

Considering only half the period of the input sinusoid, the expression of the duty cycle for the boost converter in CCM is:

Equation 10

$$d(t) = 1 - \frac{V_{in}|\sin \omega t|}{V_o}$$

where V_o is the output bus voltage, and V_{in} sin ωt is the mains voltage. However, this converter is designed to work in DCM and therefore the correct expression of the duty cycle is:

Equation 11

$$d(t) = D \cdot \sqrt{1 - \frac{V_{in}|\sin \omega t|}{V_o}}$$

where D is the constant duty cycle in absence of modulation. Since the implementation of this formula is quite complex, the feed-forward duty cycle term has been calculated using the following expression:

Equation 12

$$d(t) = k_{ff} \cdot \left(1 - m \cdot \frac{V_{in}|\sin \omega t|}{V_o}\right)$$

Where k_{ff} is a gain depending on the load and the input voltage and m is a constant modulating index.

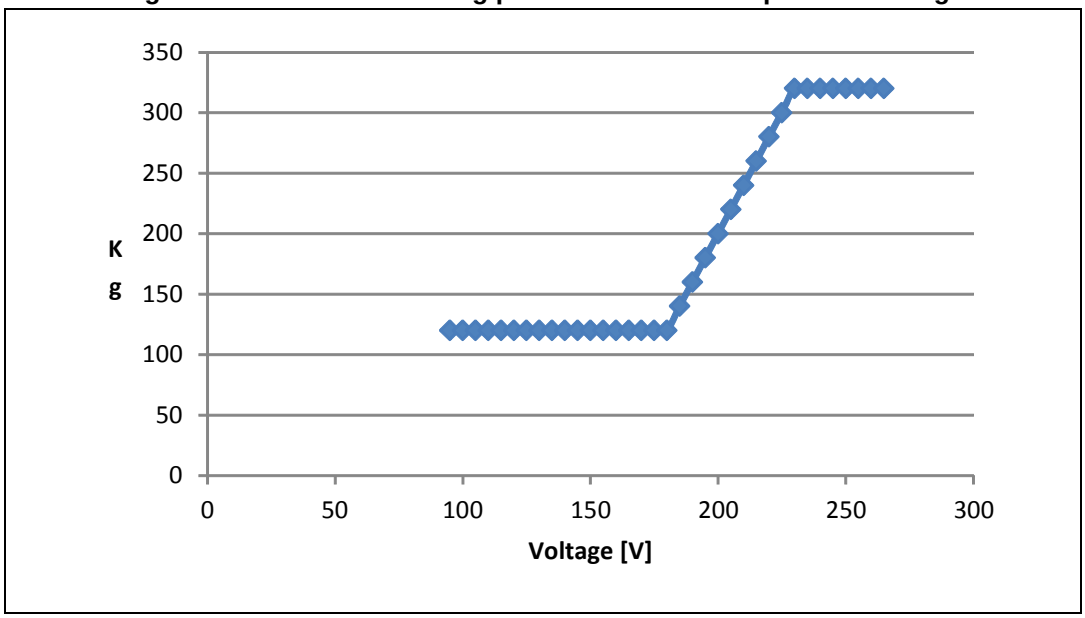
The gain k_{ff} increases with load and decreases with input voltage. Since the output of the PI voltage regulator depends on the load, the expression chosen for feed-forward duty cycle gain is the following:

Equation 13

$$k_{ff} = k_g \cdot \frac{V_{PIout}}{V_{in}}$$

where V_{in} is the amplitude of mains voltage, V_{PIout} is the output of the voltage PI regulator and k_g is a gain that varies with the input voltage amplitude according to the diagram shown in *Figure 10*.

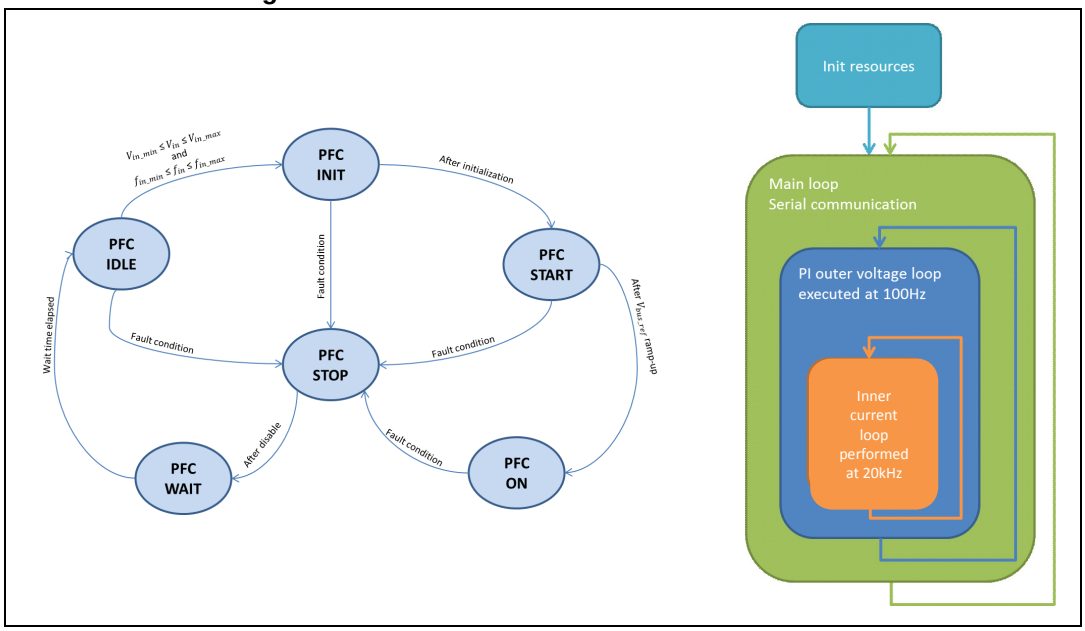
Figure 10. variation of the Kg parameter with the input PFC voltage



2.4 PFC firmware overview

The execution of the PFC firmware is based on the implementation of a state machine made up of six states. The diagram in *Figure 11* provides an overview of the firmware architecture. As soon as the microcontroller is supplied, all the peripherals are configured and the firmware is in PFC IDLE state. Here the system waits for the AC mains insertion and verifies that no faults are present. If no faults are detected, the new state is PFC INIT. In this state the integral terms of PI regulators are reset and the PM8834 (PFC MOSFET driver) is enabled. The PFC output reference voltage is initialized to the last sampled value. After this, the new state is PFC START, where the output voltage ramp function is executed. When the ramp is completed and the output voltage is equal to 430 V DC, the LLC L6491 driver is enabled and a serial command is sent to the secondary microcontroller to confirm that the PFC startup is completed. Then, the feed-forward duty cycle control is enabled and the next state is PFC ON. If in any of the above states a fault condition is verified the system is forced into PFC STOP state.

Figure 11. PFC firmware state machine overview



The possible faults are:

- Input voltage under/overfrequency (F< 45 Hz; F>65 Hz)
- Input under/over voltage (Vin< 95 V RMS; Vin>264 V RMS)
- Bus DC undervoltage (320 V)
- Bus overvoltage (Vbus>470 V)

In any of these cases both the PFC and LLC PWM modulation are disabled. The MOSFET driver enabling signal is low and the system is in PFC WAIT state for 5 seconds before the system enters the PFC IDLE state.

If during PFC operation, the bus voltage is greater than 450 V but lower than 470 V, the PFC operates in BURST MODE. In this case, the PFC is forced into the STOP state and only the PFC modulation is disabled while the LLC converters continue to operate. The WAIT state is bypassed and the system is forced into IDLE state. The PWM modulation is re-enabled when the PFC bus voltage is below 430 V.

As described above, the control firmware performs several tasks, with different timings and priorities to ensure both output voltage regulation and input current regulation. The main

tasks and functions are summarized in *Table 3*, together with the execution time and priority level.

Table 3. Function names and tasks of the PFC firmware

Function	Task	Execution frequency	Priority
ADC1_COMP_IRQHandler()	Current control loop Sinusoidal reference calc. Input voltage sign detection Average of last 3 current samples	20 kHz 60 kHz 60 kHz 60 kHz	High
TIM14_IRQHandler()	Voltage control loop Update control parameters	100 Hz	Medium
TIM6_DAC_IRQHandler()	Computing of Vac frequency and amplitude	2 kHz	Medium
main()	Fault checks State machine Serial communication LED		Low

After the initialization of the main peripherals such as system clock, ADC, DMA, timers, UART and I/O ports, which are executed in the main loop, the fault check function and serial communication tasks are performed. These tasks have lower priority level compared to those executed in specific interrupts.

As soon as the 500 W power supply is connected to the mains supply, the PFC is in idle state and a fault check routine is executed to ensure that no fault conditions are present. During this phase, the input voltage amplitude and frequency are calculated in order to verify that the mains parameters are within the converter specified operating window. In this case, the PM8834 gate driver, used to drive the two PFC MOSFETs, is enabled and the main PFC control algorithm is performed. A soft-start routine is first executed to linearly increase the DC bus voltage up to 400 V. When the soft-start is completed, the primary STM32F051K8 microcontroller sends the information of the correct PFC status to the secondary STM32F334x microcontroller, via serial communication. After having sent this information, the primary microcontroller starts the control loop routine, updating the control regulator parameters and enabling a second voltage ramp-up to increase the bus voltage to 430 V.

The algorithm for the computation of the input voltage amplitude and frequency is performed when the update event of timer 6 (TIM6) occurs (every 500 µs). The voltage control loop is executed every 10 ms when the update event of timer 14 (TIM14) occurs. Also, the calculation of new feed-forward duty cycle control parameters is triggered by the same event.

The current control loop is the highest priority task and is performed when the interrupt of the ADC end of conversions is triggered. All the acquisitions are synchronized with timer 1 (TIM1) which generates the output PWM signals (CH1 and CH2 of TIM1) as shown in *Figure 12*. A single sampling in single period technique is adopted.

Figure 12. Timer 1 utilization for PFC PWM generation and ADC conversion trigger

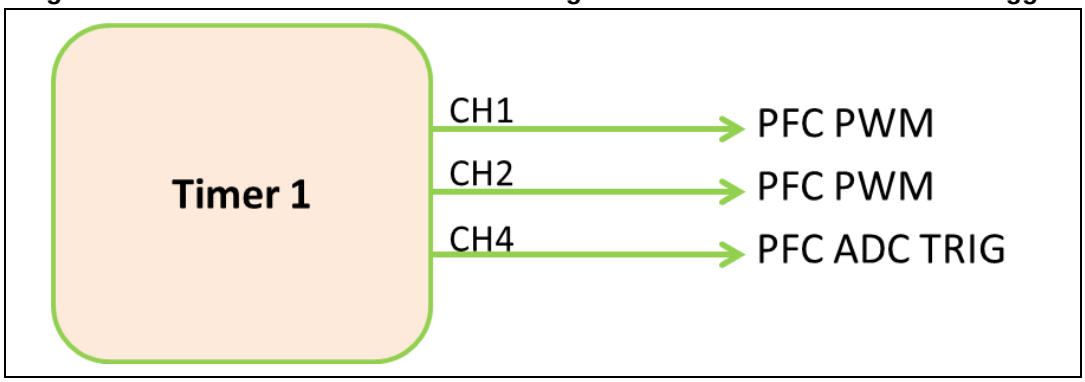
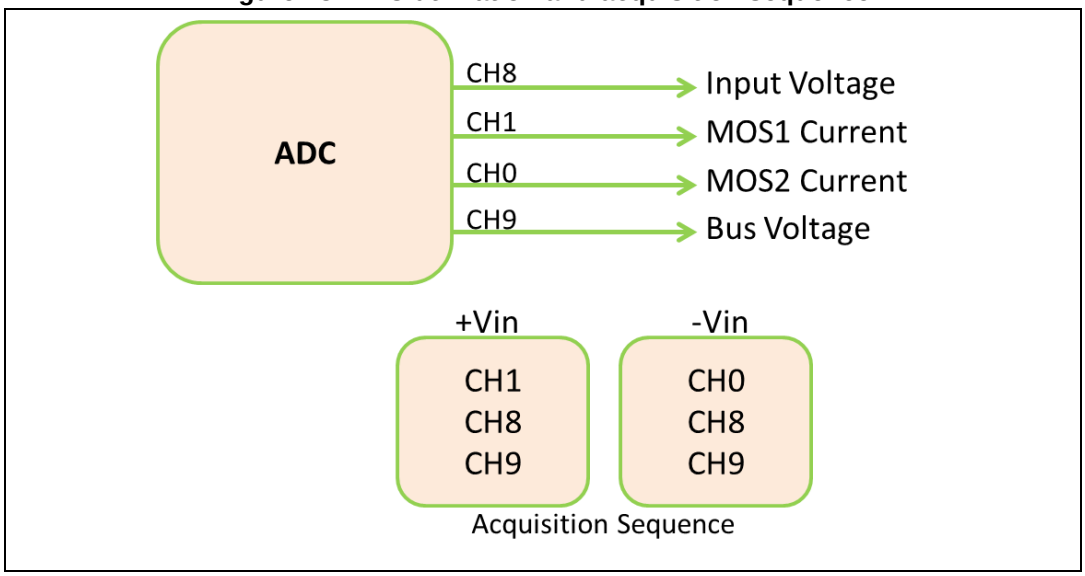


Figure 13. ADC utilization and acquisition sequence



The switch current is sensed at the midpoint of the PWM ON time which corresponds to the average inductor current in CCM. A sample correction algorithm can be implemented to take into account DCM operation. This is generally done, when necessary, to improve the input current THD. The ADC samples the MOSFET current first, either across MOS1 or MOS2, depending on the sign of input voltage sine waveform. Then, the input voltage is sampled and immediately after the output bus voltage is sampled. The acquired samples are then transferred into a buffer by DMA, keeping CPU resources free for other operations. The acquisition sequence (which depends on the sign of the input voltage) and ADC channels utilization is shown in *Figure 13*.

If a fault condition occurs, the PWMs are stopped, the PFC gate driver is disabled and a serial message is sent to the secondary side microcontroller in order to stop the LLC control algorithm.

Table 4 summarizes the resources required for the implementation of the digital control of the 500 W semi-bridgeless PFC.

Table 4. Microcontroller resources for PFC digital control implementation

Signal	Type	MCU resource	Resolution
Input voltage	Analog	ADC1 CH8	12 bit (1MSPS)
Output voltage	Analog	ADC1 CH9	12 bit (1MSPS)
MOS1 current	Analog	ADC1 CH1	12 bit (1MSPS)
MOS2 current	Analog	ADC1 CH0	12 bit (1MSPS)
ADC trigger	Digital	TIM1 CH4	
Gate drive 1	Digital	TIM1 CH1 (PWM1)	Dres=0.125% @ 60kHz
Gate drive 2	Digital	TIM2 CH2 (PWM2)	Dres=0.125% @ 60kHz
RS232-RX	Digital	UART1 (PB10)	
RS232-TX	Digital	UART1 (PB6)	
Temp. sense	Analog	ADC1 (CH6)	
LED	Digital	GPI/O (PB2)	
PM8831 enable/disable	Digital	GPI/O (PA12)	
L6491 enable/disable	Digital	GPI/O (PF1)	

3 LLC DC-DC converter design

The purpose of the DC-DC stage is to step the PFC output voltage down to 12 V. The topology used for this conversion stage, the LLC half-bridge, is shown in *Figure 14*. The power stage of the LLC converter is formed by the input and output capacitors C2 and C3, MOSFETs M3, M4, transformer T1 and resonant capacitor Cr. The resonant inductor Lr and the magnetizing inductor Lm depicted in *Figure 14* are integrated in the high frequency transformer. The output rectification stage is implemented with two MOSFETs, M5 and M6, used to exploit the advantages of synchronous rectification. The main advantages of the LLC topology are:

- ZVS at turn-on for the primary side switches
- ZCS at turn off for the secondary side switches
- Very good load regulation

The main drawback is the high sensitivity to input voltage variations which requires some design trade-offs to optimize the circuit in a wide input voltage range. The specifications used for this design are reported in *Table 5*.

Figure 14. Basic schematic of the LLC DC-DC converter

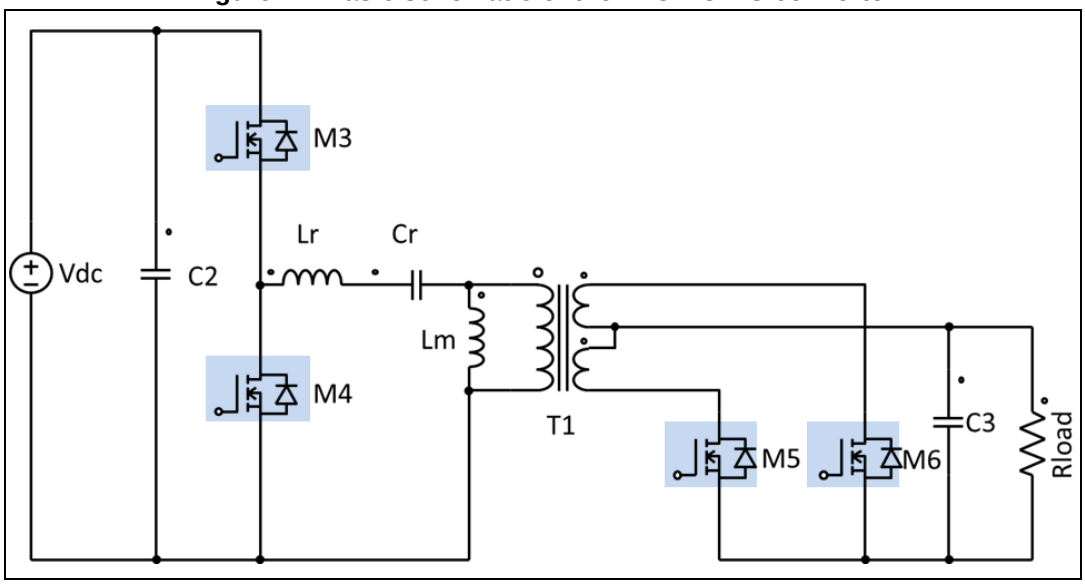


Table 5. Main specifications of the LLC converter

Parameter	Value
Input voltage	420 V
Minimum input voltage	400 V
Maximum input voltage	440 V
Nominal output voltage	12 V DC
Efficiency	>96%
Output power	500 W
Switching frequency	80 kHz @ full load, 420 V DC Input
Maximum switching frequency	90 kHz
Stray capacitance	350 pF
Dead time	350 ns

The voltage gain of the LLC converter resonant tank can be expressed as in equation 14.

Equation 14

$$M(f_n,\lambda,Q)=\frac{1}{\sqrt{\left(1+\lambda-\frac{\lambda}{f_n^2}\right)^2+Q^2\left(f_n-\frac{1}{f_n}\right)^2}}$$

where:

$\lambda=\frac{L_r}{L_m}$ is the ratio between the resonant tank inductance and the transformer magnetizing inductance;

$f_n=\frac{f_{sw}}{f_r}$ is the normalized frequency, ratio between the switching frequency and the resonant frequency;

$Q=\frac{1}{R_{ac}}\sqrt{\frac{L_r}{C_r}}$ is the quality factor;

$R_{ac}=\frac{8n^2V_{out}^2}{\pi^2P_{out}}$ is the equivalent load resistance.

Under no-load conditions (Q=0) equation 14 can be written as:

Equation 15

$$M_{OL}(f_n,\lambda)=\frac{1}{\left|\left(1+\lambda-\frac{\lambda}{f_n^2}\right)\right|}$$

In this operating condition a second resonant frequency can be defined:

Equation 16

$$f_0=\frac{1}{2\pi\sqrt{(L_m+L_r)C_r}}=f_r\cdot\sqrt{\frac{\lambda}{1+\lambda}}$$

Or in normalized form

Equation 17

$$f_{n,0} = \frac{f_0}{f_r} = \sqrt{\frac{\lambda}{1+\lambda}}$$

In fact, in no-load conditions (the rectifier is not conducting) the total primary inductance (magnetizing plus leakage inductance) resonates with the capacitor. At this frequency the no-load gain characteristic tends to infinity.

For an infinite value of the normalized frequency the no-load gain M_{OL} tends to M_∞:

Equation 18

$$M_\infty = \frac{1}{1+\lambda}$$

The design steps are summarized in the following part of this document:

- Transformer turns ratio:

  This is calculated assuming that the required gain at nominal input voltage is unitary:

Equation 19

$$M_{nom} = 2n\frac{V_{out}}{V_{in\_nom}} = 1 \quad \rightarrow \quad n = \frac{V_{in\_nom}}{2V_{out}} = \frac{420}{2 \cdot 12} = 17.5$$

The transformer turns ratio has been chosen equal to 18.

- Calculation of minimum and maximum voltage gain (assuming 5% margin):

Equation 20

$$M_{min} = 2n\frac{V_{out}}{V_{in\_max}} \cdot 0.9 = 2 \cdot 18 \cdot \frac{12}{440} \cdot 0.95 = 0.93$$

$$M_{max} = 2n\frac{V_{out}}{V_{in\_min}} \cdot 1.1 = 2 \cdot 18 \cdot \frac{12}{400} \cdot 1.05 = 1.13$$

- Maximum input current

Equation 21

$$I_{in\_max} = \frac{P_{out}}{0.96 \cdot V_{in\_min}} = 1.3\ A$$

- Equivalent load resistance

Equation 22

$$R_{ac} = \frac{8 \cdot n^2 \cdot V_{out}^2}{\pi^2 \cdot P_{out}} = 75.71\Omega$$

- Calculation of maximum normalized operating frequency:

Equation 23

$$f_{n,max} = \frac{f_{max}}{f_r} = 1.125$$

- Inductance ratio:

Equation 24

$$\lambda = \frac{L_r}{L_m} = \frac{1-M_{min}}{M_{min}} \cdot \frac{f_{n,max}^2}{f_{n,max}^2-1} = 0.34$$

- Calculation of the maximum value of Q to operate in ZVS at full load and minimum input voltage

Equation 25

$$Q_{ZVS1} = \frac{\lambda}{M_{max}} \cdot \sqrt{\frac{1}{\lambda} + \frac{M_{max}^2}{M_{max}^2-1}} = 0.82 \quad \rightarrow choose\ Q_{ZVS1} = 0.8$$

- Calculation of the maximum Q value to work in the ZVS with no-load condition and maximum input voltage:

Equation 26

$$Q_{ZVS2} = \frac{2}{\pi} \cdot \frac{\lambda \cdot f_{n,max}}{(\lambda+1) \cdot f_{n,max}^2} \cdot \frac{t_d}{R_{ac} \cdot C_{ZVS}} = 3.2$$

$$Q_{ZVS} \leq min(Q_{ZVS1}, Q_{ZVS2})$$

The value of Q_{ZVS} is chosen equal to Q_{ZVS1}.

- Calculation of resonant tank components:

Equation 27

$$Z_0 = Q_{ZVS} \cdot R_{ac} = 62.4\Omega$$

$$C_r = \frac{1}{2 \cdot \pi \cdot f_r \cdot Z_0} = 31.8nF$$

$$L_r = \frac{Z_0}{2 \cdot \pi \cdot f_r} = 124.2uH$$

$$L_m = \frac{L_r}{\lambda} = 361uH$$

- Resonant Tank

The selected values differ from the calculations as a result of the efficiency optimization process done at an input voltage of 430 V DC (selected output PFC voltage). The resonant tank values are:

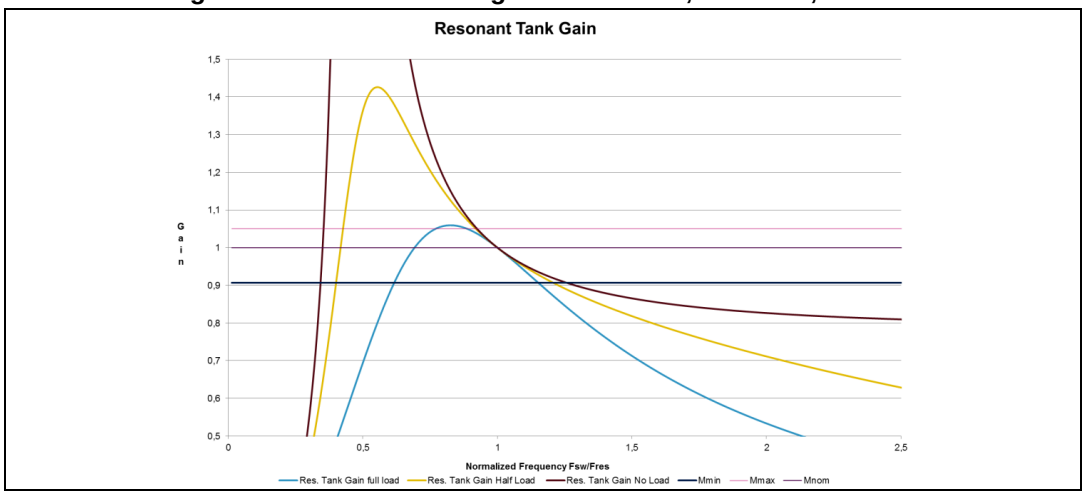
C_r=30 nF

L_r=140 uH

L_m=500 uH

The transformer has been designed to integrate both the series inductance Lr and the magnetizing inductance Lm. The resonant capacitance is realized by parallel connection of two 15 nF, 1 kV polypropylene capacitors. With the values reported above, the resulting resonant tank gain is depicted in *Figure 15*.

Figure 15. Resonant tank gain at full load, half load, no load



The frequency at full load and 430 V DC input is 77.7 kHz. The minimum operating frequency at full load and minimum input voltage is 68.3 kHz. The maximum operating frequency is obtained with no load and maximum input voltage and is equal to 96.3 kHz.

- Half-bridge MOSFETs selection:

The power MOSFETs used on the primary side of the LLC converter have 600 V breakdown voltage and drain current of 6.9 A at 100 °C case temperature and 0.38 Ω maximum drain-to-source resistance.

The part number of this device is STP13NM60ND. It is characterized by intrinsic fast-recovery body diode produced using the second generation MDmesh™ technology. This ensures very low on-resistance and optimal switching performance making them ideal for this application.

The breakdown voltage is selected considering the following equation:

Equation 28

$$V_{br} \geq 1.2V_{in\_max} = 540V$$

where 20% derating is considered.

- SR MOSFETs selection:

The power MOSFETs used on the secondary side for synchronous rectification are characterized by 30 V breakdown voltage and 32 A drain current at 100 °C PCB temperature. They feature extremely low drain-to-source resistance, ideal to keep secondary side conduction losses low thanks to the 7th generation of STripFET™ DeepGATE™ technology. The part number is STL160N3LLH6 which is packaged in a Power Flat 5X6. Two of these devices are parallel-connected on each side of the rectifier circuit in order to minimize conduction losses.

The LLC converter parameters resulting from the design are summarized in *Table 6*.

Table 6. LLC converter parameters

Parameter	Value
Magnetizing inductance	500 uH
Resonant inductance	140 uH
Transformer turns ratio	18
Resonant capacitor	30 nF
Resonant frequency	77.7 kHz
Maximum switching frequency	96.3 kHz
Minimum switching frequency	68.3 kHz
Input voltage operating range	400 V to 440 V
Output voltage	12 V
Primary side MOSFETs	STP13NM60ND
SR MOSFETs	STL160N3LLH6

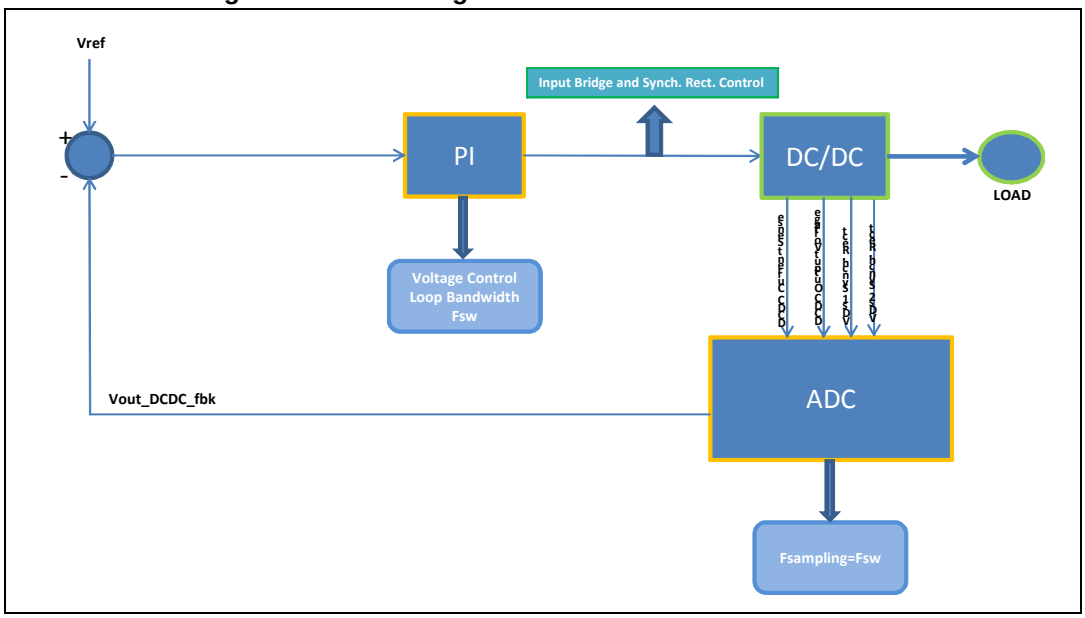
3.1 LLC converter firmware overview and control algorithm

The LLC firmware is implemented on the secondary side MCU which is the STM32F334x, a 32-bit microcontroller from the STM32 family. The control strategy generates the gate signals for both primary and secondary side MOSFETs in order to ensure precise output voltage regulation at 12 V DC.

The secondary side MOSFETs are used to reduce the conduction losses produced by standard output rectifier diodes. The SR MOSFETs are properly controlled by the MCU implementing a synchronous rectification control strategy which improves the efficiency and compensates for delays caused by hardware components and parasitic elements.

The block diagram of the control scheme is shown in *Figure 14*.

Figure 16. Block diagram of the LCC converter control



A simple voltage control loop, based on the use of a PI regulator whose input is the error between the reference voltage and LLC converter output voltage, is adopted.

The STM32F334x high resolution timer HRTIM generates the driving signal pattern to control the primary and secondary MOSFETs. The HRTIM is specifically designed to drive power conversion systems. It is characterized by a modular architecture and can generate up to ten digital signals with either independent or coupled waveforms.

The HRTIM has timing measure capabilities and links to built-in ADC and DAC converters. It features light load management mode and is able to handle various fault schemes for safe shutdown purposes. The HRTIM can be partitioned into several sub modules:

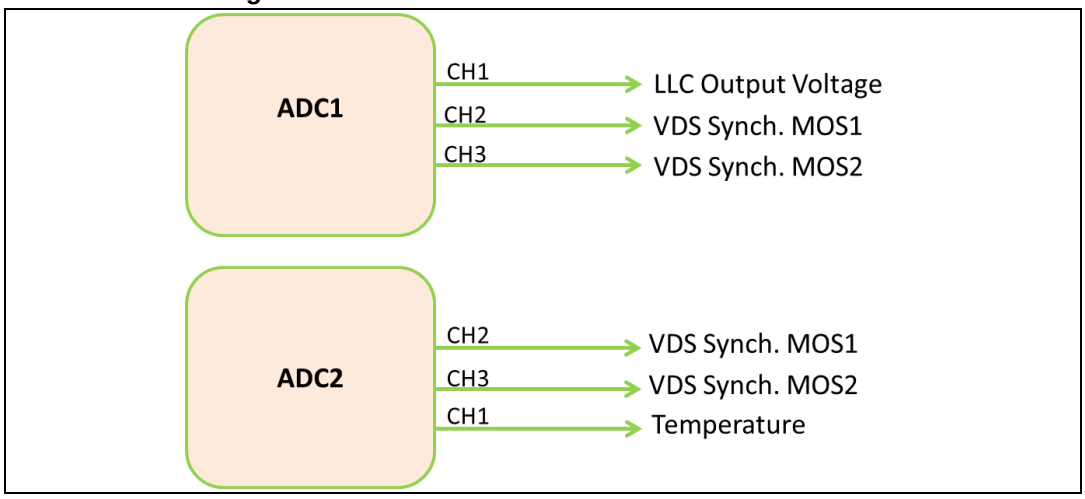
- The master timer
- The timing units (timer A to timer E)
- The output stage
- The burst mode controller
- An external event and fault signal conditioning logic
- The system interface

The HRTIM is configured as follows to drive the LLC stage with synchronous rectification:

  – The master timer is used for synchronization of Timer A, C and D
  – Timer C is used for primary half-bridge modulation
  – Timer A and Timer D are used for secondary synchronous rectification
  – Timer C is configured in half mode and drives two complimentary outputs CHC1 and CHC2 with 50% duty cycle and a suitable dead time.

Timer A output CHA1 and Timer D output CHD1 are used to generate the two synchronous rectification MOSFET modulation signals. The ON and OFF time of each driving signal generated by Timer A and Timer D is dynamically adjusted and depends on the drain-to-source voltage of the synchronous rectification MOSFETs. These voltages are acquired by two 5 MHz ADC converters, namely ADC1 and ADC2. The utilization of the two A/D converters is shown in *Figure 17*.

Figure 17. STM32F334x ADC1 and ADC2 utilization



The hardware is configured to acquire some other measurements such as heatsink temperature, auxiliary power supply output voltage, LLC transformer primary current and its average value.

ADC1 CH1 acquisition is triggered by the update event of the master timer, while CH2 and CH3 acquisitions are triggered by either timer A or timer C compare events. Similarly, ADC2 CH2 and CH3 are triggered by either timer C or timer D compare events. The injected acquisition sequence and trigger events are shown in *Figure 18* while the HRTIM timing configuration is shown in *Figure 19*.

Figure 18. ADC1 and ADC2 injected acquisition sequence and trigger events

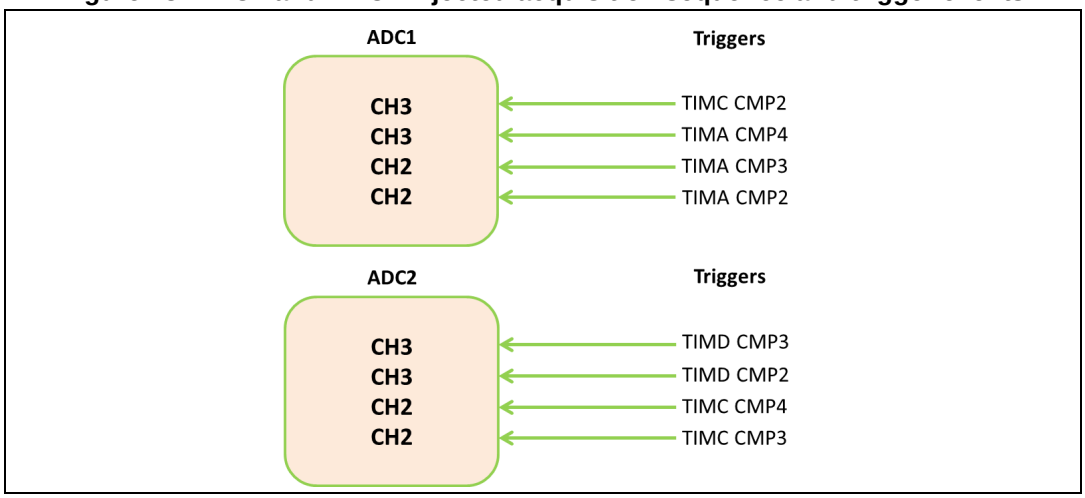
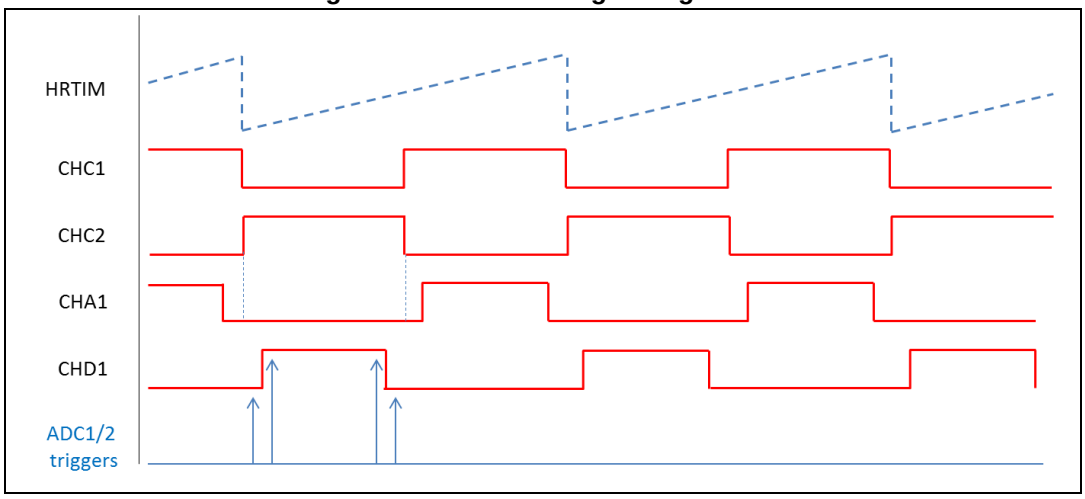


Figure 19. HRTIM timing configuration



The voltage control loop consists of a standard PI regulator and is executed at the update event of the master timer. The regulator output is the new value of the primary MOSFET driving signal period in terms of number of clock cycles (new value of HRTIM_MPER register). In this way, the frequency can vary from 70.3 kHz up to 130 kHz, while the duty cycle is fixed at 50%. Together with the period, the new rising and falling edges of the SR signals are calculated. The calculation includes a blanking time to take into account the opto-isolator delay and the delay due to the sampling and acquisition of SR MOSFETs drain-to-source voltage.

The SR control algorithm tries to maintain the two drain-to-source voltage ADC samples (each drain-to-source voltage is sensed twice) under/above a reference value to detect the correct turn-on and turn-off of SR MOSFETs. If the first and second samples are not under/above the preset reference value, the on-time is made longer or shorter.

The LLC converter firmware structure and its main tasks are highlighted in *Figure 20* and,*Table 7* respectively.

Figure 20. LLC firmware structure overview

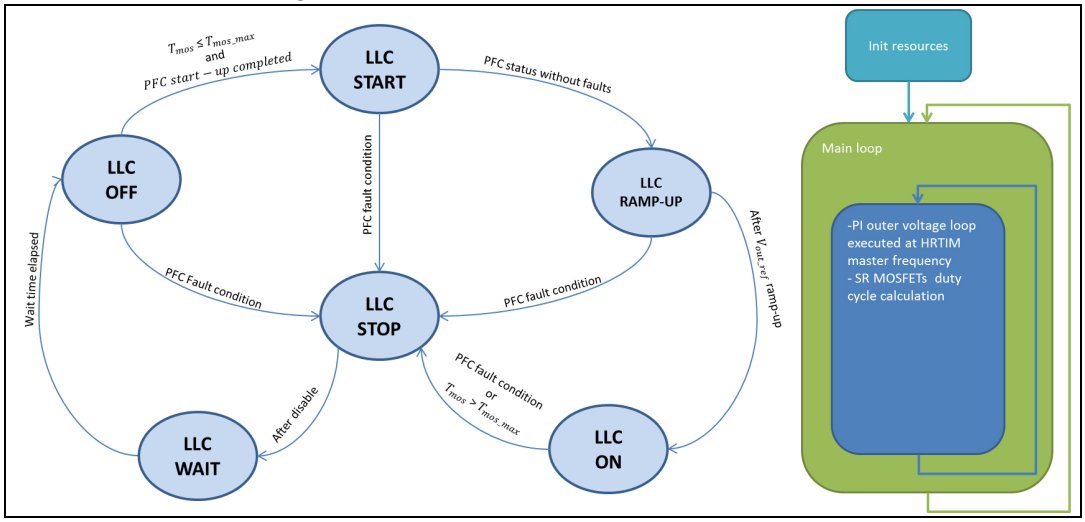


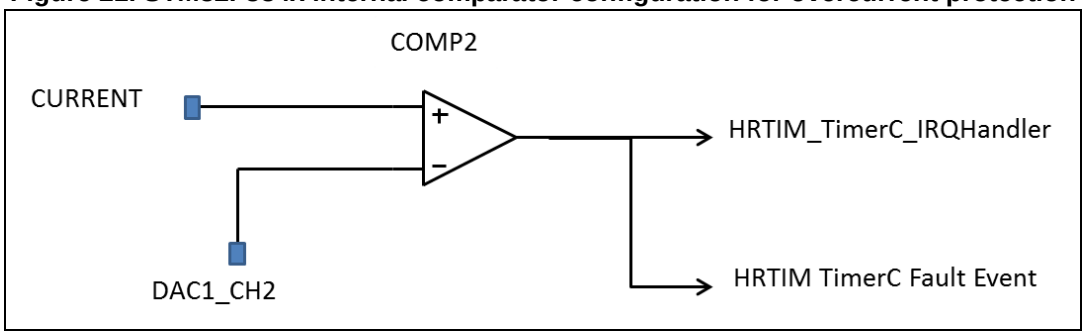
Table 7. LLC firmware tasks

Function	Task	Execution frequency	Priority
HRTIM_MASTER_IRQHandler()	Voltage control loop Synchronous rectification Burst mode	HRTIM master frequency	Medium
HRTIM_TimerC_IRQHandler()	Output short-circuit protection	Comparator trigger	High
USART1_IRQHandler()	Acquisition of PFC status	On acquisition	Low
main()	State machine LED Serial communication Temperature check		Low

The STM32F334xx devices embed 3 comparators that can be used either as standalone devices (all terminals are available on I/Os) or combined with the timers. They can be used for a variety of functions such as wakeup from low-power mode triggered by an analog signal, analog signal conditioning and cycle-by-cycle current control loop when combined with the DAC and a PWM output from a timer.

In this design an internal comparator is used to implement the output overcurrent protection. The configuration is shown in *Figure 21* where the inverting pin of the microcontroller internal comparator COMP2 is connected to CH1 of DAC1 and the non-inverting pin is connected to the output of the current sense circuit used to measure the LLC converter primary current.

Figure 21. STM32F334x internal comparator configuration for overcurrent protection



When the sensed current is higher than the preset threshold, a fault event is generated to set the Timer C output channels in idle state. In addition, the HRTIM Timer C interrupt is generated to set the state machine in LCC_STOP state. After such an event, the state is updated to LLC_WAIT and, after this, the new state is LLC_OFF. If no faults are detected the LLC converter can be started again after the PFC bus voltage ramp-up.

Burst mode operation is implemented for light load management. The main purpose is to increase the efficiency of the converter by reducing the number of transitions on the outputs and the associated switching losses. The STM32F334C8 burst mode controller allows having the outputs alternatively in IDLE and RUN state, by hardware, so that some switching periods are skipped with a programmable periodicity and duty cycle.

The burst mode operation is enabled when the output of the voltage control PI regulator is lower than a predefined threshold (switching period) corresponding to a switching frequency of 115 kHz. Similarly, it is disabled when the PI regulator output is greater than a threshold corresponding to 110 kHz. In this way, the output voltage is regulated at 12 V ± 100 mV during no-load and light load operation.

4 Experimental characterization

This section includes the validation results of the 500 W digital power supply design. It includes the efficiency and power quality test results at different input voltage values and the main waveforms of the two converters.

The power supply efficiency measured at different mains voltages, namely 120 V AC and 230 V AC., is shown in *Table 8* and *Table 9*.

The efficiency was measured in the following conditions:

1. The board was operated at half load for 30 minutes.
2. The efficiency results were taken in the following output load points: 6 A, 12 A, 18 A, 24 A, 28 A, 34 A, 42 A.
3. The input and output voltages were measured directly at the input and output connectors of the board.
4. All the measurements were taken using the Voltech PM6000 Universal Power Analyzer
5. The power measurements do not take into account the power consumption of the fan which will be activated above 300 W.
6. The board was tested with open frame at an ambient temperature of 25 °C.

Table 8. Efficiency measurements at 120 V AC input

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
120	0.712	82.6	12.07	6	72.76	88.08
120	1.33	157.98	12.03	12	144.58	91.51
120	1.96	234.01	12.01	18	216.49	92.51
120	2.61	312,34	12.02	24	288.74	92.44
120	3.05	365.2	12,03	28	337.48	92.40
120	3.72	445.24	11.99	34	409.37	91.94
120	4.63	554.2	12.01	42	505.69	91.24

Table 9. Efficiency measurements at 230 V AC input

V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (A)	P_{OUT} (W)	Efficiency (%)
230	0.45	81.71	12.1	6	72.62	88.87
230	0.73	156.37	12.04	12	144.47	92.38
230	1.04	232.65	12.01	18	216.56	93.08
230	1.37	309.26	12.04	24	288.63	93.32
230	1.59	360.98	12.03	28	336.62	93.25
230	1.94	441.15	11.99	34	410.26	92.99
230	2.40	546.81	12.01	42	505.5	92.44

The peak efficiency is obtained at 230 V AC input is equal to 93.2%. For 120 V AC input the peak efficiency is reduced to 92% due to higher input to output voltage ratio.

Table 10 and *Table 11* report the measurement of current THD% and power factor both at 120 V and 230 V AC input voltage. It can be noted that the total harmonic distortion is still low even for high input voltage values. The power factor is close to unity for both low and high input voltage values.

Table 10. DSMPS power factor and current THD% at 120 V AC input

Output load at 120 V AC	PF	THD%
6 A	0.965	5.4
12 A	0.984	5.4
18 A	0.992	4.2
24 A	0.994	3.5
28 A	0.996	3.2
34 A	0.996	3.2
42 A	0.997	4.3

Table 11. DSMPS power factor and current THD% at 230 V AC input

Output load at 230 V AC	PF	THD%
6 A	0.78	13.6
12 A	0.925	11.4
18 A	0.964	9.7
24 A	0.977	8.9
28 A	0.983	7.9
34 A	0.986	7.6
42 A	0.989	7.4

Figure 22. PFC inductor current at 120 V input, full load

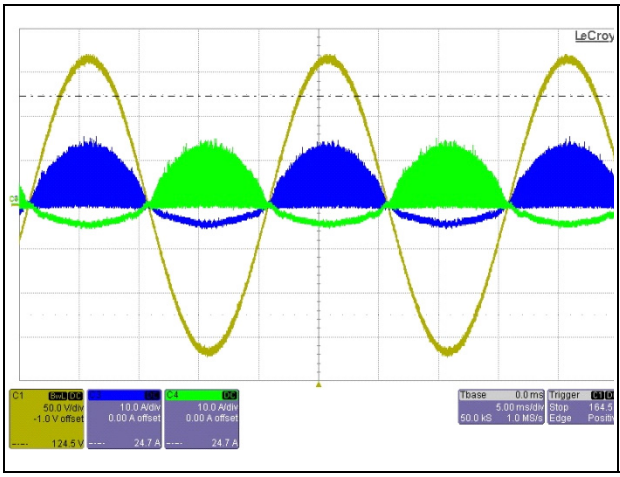
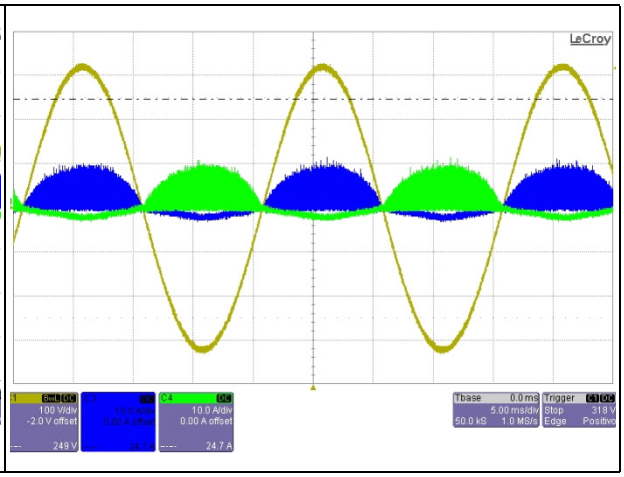


Figure 23. PFC inductor current at 230 V input, full load



The PFC inductor currents are shown together with the input voltage in *Figure 22* and *Figure 23*. It is possible to highlight that only one branch of the bridgeless PFC circuit is switching during each half period of the input voltage.

The PFC efficiency in the whole operating range is highlighted in *Figure 24* and is as high as 98%. The power factor for 120 V and 230 V AC input is depicted in *Figure 25* for an output load varying form 70 W up to 500 W. In this operating range the power factor is always higher than 0.9.

Figure 24. PFC circuit efficiency

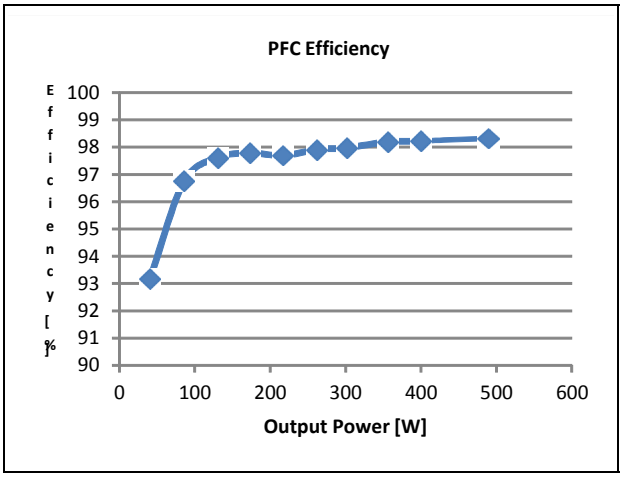


Figure 25. PFC input current power factor

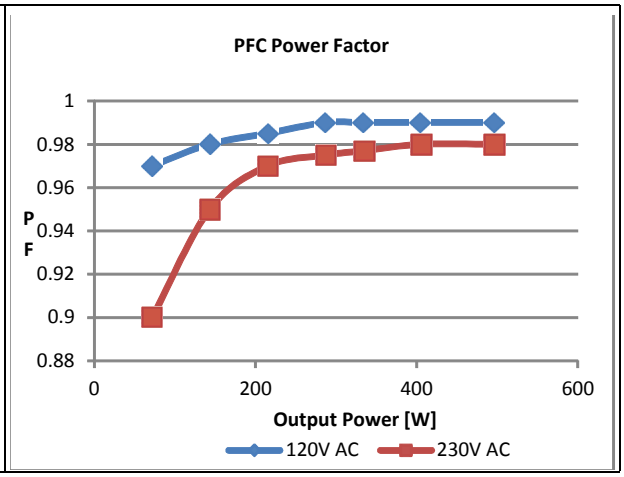


Figure 26. PFC inductor L2 (blue) and L1 (green) current and MOSFET Q1 drain voltage (purple) at 120 V, 60 Hz input, full load

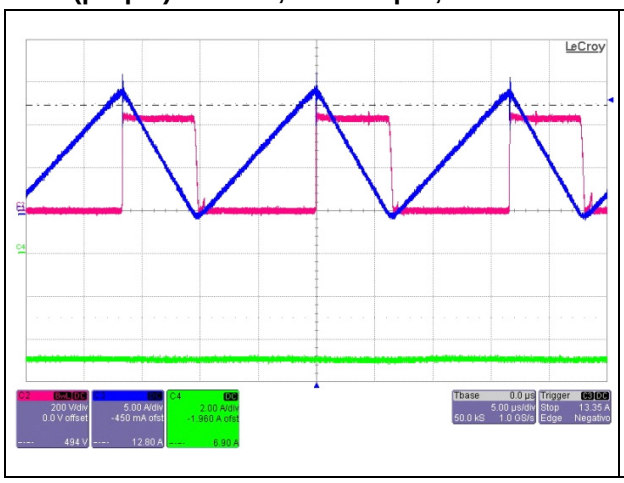


Figure 27. PFC inductor L1 (green) L2 (blue) and current and MOSFET Q2 drain voltage (purple) at 120 V, 60 Hz input, full load

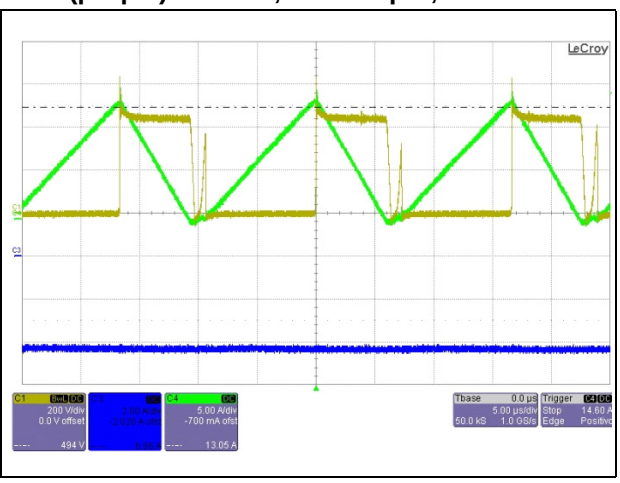


Figure 26 and *Figure 27* show the inductor currents and PFC MOSFETs drain-to-source voltage at full load for 120 V operation. *Figure 28* and *Figure 29* show the same waveforms for 230 V operation. In both cases the PFC is operating in DCM.

The LLC converter main switching waveforms are shown in *Figure 30* and *Figure 31* for full load and no-load operation, respectively. The MOSFET current is negative before the device is turned on thus providing zero voltage switching.

The switching frequency at full load and nominal input voltage is 77 kHz while during no-load operation the burst mode is enabled and the switching frequency can vary in the 115-130 kHz range. The operating switching frequency for different load currents is reported in *Figure 32*, while *Figure 33* shows the LLC converter efficiency in whole operating range at nominal input voltage.

Figure 28. PFC inductor L2 (blue) and L1 (green) current and MOSFET Q1 drain voltage (purple) at 230 V, 50 Hz input, full load

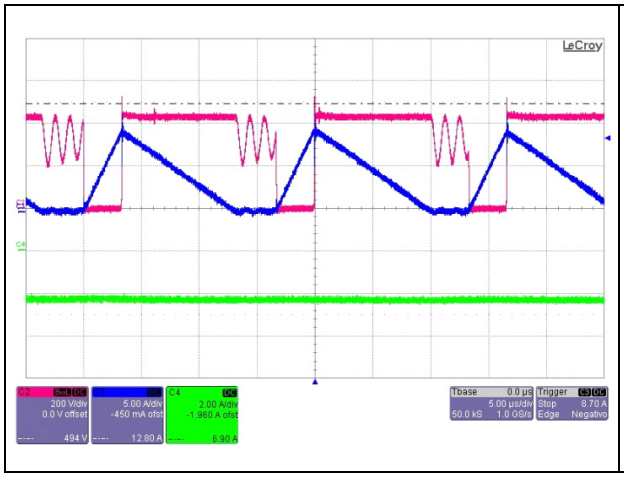


Figure 29. PFC inductor L1 (green) L2 (blue) and current and MOSFET Q2 drain voltage (purple) at 230 V, 50 Hz input, full load

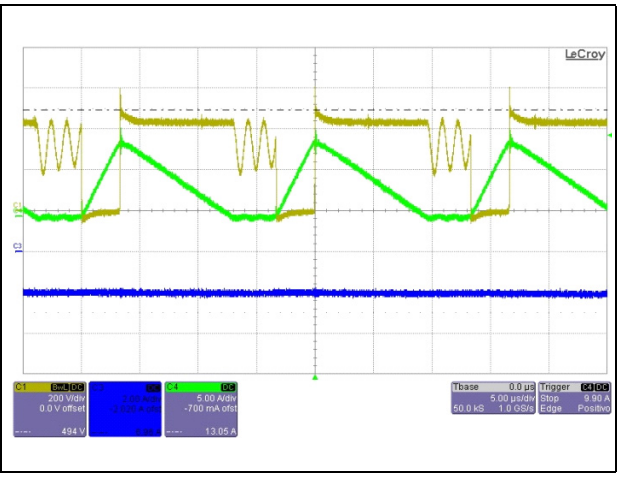


Figure 30. LLC converter, MOSFET Q12 Gate signal (yellow), drain current (blue), drain voltage (purple) at full load (42 A output)

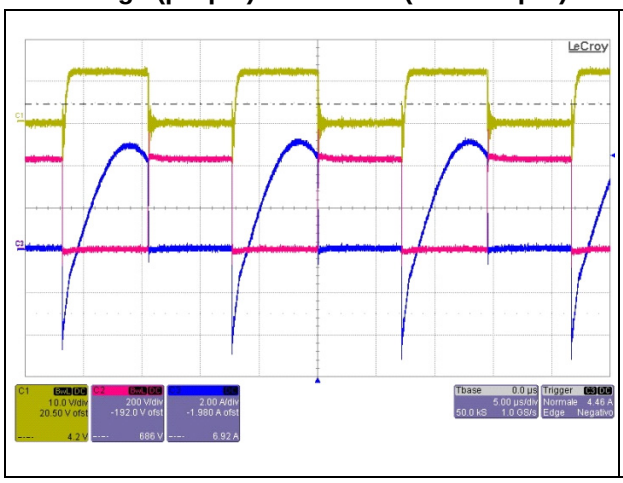


Figure 31. LLC converter, MOSFET Q12 Gate signal (yellow), drain current (blue), drain voltage (purple) at no load

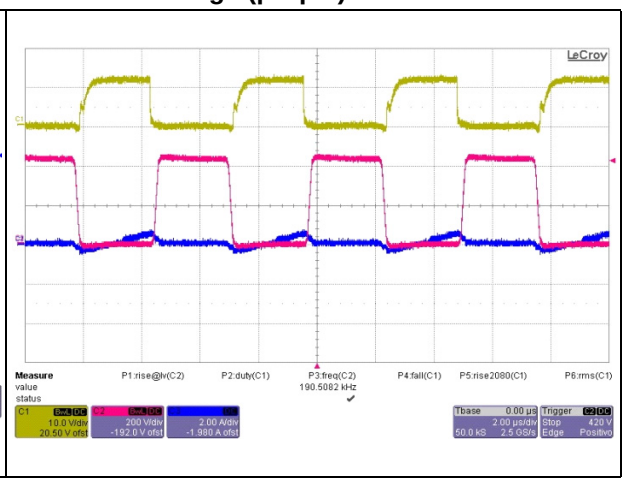


Figure 32. LLC switching frequency vs. output current

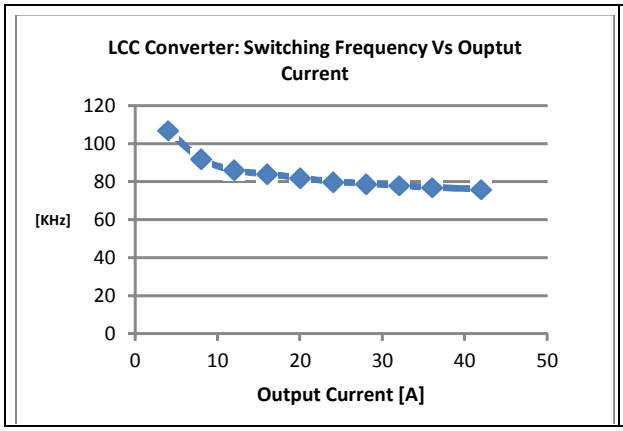
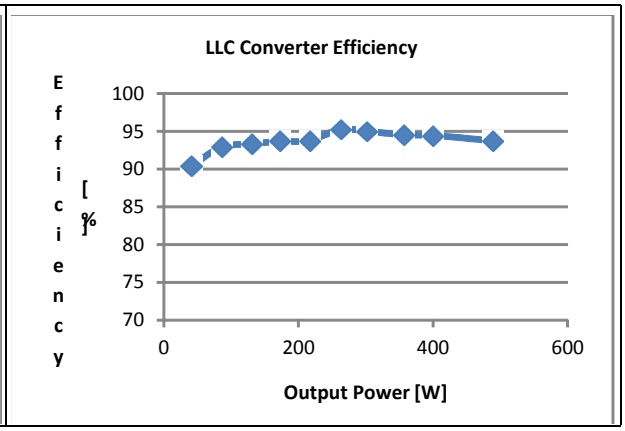


Figure 33. LLC converter efficiency



The impact on the power supply regulated 12 V output voltage when the load is increased from 10% to 90% of the nominal value is shown in *Figure 34*, *Figure 35* and *Figure 36*. In every case the output voltage is tightly regulated and the steady state operation is restored in less than 5 ms.

Figure 34. Load transition from 10% to 90% max load (max load=42 A) with 120 V, 60 Hz AC input

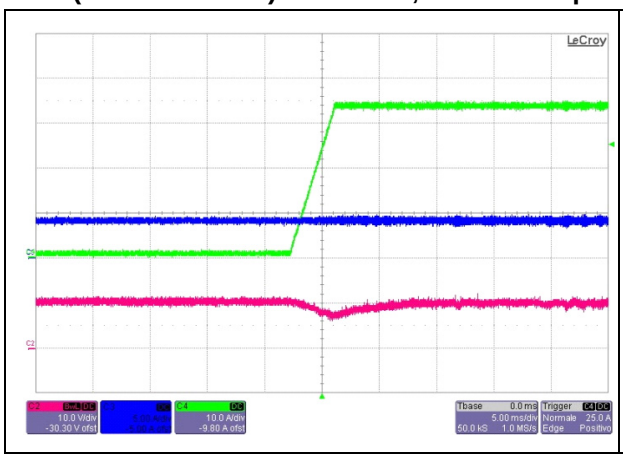


Figure 35. Load transition from 90% to 10% max load (max load=42 A) with 120 V, 60 Hz AC input

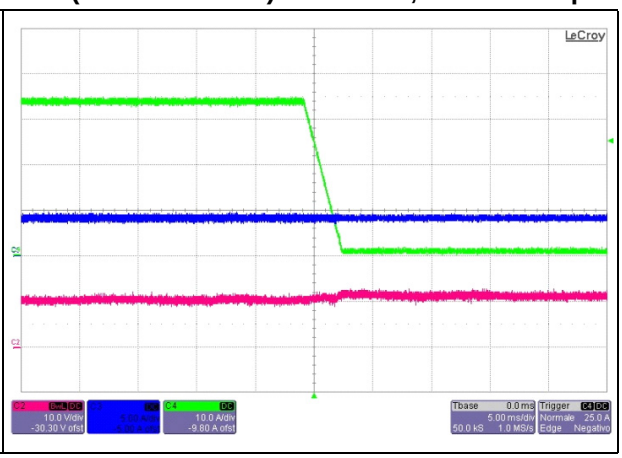


Figure 36. Repetitive dynamic load variation 10% to 90% max load

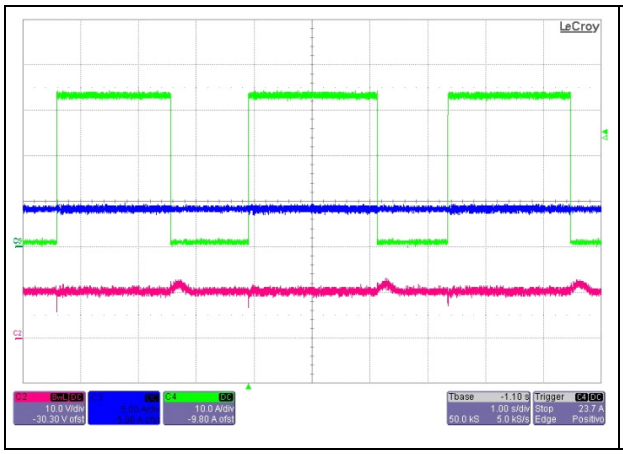
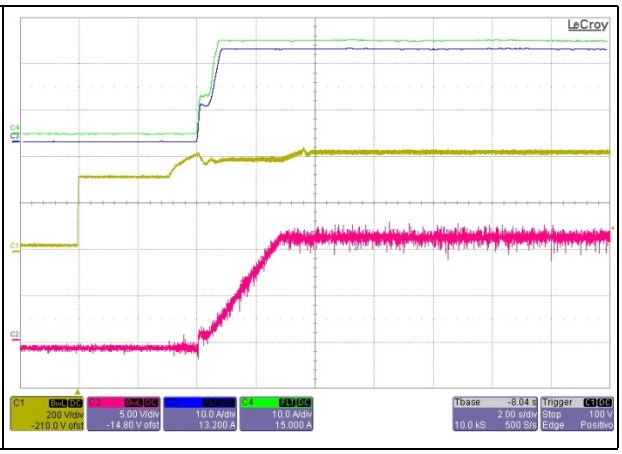


Figure 37. Startup at full load (42 A), 230 V, 50 Hz input voltage; PFC bus voltage (yellow), 12 V output (purple); output current (green and blue)



The typical converter waveforms at startup are shown in *Figure 37*. The bus DC voltage is initially regulated at 400 V. As soon as the output current has reached the steady state value, the bus DC voltage is increased to 430 V.

Figure 38. Input current waveform at full load, 120 V AC input

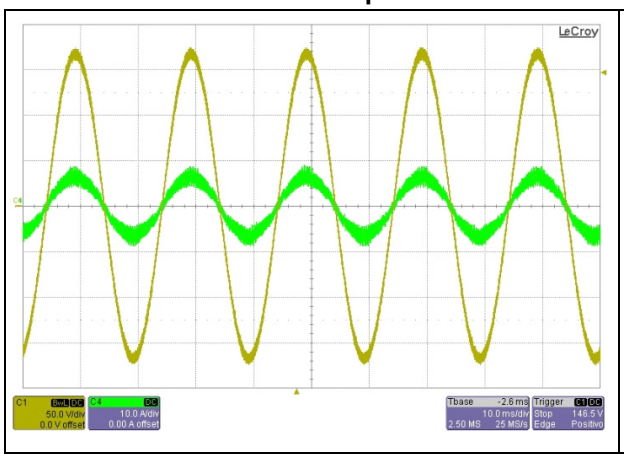
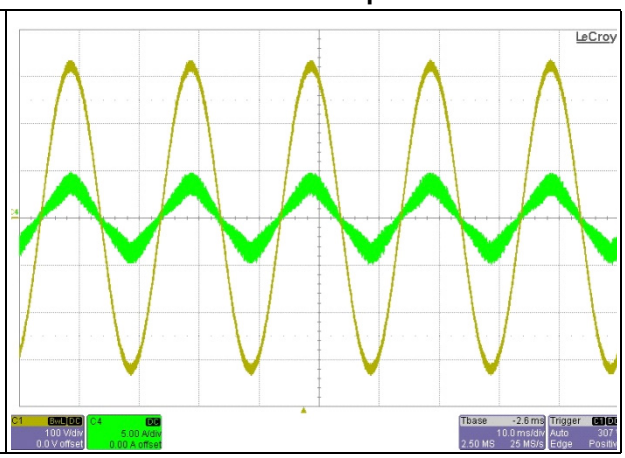


Figure 39. Input current waveform at full load, 230 V AC input



Finally, *Figure 38* and *Figure 39* show the input current waveforms at 120 V and 230 V AC input at full load.

Appendix A Schematic diagrams

Figure 40. Schematic diagram (1 of 6)

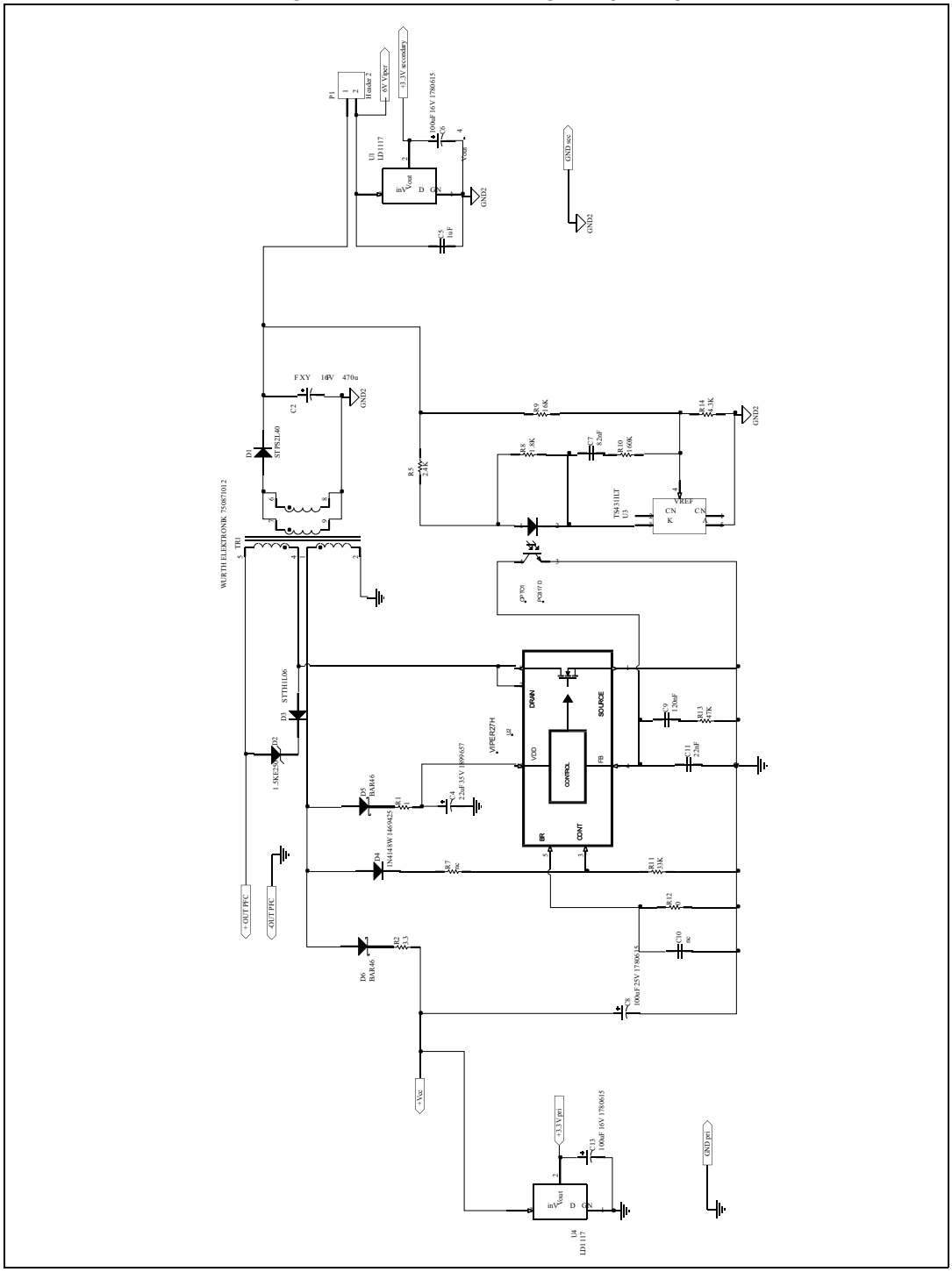


Figure 41. Schematic diagram (2 of 6)

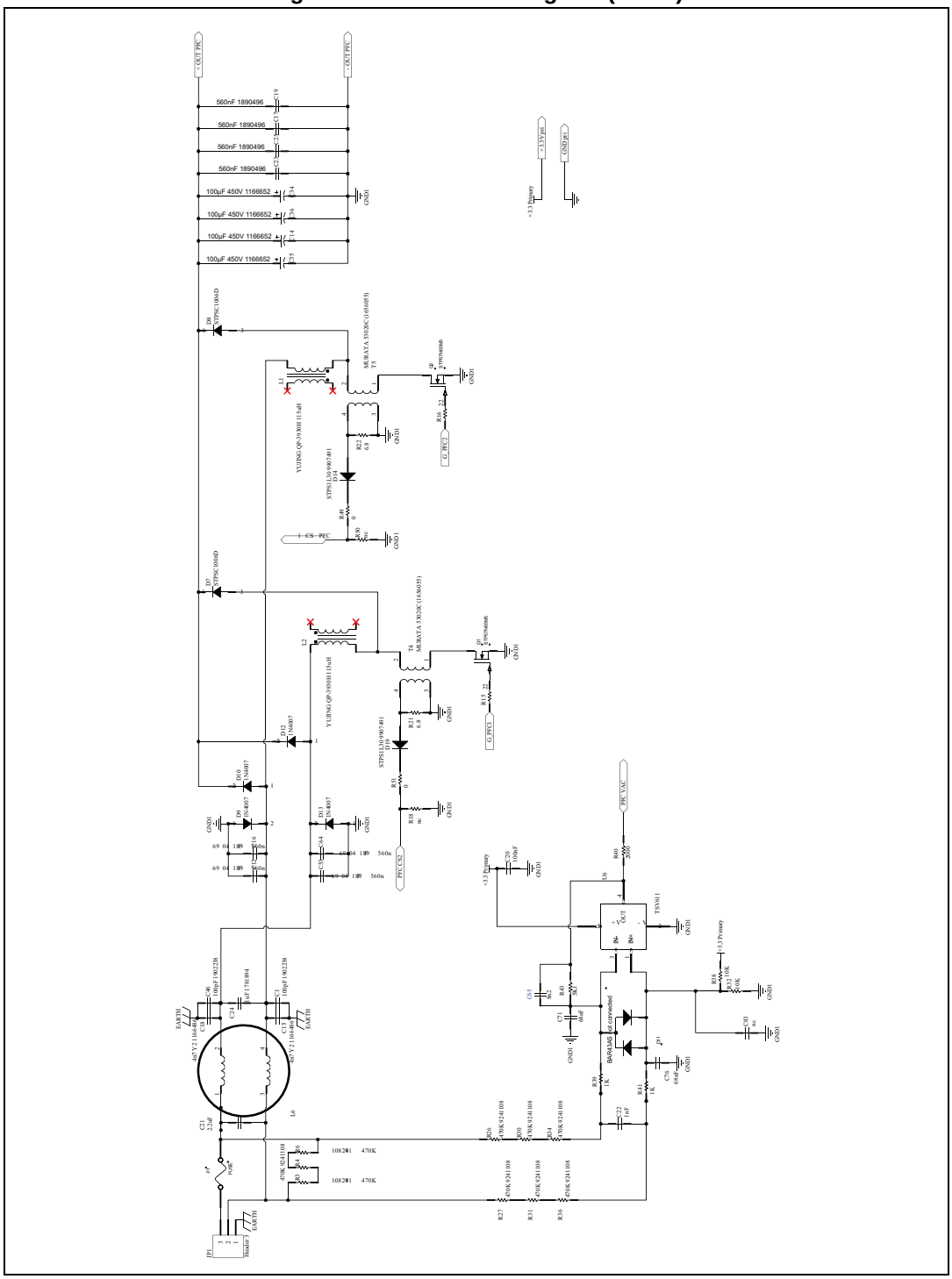


Figure 42. Schematic diagram (3 of 6)

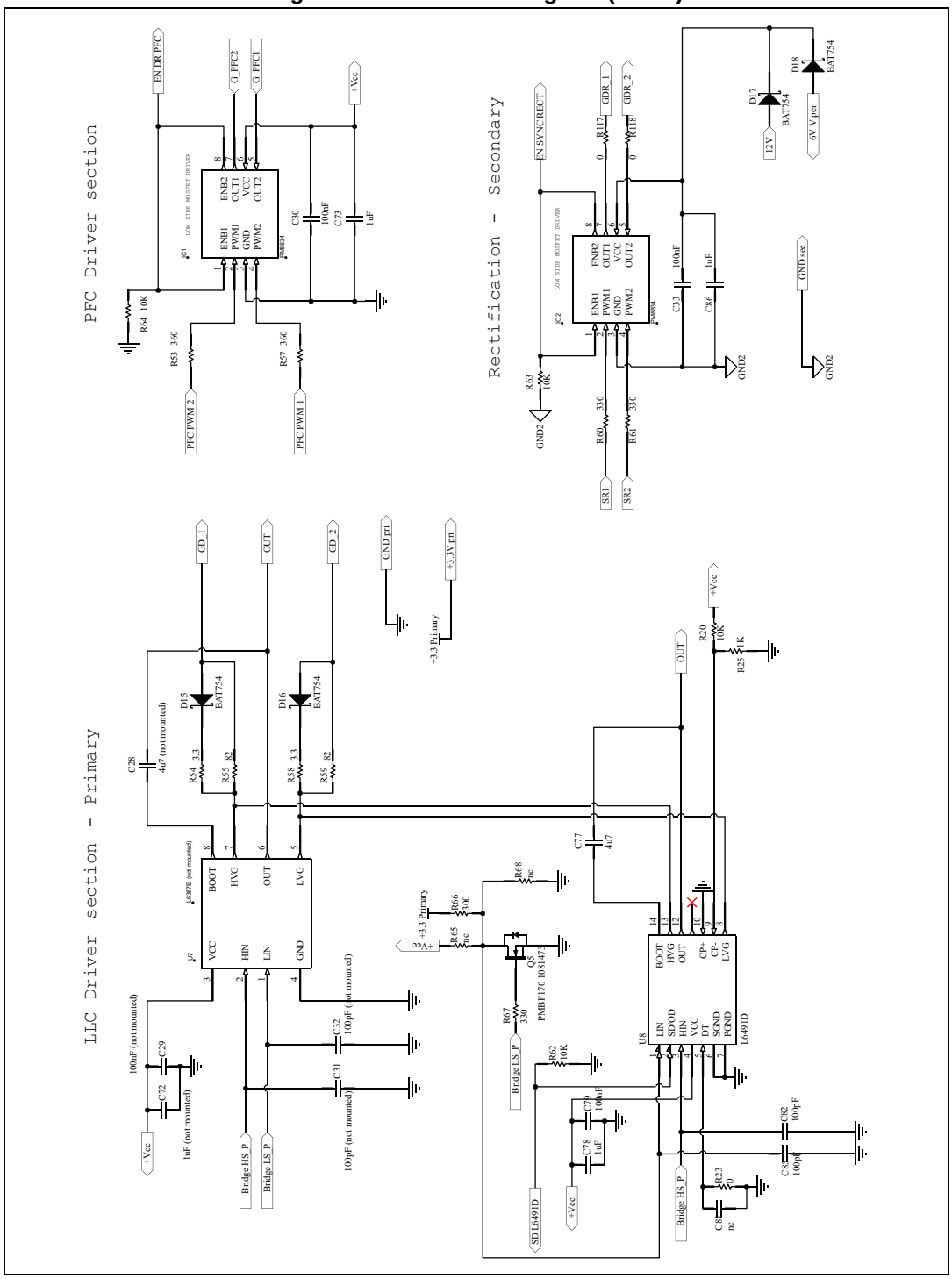


Figure 43. Schematic diagram (4 of 6)

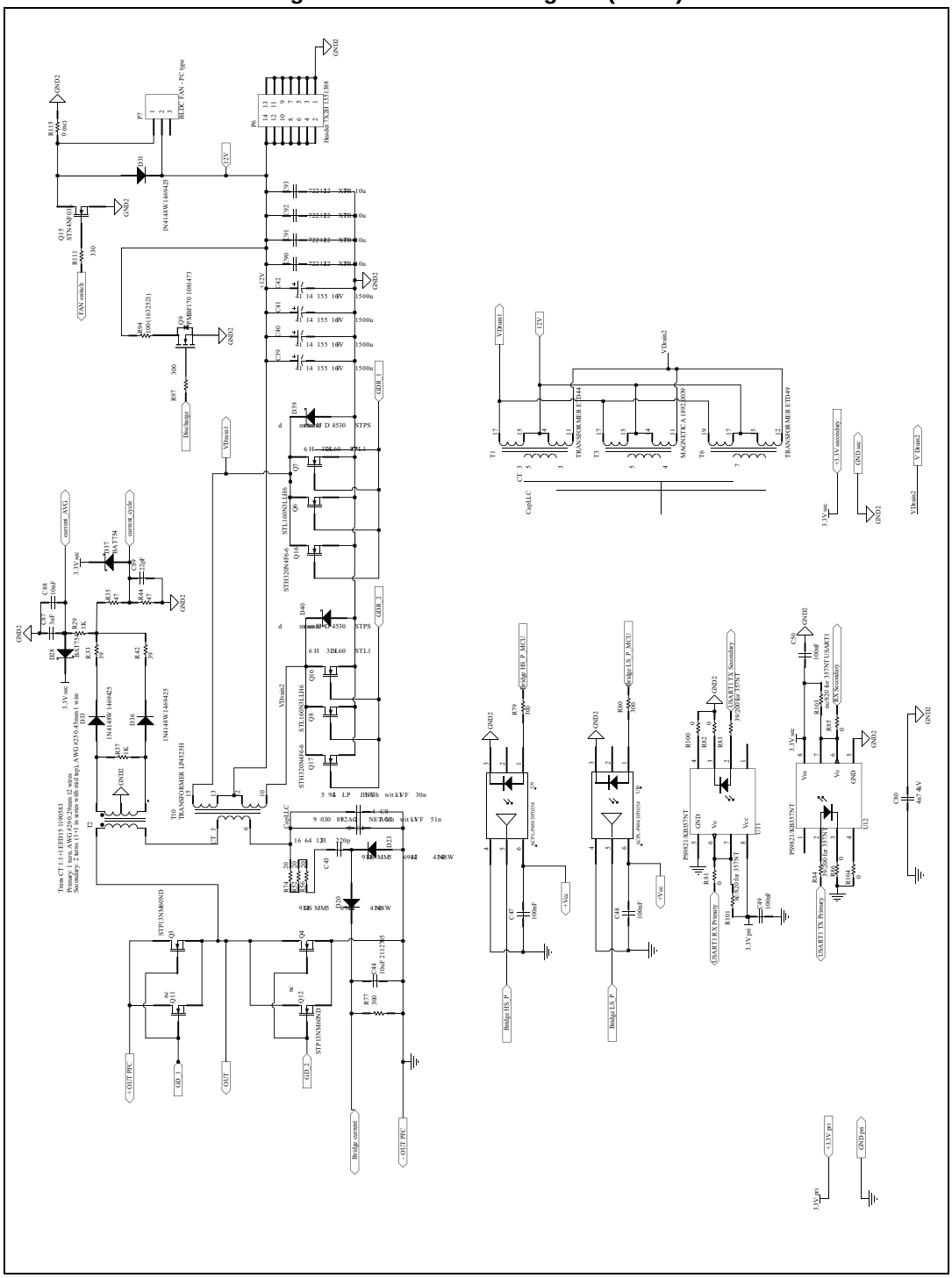


Figure 44. Schematic diagram (5 of 6)

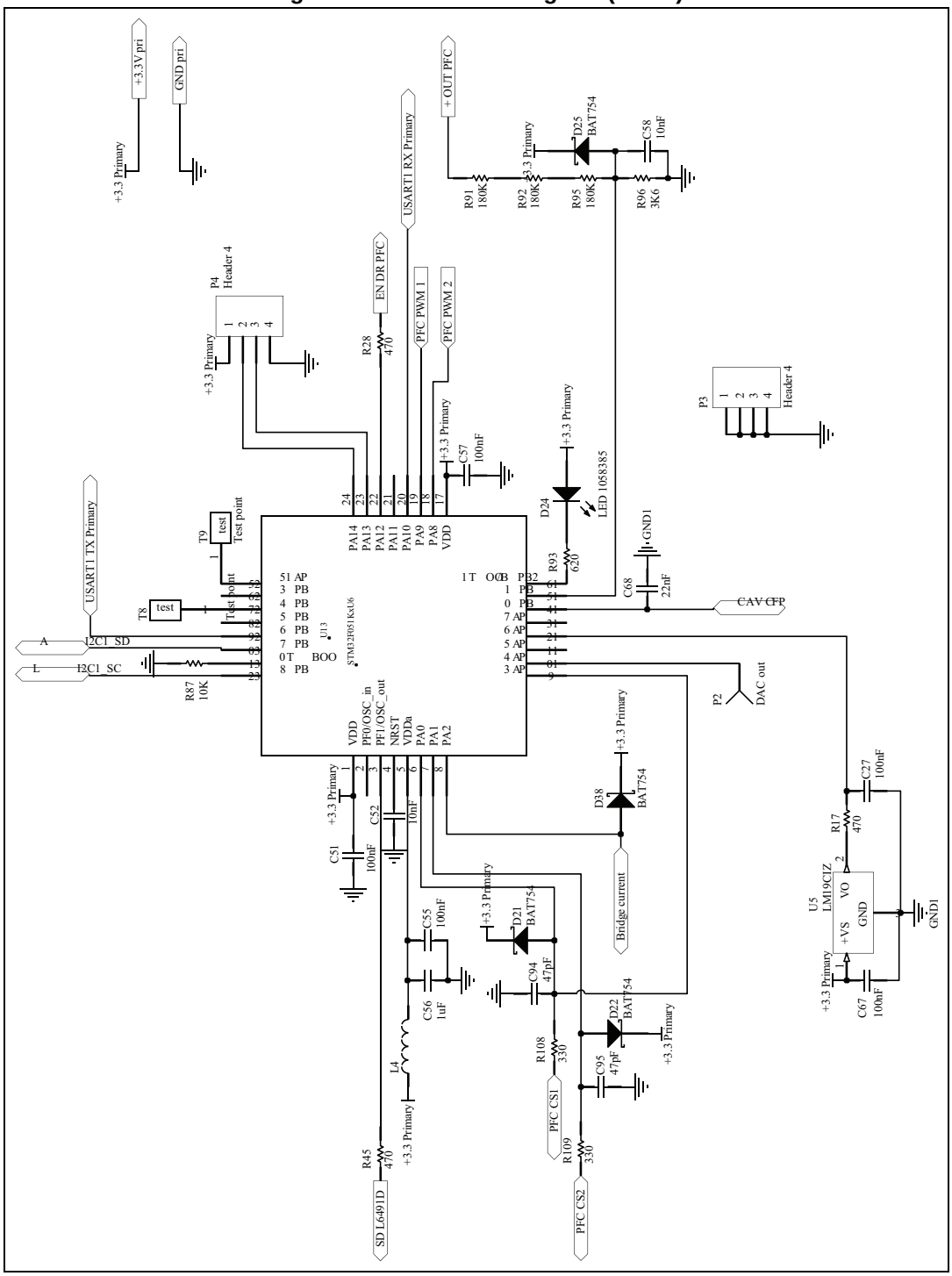
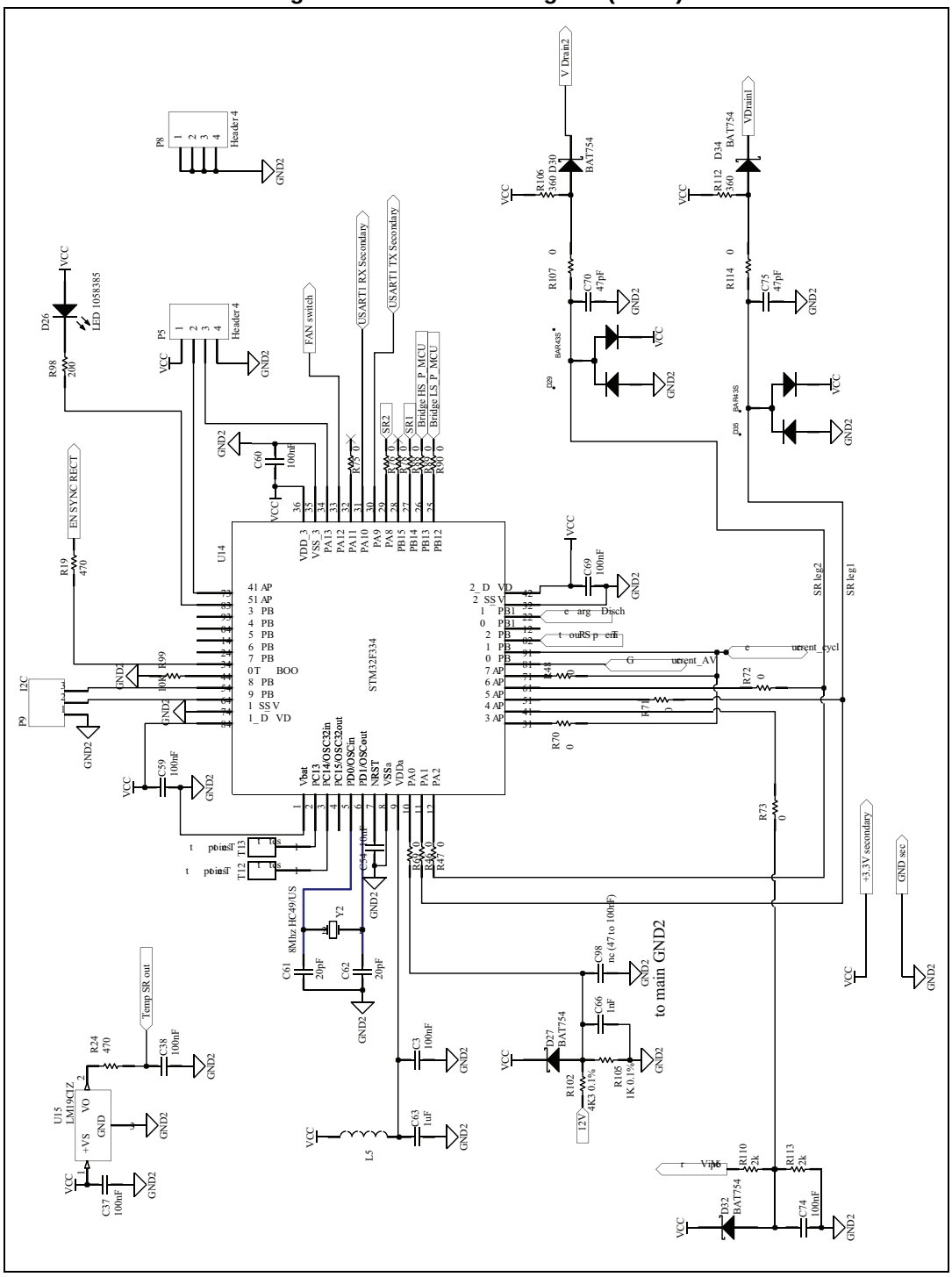


Figure 45. Schematic diagram (6 of 6)



5 Conclusion

This application note describes the design of a 500 W fully digital switch mode power supply. The system is based on a two-stage architecture consisting of a semi-bridgeless PFC circuit and an LLC half-bridge DC-DC stage. The control architecture is designed around two 32-bit MCUs from the STM32 family of microcontrollers. The control algorithm for both the PFC and the LLC converters is highlighted throughout the document. The experimental evaluation shows that high efficiency (93.2%), near unity power factor, and low THD% can be achieved under wide input voltage and load current conditions thanks to the performance of the ST products used and to the implementation of suitable control strategies on high-performance 32-bit microcontrollers.

6 References

- AN2450: LLC resonant half-bridge converter design guideline
- High frequency transformer for 500 W LLC converter: Magnetica 1892.0039
- Inductor chokes for 500 W bridgeless PFC: Yujing Technologies 11999-126H400210 QP-3930H

7 Revision history

Table 12. Document revision history

Date	Revision	Changes
19-Jun-2014	1	Initial release.