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# IR3M95N4

Application note Ver.0.1

DEVELOPMENT DEPT. II

SYSTEM DEVICE UNIT

ELECTRONIC COMPONENTS AND DEVICES DIVISION

SHARP CORPORATION

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## 1. General description

IR3M95N4 is a controller IC of LED Lighting power supply.

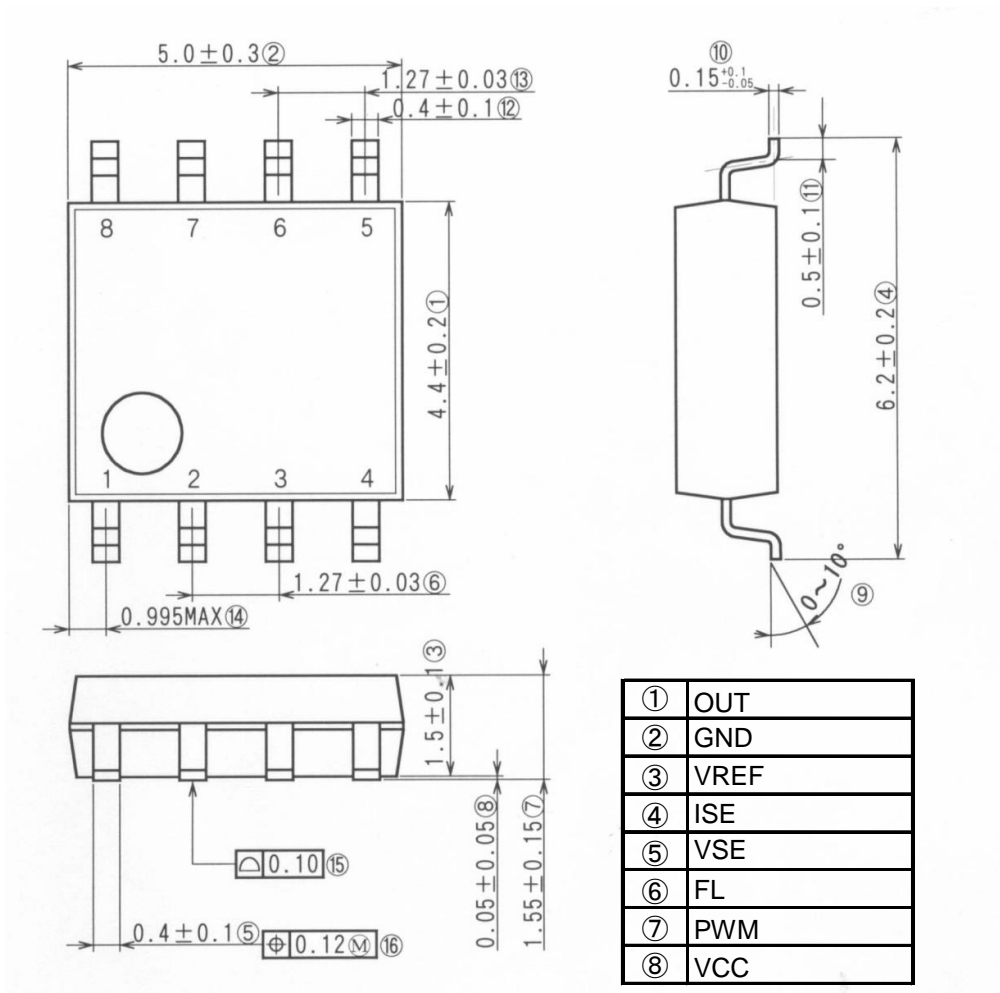
Operation mode is Critical Current Mode. It can enable high power factor by controlling ON period constant, and enable high efficiency and low EMI by quasi-resonant operation.

Either insulated or non-insulated circuit is capable in accordance with the purpose.

Insulated circuit uses flyback converter method, and is able to control in high power factor and high accuracy.

Non-insulated circuit uses step up converter method with transformer, and is able to control in high power factor, high accuracy and high efficiency. In comparison with insulated circuit, non-insulated circuit can smaller the size and lower the price of the power system by decreasing external components.

## 2. Pin assignment and Package outline



### 3. Pin description

Pin name	Pin description
1.OUT	Gate drive for the external switching MOSFET
2.GND	Ground pin
3.VREF	Analog dimmer input pin
4.ISE	Current sense of the primary winding
5.VSE	Voltage sense of the auxiliary winding
6.FL	The output pin of error amplifier.
7.PWM	PWM signal input pin
8.VCC	Power supply pin

### 4. Absolute maximum ratings

Absolute maximum ratings are values or ranges which can cause permanent damage.

Please do not exceed this range even when start up or shut down.

Ta=25°C

Parameter	Symbol	Rating	Unit	Applied terminal
Power Supply Voltage	Vcc	-0.3 ~ 28.0	V	VCC
Input Terminal Voltage	VI1	-0.3 ~ 6.0	V	ISE, VSE, FL,VREF,PWM
Output Terminal Voltage	VO1	-0.3 ~ 28.0	V	OUT
Operating Temperature	TOPR	-30 ~ 100	°C	
Storage Temperature	TSTG	-40 ~ 150	°C	

## 5. Electrical characteristics

Unless otherwise specified, condition shall be GND=ISE=VSE=0V, VCC=16V, Ta=25°C.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
VCC section						
VCC Input Voltage	VCC1	10	16	18	V	
VCC Startup Current	ICC1	—	30	T.B.D.	μA	VCC=Startup voltage – 0.1V
VCC Operating supply current	ICC2	—	1.4	T.B.D.	mA	
VCC Turn ON threshold	Vst	T.B.D.	18.0	T.B.D.	V	
VCC Turn OFF threshold	Vuvlo	T.B.D.	6.0	T.B.D.	V	
Gate driver section						
Output Low Resistance	RL	—	—	15	Ω	OUT+0.1V
Output High Current	IOH	40	—	—	mA	OUT<8V
Output High Voltage Limit	VOH	T.B.D.	10	T.B.D.	V	
Oscillator section						
Frequency	fosc	T.B.D.	200	T.B.D.	kHz	FL=2.5V
Error Amplifier Section						
Reference Voltage	VREF	T.B.D.	2.50	T.B.D.	V	
Feedback Voltage	VFB	T.B.D.	300	T.B.D.	mV	VSE=1V, ISE=0.3V, FL=2.5V
Transconductance	Gm	—	43	—	μA/V	ISE=0.3V
FL Operating range	Vfl	0.5	—	4.0	V	
Zero Cross Detect Section						
VSE Threshold Voltage	VVSE	T.B.D.	0.3	T.B.D.	V	FL=2.5V
PWM section						
PWM Operating range	Vpwm	0	—	2	V	
Threshold High Voltage of PWM	VPWMH	T.B.D.	0.25	T.B.D.	V	
Threshold Low Voltage of PWM	VPWML	T.B.D.	0.125	T.B.D.	V	
FUNC Bias Current	IFUNC	T.B.D.	10.0	T.B.D.	μA	
Over Current Protection Section						
Threshold Voltage	VOCP	T.B.D.	1.60	T.B.D.	V	FL=2.5V
Minimum Off Time in OCP	tmin	T.B.D.	70	T.B.D.	us	
Leading edge blanking time	tleb1	—	200	—	ns	
Over Voltage Protection Section						
Threshold Voltage of VSE	VOVP_VSE	T.B.D.	2.1	T.B.D.	V	
Threshold Voltage of VCC	VOVP_VCC	T.B.D.	22.7	T.B.D.	V	
Leading edge blanking time	tleb2	—	600	—	ns	
Over Temperature Protection Section						
Threshold Temperature	TSD	135	150	165	°C	Junction temperature ,(※)

(※) It is secured by the design and the test is not done.

## 6 . Operation mode description

### 6 . 1 Critical Current Mode operation

When using insulated flyback converter method, this IC will operate in Critical Current Mode by detecting the timing when the secondary inductor's current becomes 0mA, and turn on the FET.

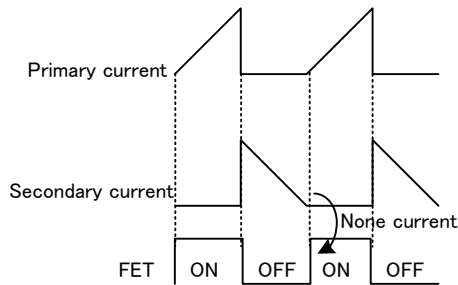


Fig.1 Critical Current Mode operation

### 6 . 2 Power factor improvement operation

ON period will become almost constant by error amplifier controlling.

Since ON period is constant, peak current of inductor will vary in proportion with input voltage.

Therefore input current varies in accordance with input voltage, and the power factor will improve.

$di(t) = v(t) \cdot dt / L$  ---- Peak current of inductor is proportional with input voltage, when ON period is the same.

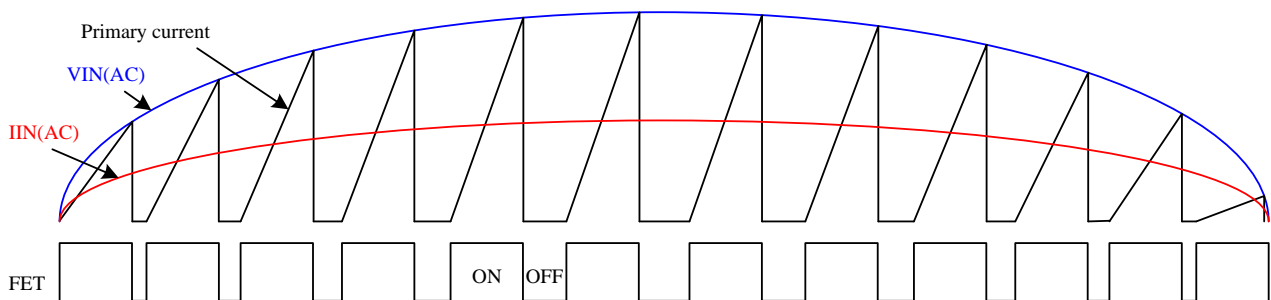


Fig.2 Improvement of power factor by constant ON time operation.

### 6.3 Quasi-resonant operation

This IC will drive the FET by Critical Current Mode, which detect the timing when the current of inductor becomes 0mA and turn on the FET.

When it is not Critical Current Mode, as shown in Fig.3, after releasing all the energy of inductor the inductance of primary transformer and the parasitic capacitance will cause ringing at the drain of FET, and spread EMI around the circuit.

When it is Critical Current Mode, the VSE terminal monitors the timing when inductor release all the energy and turn on FET almost at the bottom point of ringing waveform, which is called quasi-resonant operation. Therefore it can minimize the noise of EMI to spread around the circuit.

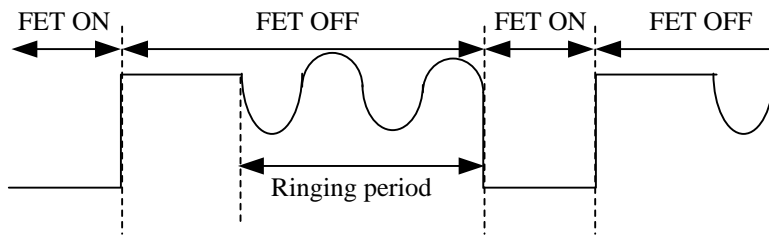


Fig.3 Waveform of FET drain (Not Critical Current Mode)

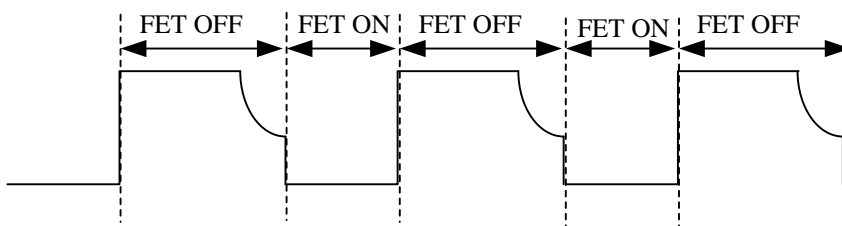


Fig.4 Waveform of FET drain (Critical Current Mode)

## 6.4 Constant Current Output Operation

When it is insulated flyback converter, constant current output is enabled only by using primary current control, without using feedback of secondary (LED) current by Photo coupler.

As shown in Fig.4, the average amount of output current ( $I_{out}$ ) can be expressed by using peak current of secondary current ( $I_{pk2}$ ) and the period secondary current flows ( $T_{res}$ ).

$$I_{out} = 1/2 * I_{pk2} * T_{res} / T_c \quad (1)$$

Peak current of primary and secondary current has relation with the ratio of primary and secondary winding.

$$I_{pk2} = N_p / N_s * I_{pk1} \quad (2)$$

(  $N_p$  = primary winding turns,  $N_s$  = secondary winding turns )

$T_{res}/T_c$  can be detected by using auxiliary winding which is set in primary transformer.

$$I_{out} = 1/2 * N_p / N_s * I_{pk1} * T_{res} / T_c \quad (3)$$

Constant current output can be obtained also in non-insulated step up circuit.

In this circuit  $I_{pk2}=I_{pk1}$ , and will be expressed as shown below.

$$I_{out} = 1/2 * I_{pk1} * T_{res} / T_c \quad (4)$$

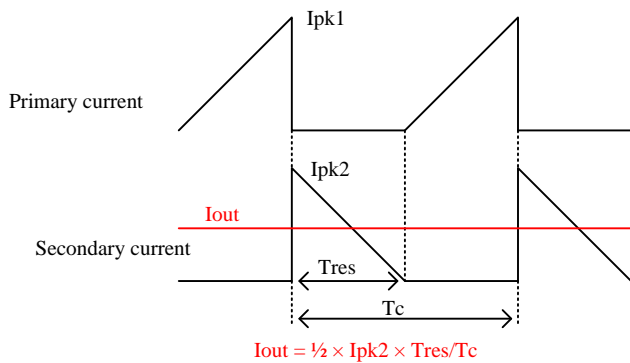


Fig.5 Constant current output control



## 7. Block description inside the IC

### 7.1 Start up circuit (VCC)

FET starts switching when VCC reaches up to start up voltage  $V_{start} = \text{Typ. } 18\text{V}$ .

After turning on AC voltage, current is supplied to  $C_{vcc}$  from  $V_{IN}$  through  $R_{start}$ , and VCC voltage rises.  $T_{start}$ , which is the time for VCC to reach start up voltage can be expressed as shown below.

$$T_{start} = C_{vcc} * V_{start} / ( I_1 - I_2 ) \quad (5)$$

$I_2$  is current consumed in IC.  $I_1$  is current supplied from  $V_{IN}$  through  $R_{start}$ .  $I_1$  can be expressed as shown below.

$$I_1 = ( V_{IN} - V_{CC} ) / R_{start}$$

Equation (5) can be expressed as shown below, using the equation above.

$$T_{start} = C_{vcc} * V_{start} / ( ( V_{IN} - V_{CC} ) / R_{start} - I_2 ) \quad (6)$$

And the loss at  $R_{start}$  is expressed as shown below.

$$R_{start} \text{ Loss} = ( V_{IN} - V_{CC} )^2 / R_{start} \quad (7)$$

When,  $V_{start} = 18\text{V}$ ,  $V_{CC} = 18\text{V}$ ,  $I_2 = 30\mu\text{A}$ ,  $C_2 = 10\mu\text{F}$ ,

$R_{start} = 300\text{k}\Omega$ ,  $V_{IN} = 100\text{V}$

$$T = 10\mu\text{F} * 20\text{V} / ( ( 100\text{V} - 20\text{V} ) / 300\text{k}\Omega - 30\mu\text{A} )$$

$$= 0.85\text{s}$$

$$R_{start} \text{ Loss} = ( 100\text{V} - 17.8\text{V} )^2 / 300\text{k}\Omega$$

$$= 23\text{mW}$$

$R_{start}$  should be smaller to speed up start-up sequence, but it has demerit of larger loss.

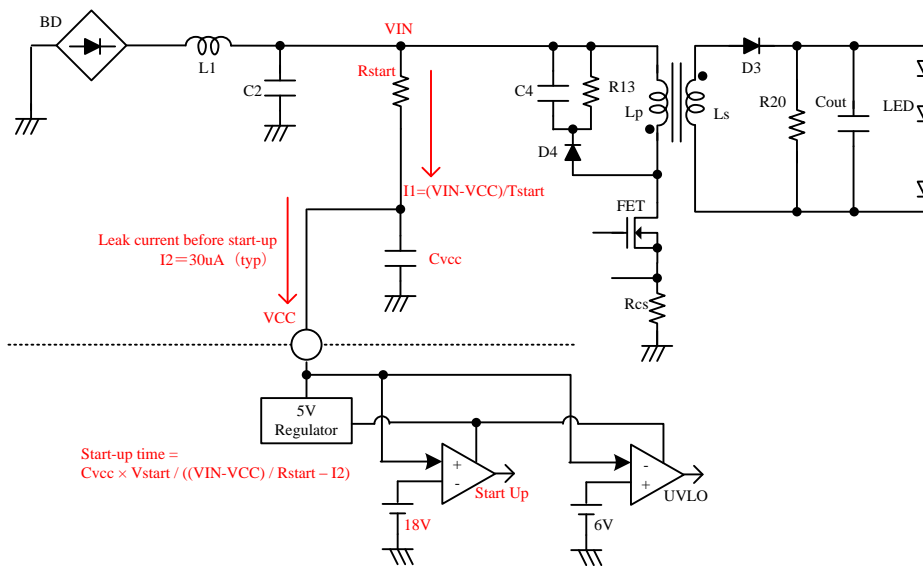


Fig.6 Start-up time



## 7.2 Switching circuit (OUT)

Connect the Gate of FET to OUT terminal.

When VSE goes down to 0.3V or less, FET turns on after 200ns (Typ.) delay time. The period FET is ON is the sum of the time in accordance with output voltage (FL) of error amplifier (EAMP) and 200ns (Typ.) delay time.

OUT is clamped by 10V (Typ.) in maximum voltage.

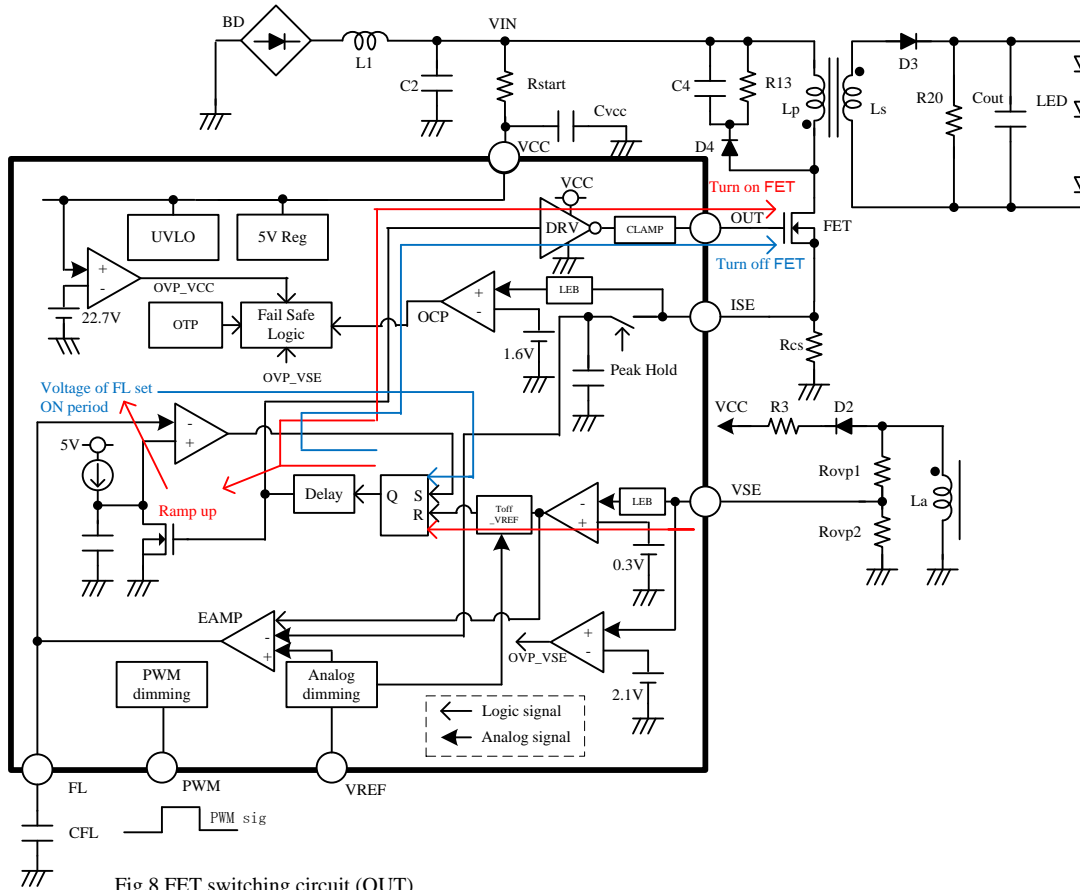


Fig.8 FET switching circuit (OUT)

FET ON timing = 200ns after VSE terminal goes down to 0.3V.

FET ON period = period in accordance with FL + delay time 200ns.

※The period in accordance with FL can be referred in "7.5 Error Amplifier (FL)".

### 7.3 ON timing detecting circuit (VSE)

When FET turns OFF, the drain voltage of FET rises, and voltage in accordance with the winding turns ratio arise at secondary and auxiliary windings. Since current of LED starts to flow when secondary winding voltage goes up to  $V_{LED} + V_{D3}$ , the voltage of auxiliary winding can be expressed as

$$(V_{LED} + V_{D3}) * N_a / N_p$$

When secondary current goes down to 0mA, the voltage of secondary winding and auxiliary winding decreases. VSE terminal has two purpose. First to detect the voltage decrease of auxiliary winding, to indicate the next ON timing. And second to measure the period that current flows at secondary winding ( $T_{res}$ ).

Leading edge blanking (LEB) from the FET OFF timing is made to mask the period until the VSE voltage stabilizes.

When VSE goes down to 0.3V or less, after 600ns (Typ.) period of leading edge blanking from the FET OFF timing, and the OFF time ( $T_{OFF\_VREF}$ ) according to  $V_{REF}$ , FET turns ON.

$T_{OFF\_VREF}$  can be referred in "7.6 Analog Dimmer ( $V_{REF}$ )".

FET ON timing :  $VSE < 0.3V$  &  $T_{off} > LEB$  &  $T_{off} > T_{OFF\_VREF}$

Actually there is error time ( $\Delta T$ ). After secondary winding current becomes 0mA, VSE terminal voltage starts decrease. The period between the starting timing of VSE decrease and the timing VSE terminal crossing down to 0.3V is error time ( $\Delta T$ ). Therefore error occurs in output current control.

$$I_{out} = 1 / 2 * N_p / N_s * I_{pk1} * (T_{res} + \Delta T) / T_c \quad (10)$$

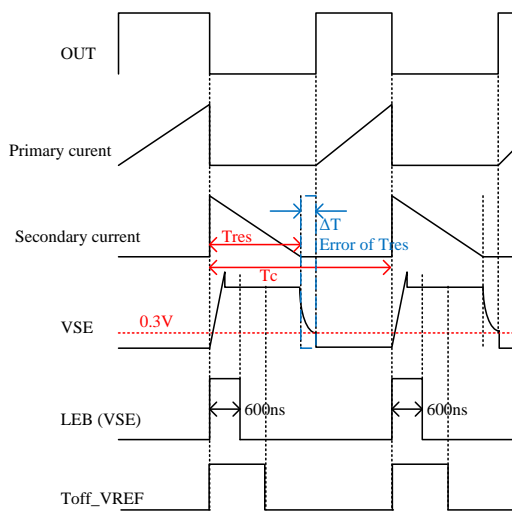


Fig.9 VSE waveform

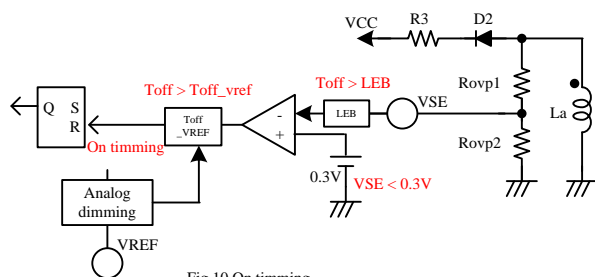


Fig.10 On timing



## 7.4 Peak current detecting circuit (ISE)

ISE terminal is made to detect peak current of primary winding current when FET is ON.

ISE terminal is connected to the source of FET, and current detecting resistor  $R_{cs}$  is connected between the source of FET and GND. The period ISE terminal detects the peak current starts from the timing 200ns before OUT turns OFF, and end at the timing OUT turns OFF. It holds the peak amount during the period FET is OFF.

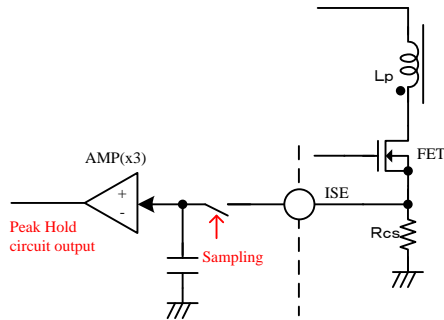


Fig.13 Peak detecting circuit of primary current

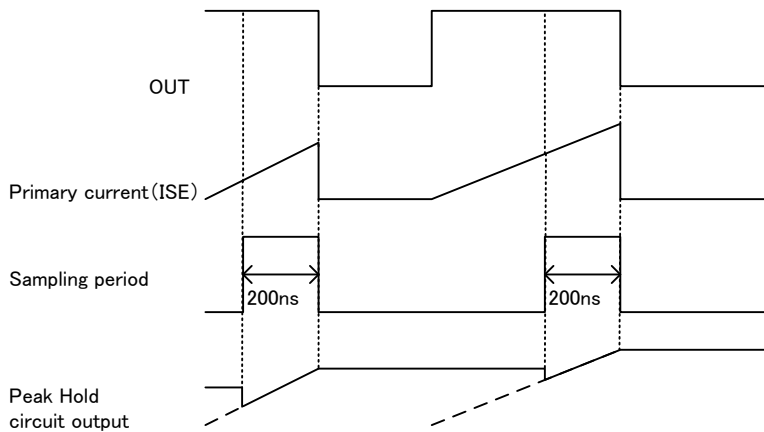


Fig.14 Peak detecting waveform of primary current

## 7.5 Error amplifier circuit (FL)

FL is an output of error amplifier (EAMP).

The voltage of FL terminal sets FET ON period. As shown in Fig.16, ON period is as shown below.

$$\text{ON period} = 2.66\text{pF} * \text{VFL} / \text{Ibias} \quad (10)$$

Variation range of VFL is 0.5V to 4V, and on period is 0.66us to 5.33us at  $\text{Ibias}=2\mu\text{A}$ .

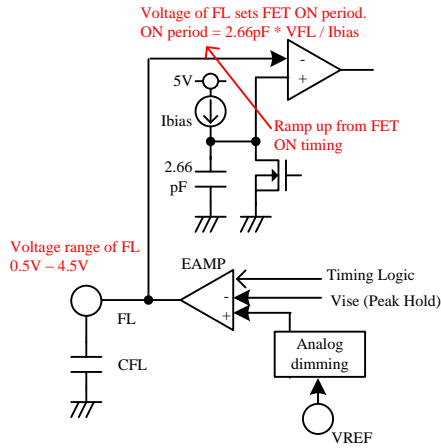


Fig.15 FET ON period control by error amplifier

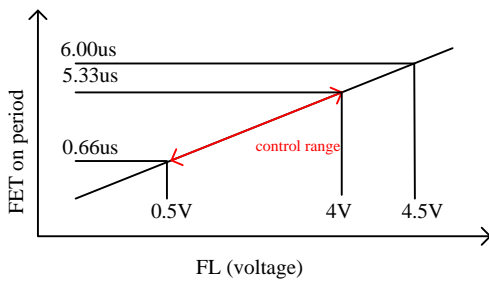


Fig.16 Relation between FL voltage and FET on period

As FL output is clamped on the maximum voltage 4.5V, ON period increases no more. This limits input AC currents when power supply voltage falls rapidly, which is brownout function.

Since power-factor may decline when CFL is small, please set up sufficiently big CFL.

The recommended value of CFL: 1uF

## 7.6 Analog Dimmer (VREF)

Output current can be adjusted according to the voltage of VREF terminal.

Since VREF terminal has input resistance of several 100 kohm, it recommends that the voltage of input is low resistance.

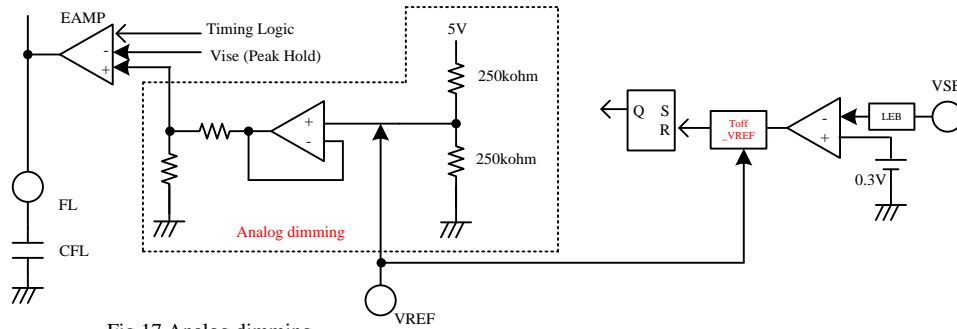


Fig.17 Analog dimming

TOFF\_VREF according to VREF voltage becomes as it is shown in (11).

$$\text{TOFF\_VREF} = 36\mu\text{s} / (\text{VREF} * 20 + 0.25) \quad (11)$$

ON time (FL) is adjusted according to TOFF\_VREF.

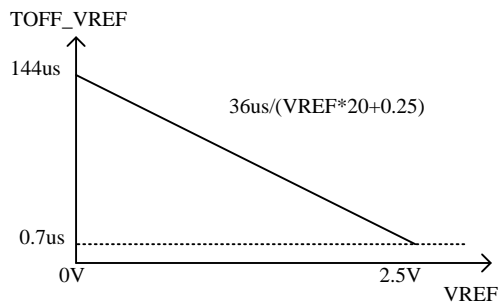


Fig.18 TOFF\_VREF



## 7.7 PWM Dimmer (PWM)

LED current can be adjusted according to Duty of PWM pulse input to PWM terminal.

The input condition of the PWM signal is as follows.

PWM pin setting (@1kHz)	Dimming result
2.0V > FUNC > 0.3V	Out pin: switching
0.1V > FUNC	Out pin: OFF (※)

(※) In PWM < 0.1V, the value of FL is kept and the switching-ON pulse is kept constant. It can be used as standby mode.

The example of connection of PWM terminal is as in Fig.19.

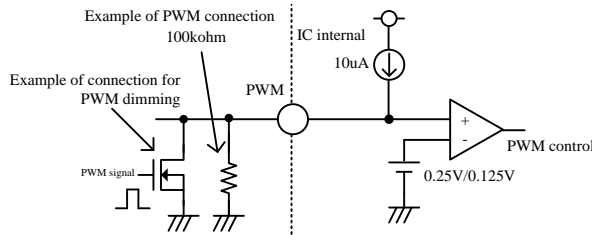
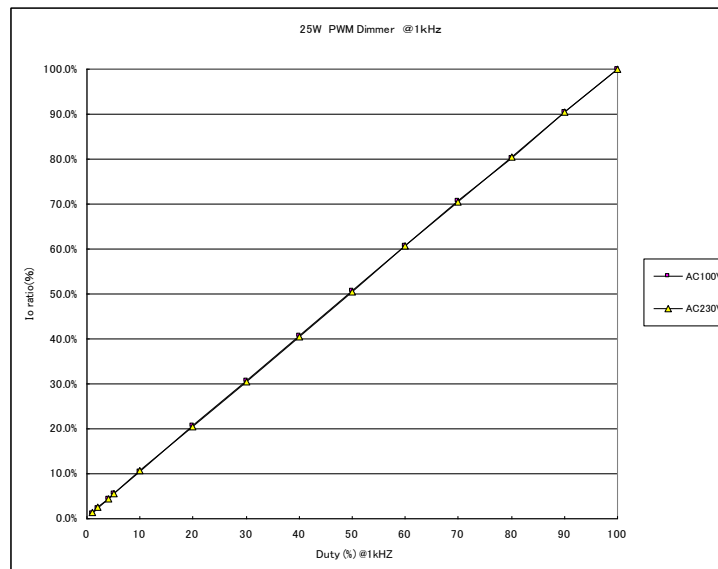
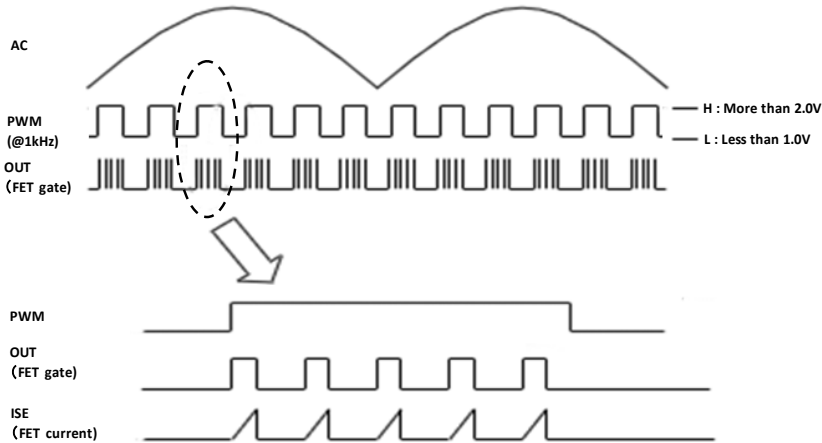


Fig.19 PWM pin

When a PWM function is used, please use it after are satisfactory or checking enough with the system, since sound may occur with a transformer, a coil, etc.





## 9. Protection Function

### 9.1 Soft start function

At start up, switching operation is performed in soft start sequence. ON time and OFF time shown at below table are repeated in turns until condition of StartupOK.

ON timing : ISE=0.6V or Ton(Max.)=6us

OFF period : Critical Current Mode operation, Toff (Min.) = 12 us or more

Condition of Startup OK : VSE > 0.8V.

Mode	Soft start	Startup OK judge
Flyback	ON: ISE=0.6V, Ton(max)=6us OFF: Critical Current Mode operation, Toff(min)=12us	VSE=0.8V

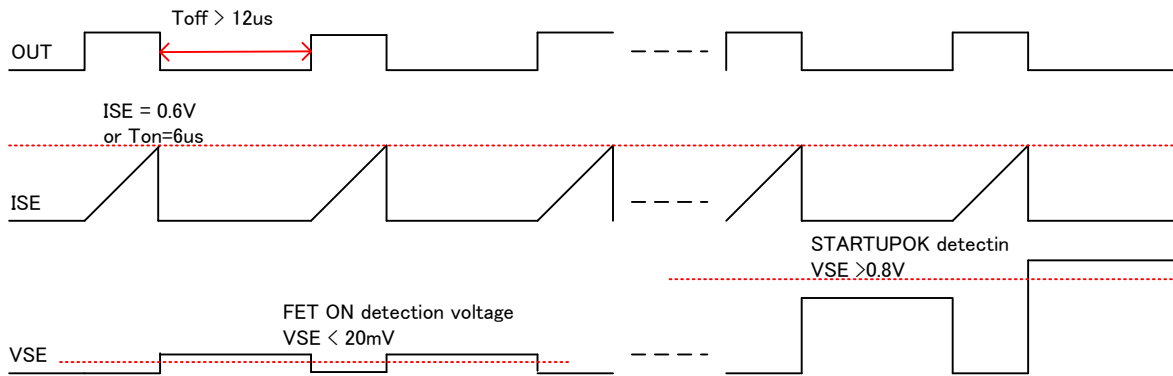


Fig.22 Softstart

## 9.2 Over temperature protection

When junction temperature of this IC exceeds 150°C, over temperature protection (OTP) starts to operate and following operation is performed.

- IC shut down (OUT is Lo).
- Discharge capacitor connected to FL (CFL).
- Discharge capacitor connected to VCC(Cvcc).
- When VCC goes down to UVLO (Typ.6V) or less, discharge of Cvcc stops.

## 9.3 VCC under voltage lock-out

IC operation stops when VCC voltage goes down to Typ.6V or less, caused by VCC voltage lowering or short between VCC and GND.

IC operation restarts when VCC voltage goes up to Typ.18V or more (start up voltage).

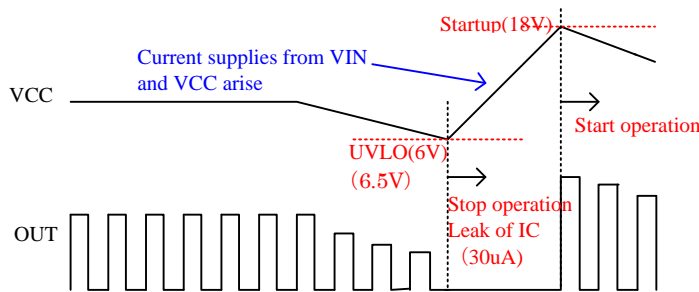


Fig.23 UVLO detection sequence

## 9.4 Output over voltage lock-out

When over voltage error is detected ,following operation is performed.

- IC shut down (OUT is Lo).
- Discharge capacitor connected to FL (CFL).
- Discharge capacitor connected to VCC(Cvcc).
- When VCC goes down to UVLO (Typ.6V) or less, discharge of Cvcc stops.

Over voltage protection is masked at Leading edge blanking (LEB) period, that is 600ns (Typ.) from the timing OUT becomes Lo (Fig. 24).

Over voltage protection is detected by  $V_{OVP\_VSE} \geq 2.1V(\text{Typ.})$  (12), and  $V_{OVP\_VCC} \geq 22.7(\text{Typ.})$  (13).

$$V_{ovp\_vse} = 2.1V * (R_{ovp1} + R_{ovp2}) / R_{ovp2} * N_s / N_a \quad (12)$$

$$V_{ovp\_vcc} = 22.7V * N_s / N_a \quad (13)$$

※ $V_{ovp\_vse}$  is over voltage threshold voltage for VSE.  $V_{ovp\_VCC}$  is over voltage threshold voltage for VCC.

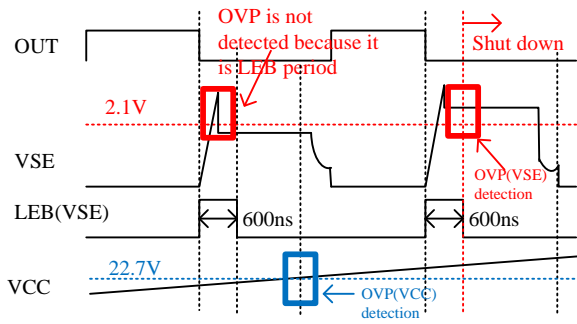


Fig.24 OVP detection

Protected operation is carried out when the conditions of VSE and VCC overlap.

### 9.5 FET over current protection

The IC observe FET ON current, and when ISE goes up to over current threshold voltage (Vocp) or more, over current error is detected and following operation is performed.

- OUT turns Lo and stops switching.
- IC do not shut down.
- OFF period will be more than 67us (Typ.).

The voltage of ISE terminal at over-current detection is as follows.

Mode	over-current detection volgate
Flyback	ISE $\leq$ 1.6V(Typ.)

Over current protection is masked at leading edge blanking (LEB) period, that is 200ns (Typ.) from the timing OUT becomes Hi (Fig. 25).

When OCP is detected, OFF period is set to be 67us(Typ.).

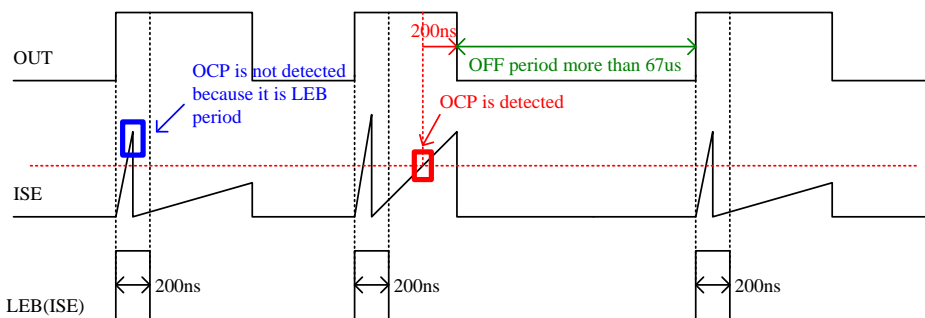


Fig.25 OCP detection

## 1 0 . External circuit example

### 1 0 . 1 Transformer

First you must fix the input condition of AC power source

VAC : 85V (Min.) ~ 265V (Max.)

Fix inductance of primary winding of transformer ( $L_p$ ) to make ON period 5us at the condition VAC (Min.).

$$L_p = VAC \text{ (Min.)} * T_{on} / I_p \quad (14)$$

When duty is 50%, since AC input current is  $I_{AC} = I_p / 4$ ,  $I_p$  can be expressed as below

$$I_p = 4 * P_{in} / VAC \text{ (Min.)} \quad (15)$$

$$I_{AC} = I_p / 4 \quad (16)$$

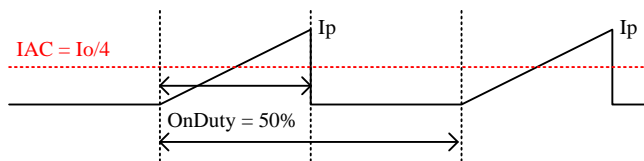


Fig.26

$P_{in}$  and  $P_{out}$  can be expressed as below, using conversion efficiency  $\eta$

$$P_{in} = P_{out} / \eta \quad (17)$$

When  $VAC(\text{Min.})=85V, T_{on}=5\mu s, P_{out}=25W,$  and efficiency  $\eta = 88\%$

$$P_{in} = 25W / 88\% = 28.4W$$

$$I_p = 4 * 28.4W / 85V = 1.34A$$

$$L_p = 85V * 5\mu s / 1.34A = 317\mu H$$

• Primary winding

$$N_p = VAC \text{ (Min.)} * \sqrt{2} * T_{on} \text{ (Max.)} / (A_e * B_T) \quad (18)$$

Use the larger amount between

$$V_{in} \text{ (Min.)} * T_{on} \text{ (Max.)} \text{ or } V_{in} \text{ (Max.)} * T_{on} \text{ (Min.)}$$

$A_e$  is the effective area of the core in transformer.

$B_T$  is saturation flux density.

Use ER28 core ( $A_e = 86\text{mm}^2$ ), calculate using saturation flux density  $B_T = 320\text{mT}$

$$N_p = 85V * \sqrt{2} * 5\mu s / (86\text{mm}^2 * 320\text{mT})$$

$$= 21.8$$

Set  $N_p$  more than the value above.

•  $N_s$  ( Secondary winding turns )

$$N_s = N_p * V_{out} / VAC \text{ (Min.)} \quad (19)$$

When  $N_p=22, V_{out}=35.5V, VAC(\text{Min.})=85V$

$$N_s = 22 * 35.5V / 85V = 9.2$$

Therefore  $N_s = 9$

· Na ( Auxiliary winding turns )

Make VCC voltage more than 16V.

$$Na = Ns * VCC / Vout \quad (20)$$

$$= 9 * 16V / 35.5V = 4.2$$

Therefore Na=4

· Winding form

Voltage change of primary winding make an effect on auxiliary winding, in accordance with magnetic coupling strength of primary winding and auxiliary winding.

It is able to weaken magnetic coupling by changing winding form, and weaken the effect on auxiliary winding

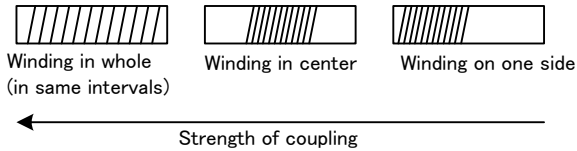


Fig.27 Strength of coupling between primary winding and auxiliary winding for each winding form of auxiliary winding.

## 1 0 . 2 F E T

Please use FET with a sufficient margin against primary winding peak current, and drain voltage rising at FET OFF.

When the gate of FET change from Hi to Lo, negative surge is applied to the source of FET. Because there is parasitic capacitance between the gate and the source of FET.

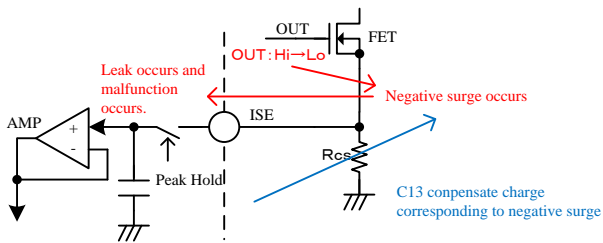


Fig.28 Counter measure against negative surge

### 1 0 . 3 Snubber circuit

When using insulated flyback circuit, you must consume the energy of leakage inductance caused by imperfect magnetic coupling of transformer at the primary winding.

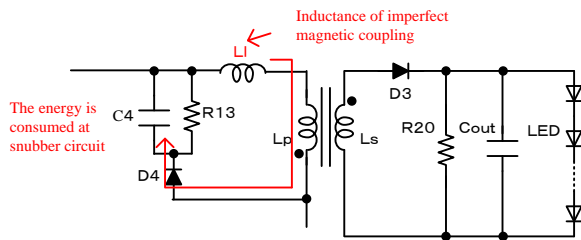


Fig.29 Snubber circuit

Appropriate value of C4 and R13 is set to keep voltage jumping of the drain at low level.

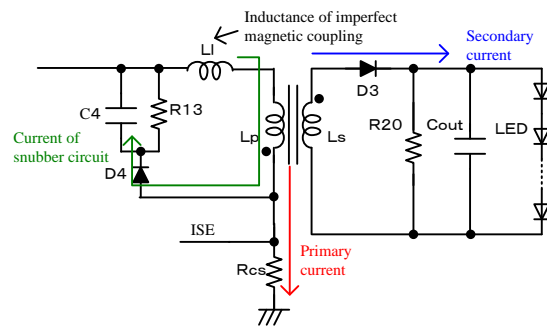
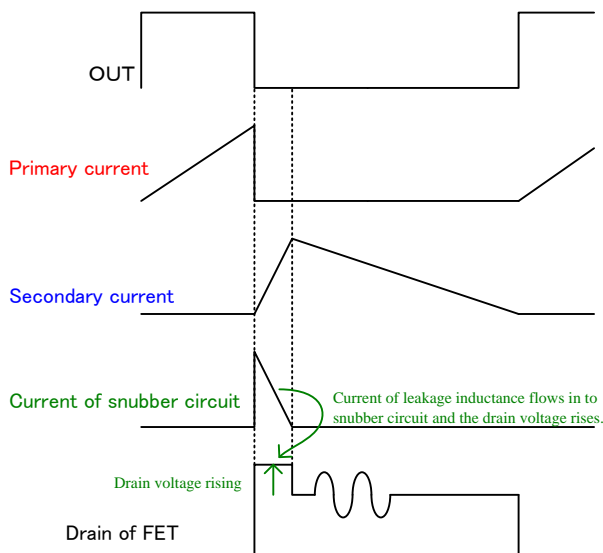


Fig.30 Drain voltage rising caused by leakage inductance



## 1 0 . 4 Filter circuit

The value of L1 and C2 is set by EMI observation. The cut off frequency of low pass filter made by L1 and C1 is as shown below.

$$F_c = 1 / ( 2\pi \sqrt{ ( L1 * C2 ) } ) \quad (21)$$

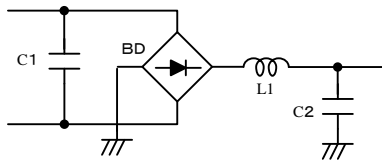


Fig.31 LC filter

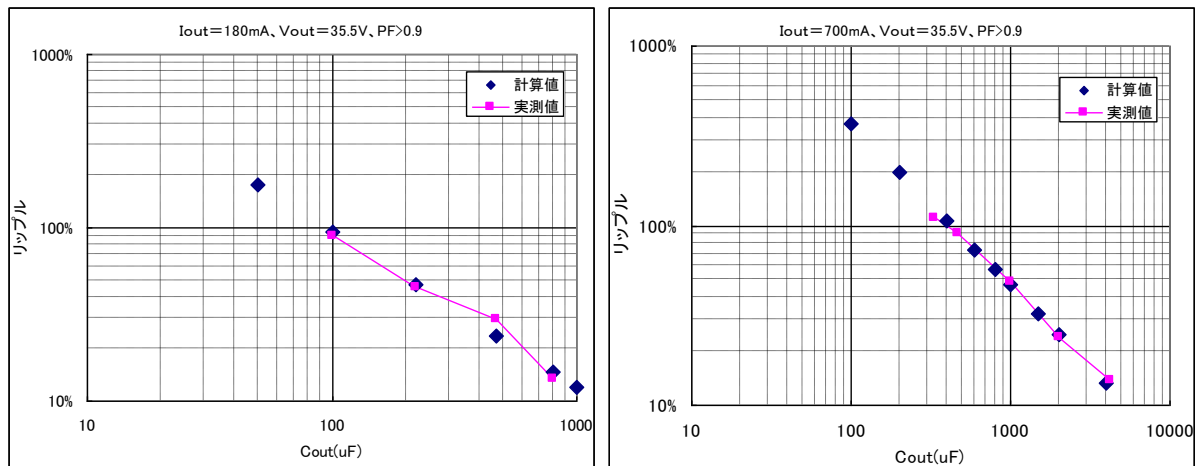
## 1 0 . 5 Output capacitor

A large value of output capacitor (Cout) is needed to keep output current ripple at low level.

At the condition of power factor more than 0.9, the output ripple is approximately as shown below.

$$\text{Output ripple rate} = I_{out} / 3 * C_{out}^{-0.9} \quad (22)$$

Where Iout is output current



## 1 1 . Notes on Contents

### 1) Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

### 2) Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

### 3) Timing Charts

Timing charts may be simplified for explanatory purposes.

### 4) Application Circuits

The application circuits shown in this document are provided for reference purposes only.

Thorough evaluation is required, especially at the mass production design stage.

Sharp does not grant any license to any industrial property rights by providing these examples of application circuits.