

Application Note:

TDPS251E0D2 LLC DC/DC Converter Evaluation Board

1. Introduction

The Evaluation Board for an LLC circuit using GaN HEMTs is described in this paper. In this board, Transphorm GaN power HEMTs with low reverse-recovery charge and low output capacitance are used in a diode-free half bridge to realize DC-DC voltage conversion with high efficiency. The performance and efficiency improvement achieved by use of the GaN HEMTs in the primary side of the LLC circuit is further enhanced by use of synchronous rectification in the secondary side. The evaluation board is shown in Fig. 1.



Fig. 1. LLC DC/DC converter Evaluation Board



2. TDPS251E0D2 Input/output Specifications:

• Input: start up voltage between 390-400Vdc (operation range: 380-400 Vdc);

• Output: 12Vdc at 20A;

• PWM Frequency: 170kHz to 250 kHz

• Auxiliary Supply (12Vdc for bias voltage): The board is optimized for this bias voltage; please provide 12V exactly for the best performance.

3. Circuit Description for LLC DC-DC Converter based on GaN HEMT

Figure 2 illustrates the topology of the evaluation board, which is based on the NCP1397 and NCP4304 controllers. The series capacitor forms the series parallel resonant tank with leakage and magnetic inductances in the primary side of the transformer. From this configuration, the resonant tank and the load on the secondary side, act as a voltage divider. By changing the frequency of input voltage, the impedance of resonant tank will change; this impedance will divide the input voltage with load. The primary-side switches, M1 and M2, are the GaN HEMTs. Transistors S1 and S2 on the secondary side are synchronous rectifiers to improve the performance and efficiency. As may be seen in Fig. 2, there is no need for special gate drivers for the GaN HEMTs. Further information and discussion on the fundamental circuit schematics and the characteristics of LLC DC-DC converters are provided in [1]-[3].

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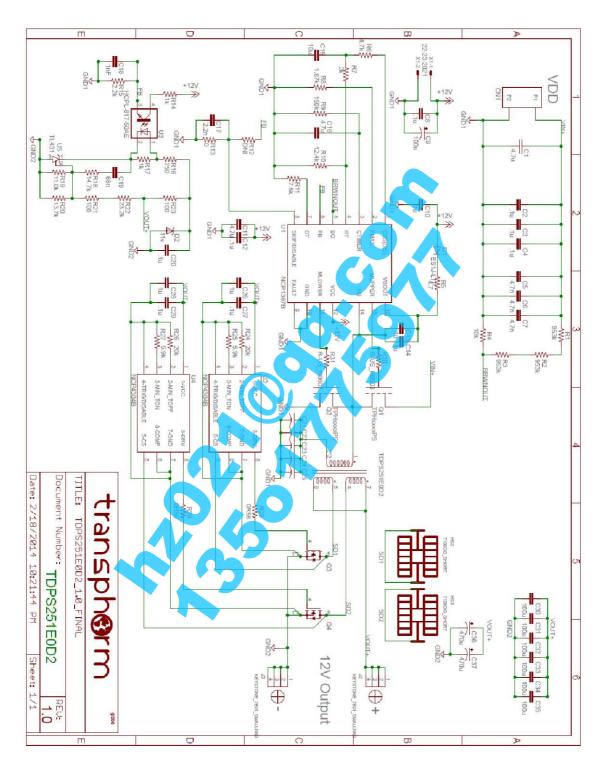


Fig.4. LLC DC/DC Converter Evaluation Board Circuit Schematics

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While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the Transphorm GaN HEMT will switch at dV/dt of 100V/ns or higher. At this level of operation, even the layout becomes a significant contributor to performance. As shown below, in Fig. 5-7, the recommended layout keeps a minimum gate drive loop; it also keeps the traces between the switching nodes very short, with the shortest practical return trace to power ground. As the power ground plane provides a large cross sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the HEMT to avoid any possible ground loop.

Note that the Transphorm GaN HEMTs in TO220 package has pin out configured as G-S-D, instead of traditional MOSFET's G-D-S arrangement. The configuration is designed with thorough consideration to minimize the Gate-Source driving loop to reduce parasitic inductance, as well as to separate the driving loop (Gate-Source) and power loop (Drain-Source) to minimize noise. For further information, different layers of TDPS251E0D2 design are shown in Fig. 5-7.

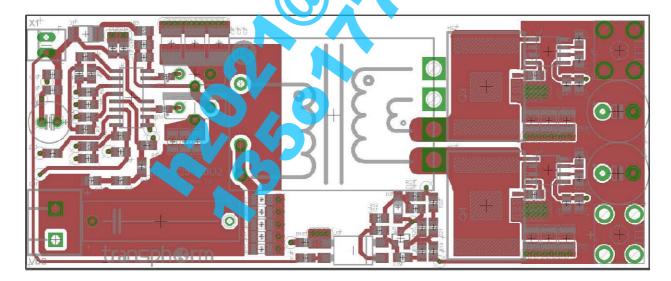


Fig. 5. LLC DC/DC converter Evaluation Board Layout, Top Layer



Probing primary-side voltage waveforms



Fig. 8. The voltage probing on the primary side for LLC DC/DC converter board

Efficiency has been measured at 390Vde input and 12Vdc output using the WT1800 precision power analyzer by Yokogawa. The results for this LLC DC/DC converter are shown in Table. 3, and Fig. 9. The peak efficiency is more than 97%, which is noticeably better than competitor LLC boards with Si switches; this high efficiency will enable customers to reduce system loss for more compact designs in addition to more efficient energy usage.

Table 3. The power and efficiency result for LLC board at 390Vdc input and 12Vdc output

Pin (W)	Pout (W)	Ploss (W)	Eff (%)
32.46	30.86	1.60	95.06
63.28	61.34	1.94	96.93
95.87	93.36	2.51	97.39
128.00	124.75	3.25	97.46
158.31	154.16	4.15	97.38
188.39	183.16	5.24	97.22
220.13	213.45	6.67	96.97
250.16	241.86	8.30	96.68

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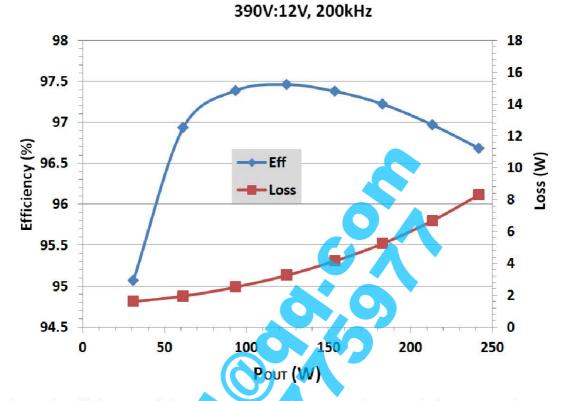


Fig. 9. The efficiency result for LLC DC/DC Converter Board at 390Vdc input to 12Vdc output

WARNING: There are no specific current or voltage protection on this board; users need to follow the test procedure and operation limits carefully. Please refer to application note AN0002 and AN0003 for further information.

REFERENCES:

- [1]. Robert L. Steigerwald, "A Comparison of Half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, Vol. 3, No. 2, pp. 174-182, April 1988.
- [2]. Bo Yang, F.C. Lee, A.J. Zhang, H. Guisong, "LLC resonant converter for front end DC/DC conversion" *Proc. IEEE APEC'02*, pp.1108 1112, 2002.
- [3]. B. Lu, W. D. Liu, Y. Liang, F. C. Lee, and J. D. VanWyk, "Optimal design methodology for LLC resonant converter," *Proc. IEEE APEC '06*, pp. 19–23, 2006.