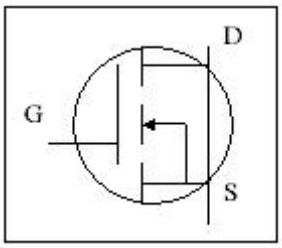
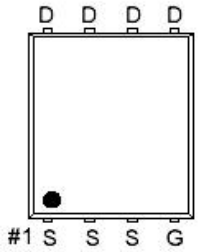
472

POWER MOSFET

The SD472 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. Standard product SD472 is Pb-free (meets ROHS & Sony 259 specifications). SD472L is a Green Product ordering option. SD472 and SD472L are electrically identical.

Simplified Schematic





RoHS Compliant

G. GATE
D. DRAIN
S. SOURCE

DFN5*6

Product Summary

VDS (V) = 30V
ID = 50A (VGS = 10V)
RDS(ON) <6 mΩ (VGS = 10V)
RDS(ON) <9.5 mΩ (VGS = 4.5V)

Absolute Maximum Ratings TA=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current G	TA=25°C	I_D	50	A
	TA=70°C		50	
Pulsed Drain Current C		I_{DM}	150	
Avalanche Current C		I_{AR}	30	A
Avalanche energy L=0.1mH C		E_{AR}	135	mJ
Power Dissipation B	TA=25°C	PD	50	W
	TA=100°C		25	
Power Dissipation A	TA=25°C	P_{DSM}	3	W
	TA=70°C		2.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient A	t ≤ 10s	$R_{\theta JA}$	15	20	°C/W
Maximum Junction-to-Ambient A	Steady-State		41	50	°C/W
Maximum Junction-to-Case B	Steady-State	$R_{\theta JC}$	2.1	3	°C/W

Electrical Characteristics (TJ=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BVDSS	Drain-Source Breakdown Voltage	ID=250uA, VGS=0V		30			V
IDSS	ZeroGate Voltage Drain Current	VDS=20V, VGS=0V				1	μA
			TJ=55°C			5	
IGSS	Gate-Body leakage current	VDS=0V, VGS=±20V				100	nA
VGS(th)	Gate Threshold Voltage	VDS=VGS, ID=250μA		1	1.4	2.5	V
ID(ON)	On state drain current	VGS=10V, VDS=5V		150			A
RDS(ON)	Static Drain-Source On-Resistance	VGS=10V, ID=30A			5	6	mΩ
			TJ=125°C		7.5		
		VGS=4.5V, ID=20A			7.6	9.5	mΩ
gFS	Forward Transconductance	VDS=5V, ID=10A			49		S
VSD	Diode Forward Voltage	IS=1A, VGS=0V			0.74	1	V
IS	Maximum Body-Diode Continuous Current					50	A
DYNAMIC PARAMETERS							
Ciss	Input Capacitance	VGS=0V, VDS=12.5V, f=1MHz			2050	240	pF
Coss	Output Capacitance				485		pF
Crss	Reverse Transfer Capacitance				280		pF
Rg	Gate resistance	VGS=0V, VDS=0V, f=1MHz			0.86	1.5	Ω
SWITCHING PARAMETERS							
Qg(10V)	Total Gate Charge	VGS=10V, VDS=12.5V, ID=20A			34	41	nC
Qg(4.5V)	Total Gate Charge				17	22	
Qgs	Gate Source Charge				5		nC
Qgd	Gate Drain Charge				3.5		nC
tD(on)	Turn-On DelayTime	VGS=10V, VDS=12.5V, RL=0.6Ω,RGEN=3Ω			7.5		ns
tr	Turn-On Rise Time				11		ns
tD(off)	Turn-Off DelayTime				27		ns
tf	Turn-Off Fall Time				8		ns
trr	Body Diode Reverse Recovery Time	IF=20A, dI/dt=100A/μs			30	36	ns
Qrr	Body Diode Reverse Recovery Charge	IF=20A, dI/dt=100A/μs			19		nC

A. The value of R θJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T A =25° C. The Power dissipation PDSM is based on R θJA and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175° C may be used if the PCB allows it.

B. The power dissipation PD is based on TJ(MAX)=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature TJ(MAX)=175° C.

D. The R θJA is the sum of the thermal impedence from junction to case R θJC and case to ambient.

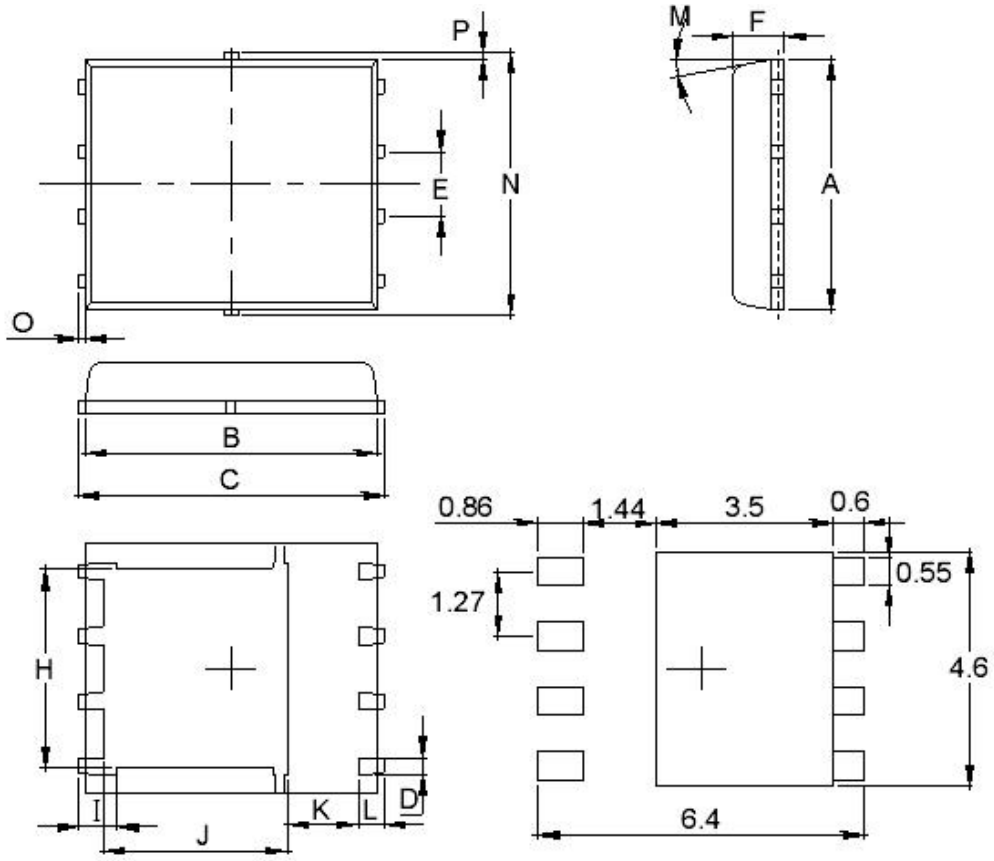
E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of TJ(MAX)=175° C.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA=25° C. The SOA curve provides a single pulse rating.

Product dimension(PDFN5X6)



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

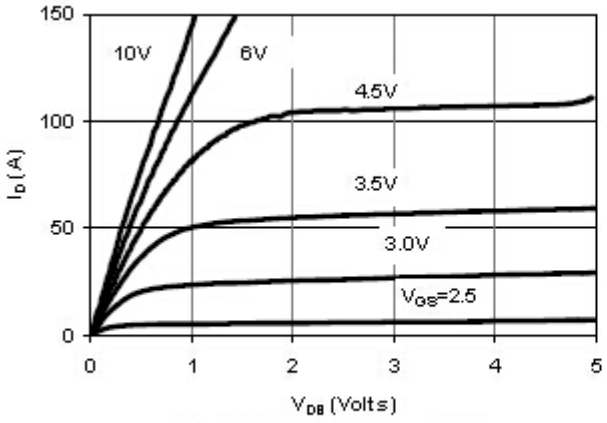


Fig 1: On-Region Characteristics

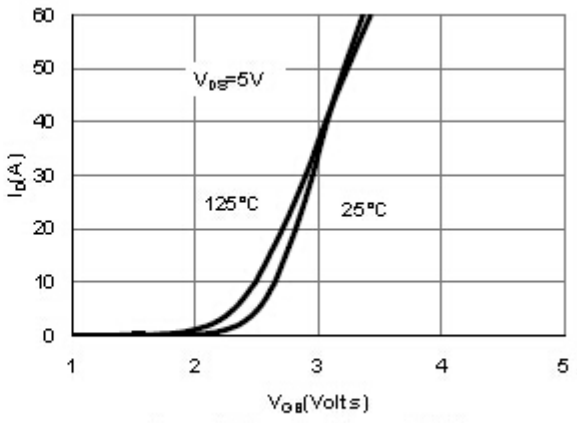


Figure 2: Transfer Characteristics

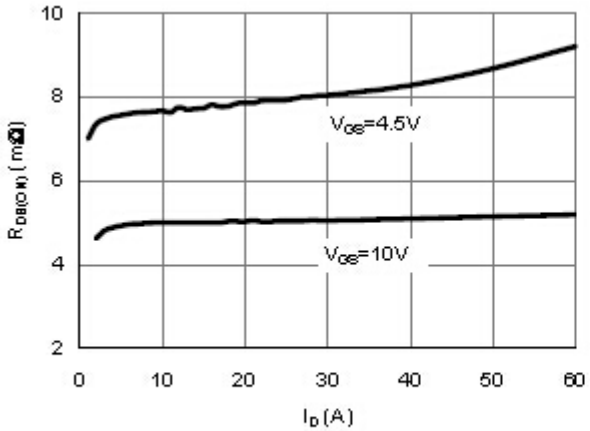


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

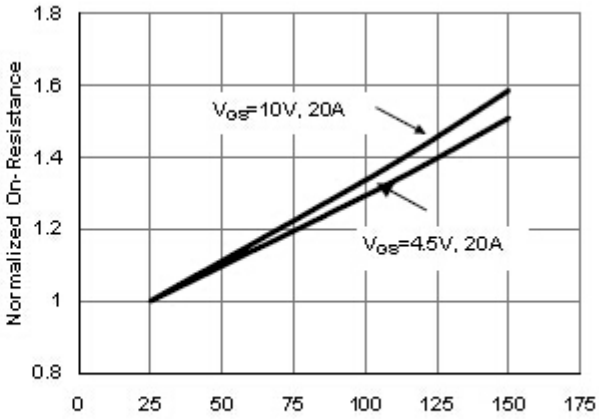


Figure 4: On-Resistance vs. Junction Temperature

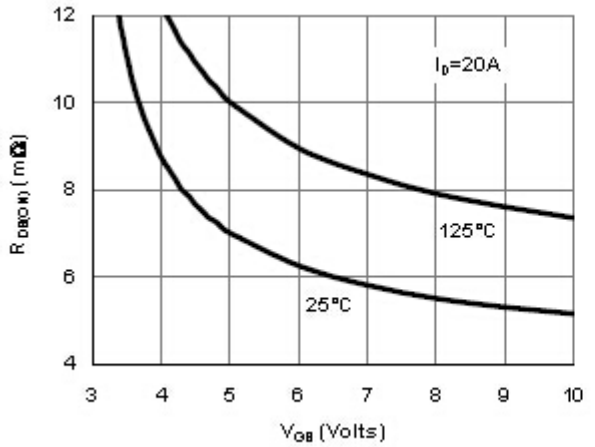


Figure 5: On-Resistance vs. Gate-Source Voltage

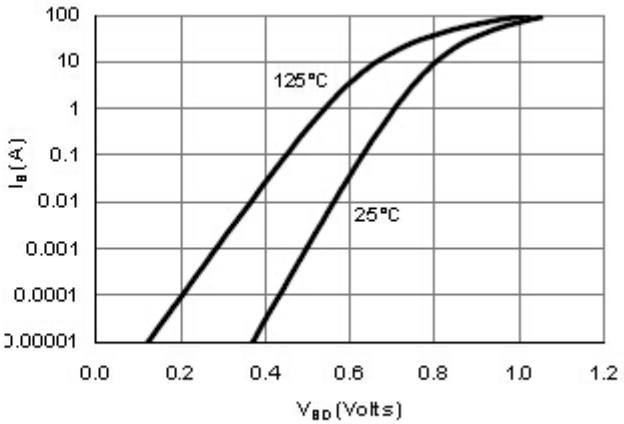


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

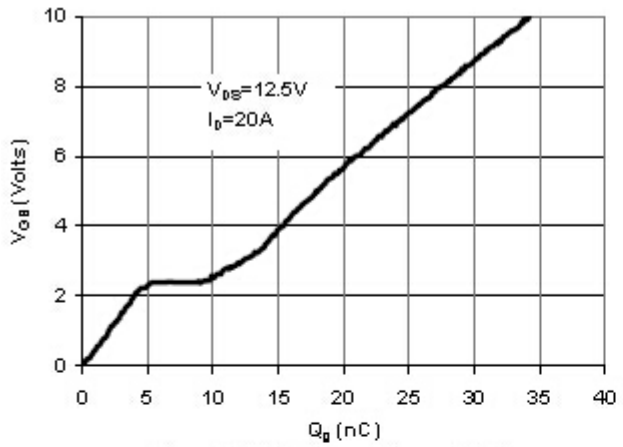


Figure 7: Gate-Charge Characteristics

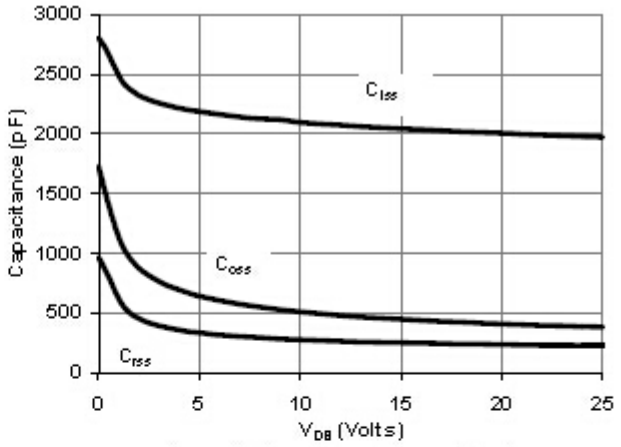


Figure 8: Capacitance Characteristics

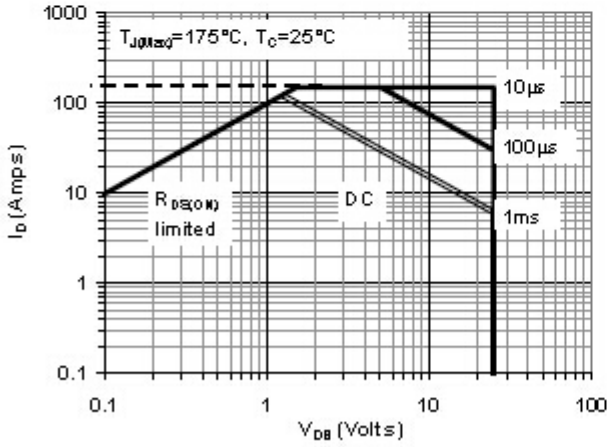


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

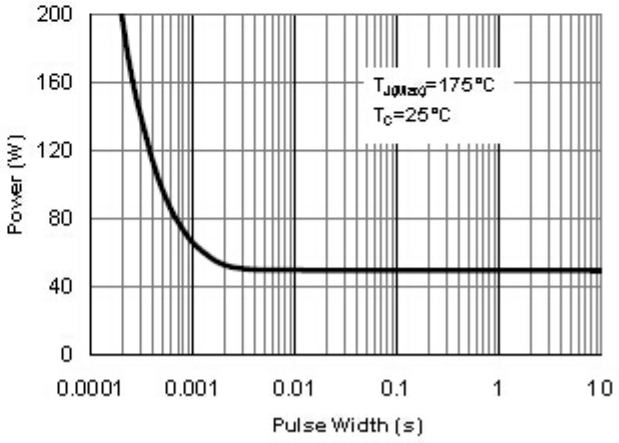


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

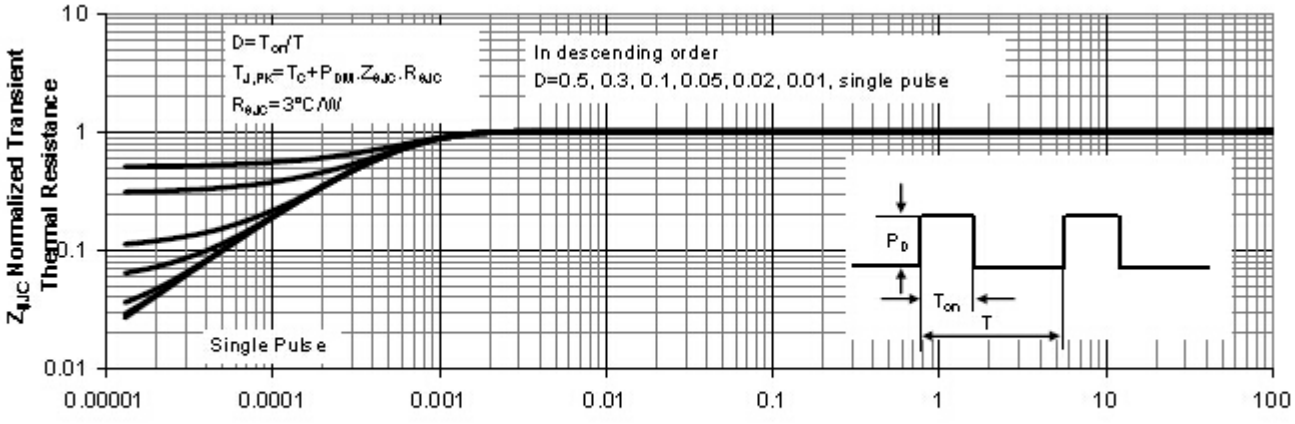


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

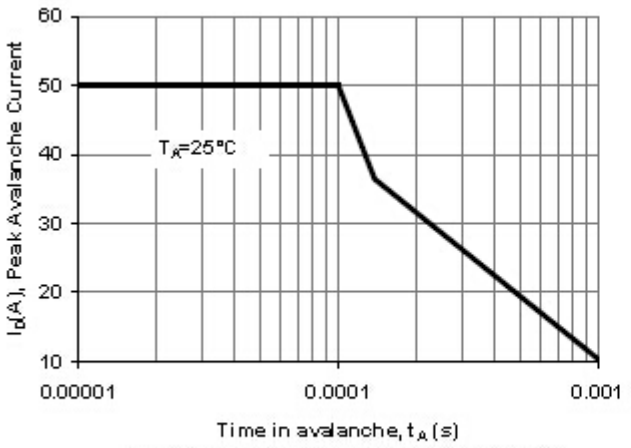


Figure 12: Single Pulse Avalanche capability

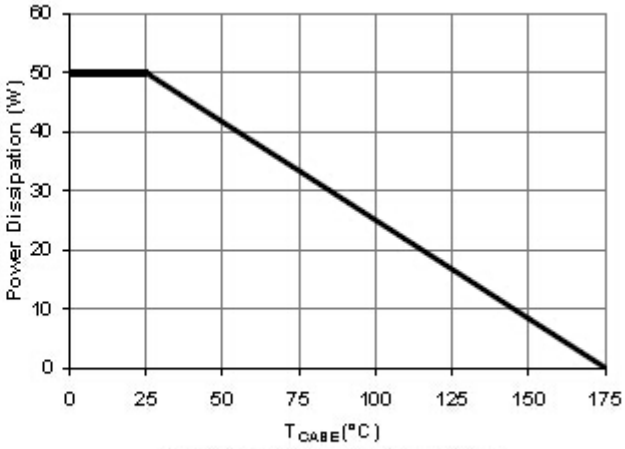


Figure 13: Power De-rating (Note B)

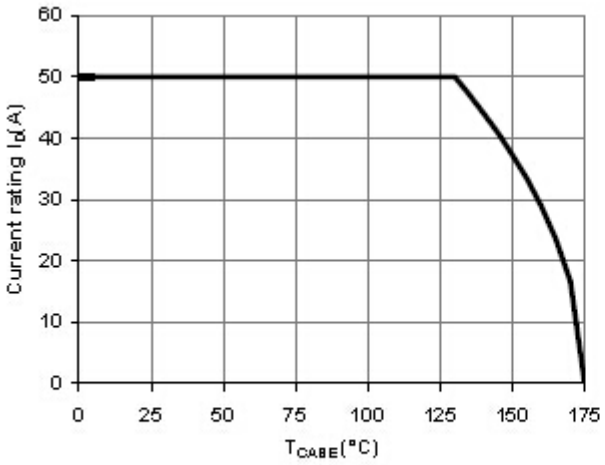


Figure 14: Current De-rating (Note B)

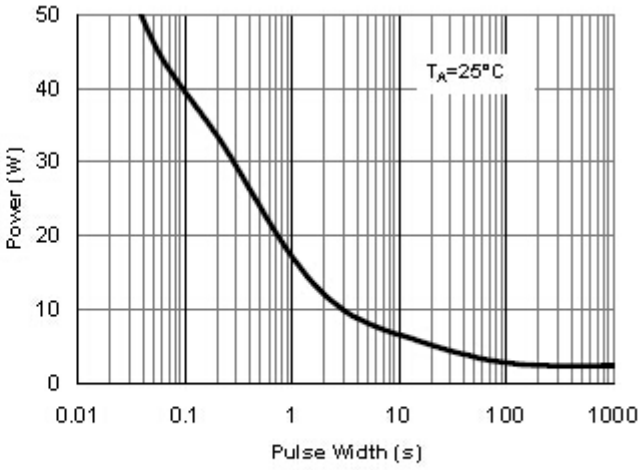


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

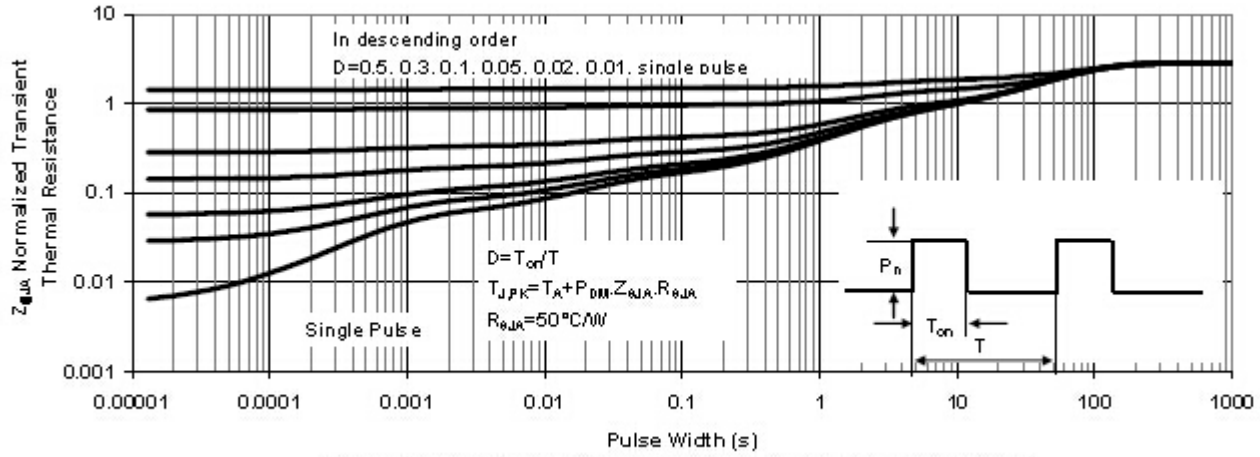


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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