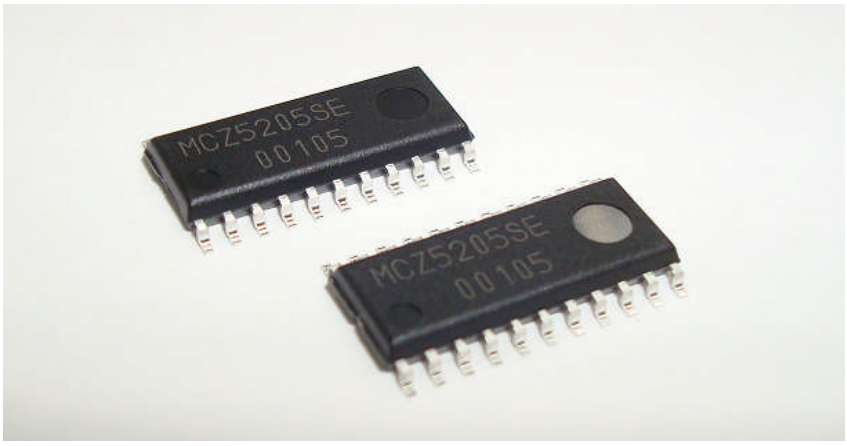
SHINDENGEN

Transition mode PFC &
High Peformance Symmetric
LLC controller

PFC / LLC Green combo

MCZ5205SE



Application Note ver. 1.0en

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1 General description

The MCZ5205SE adopts one chip solution to provide CrM PFC and LLC controller/driver in small package. This robust combo-IC eliminates external components for protective function and its multi functional terminal configuration simplifies power supply designing by using minimal components.
Active standby function provides improved efficiency at light load condition.
CrM PFC and Symmetric LLC combination provides excellent performance in low noise characteristics and also highly efficient power supply solution.

The MCZ5205SE is most suitable for:

- FPD PSU (LCD / PDP / Projection)
- OA equipment PSU (LBP …etc.)
- High power adapter
- High power industrial equipment
- High power LED lighting driver

1.1 Features

1. PFC and LLC controllers are integrated in SOP22 package.
2. Active standby function improves efficiency at light load condition.
3. PFC adopts OVP multi-detective function to simplify the circuit.
4. Optimized PFC/LLC on-off timing.
5. Vcc up to 35V with 12.6 / 8.5V UVLO.

[PFC]

1. Critical conduction mode PFC controller.
2. Peak current limiting threshold of 0.5V.
3. No input line sensing is required.
4. Various protections are installed. (feedback pin open/short, dynamic OVP, Thermal shutdown)

[LLC]

1. Optimized Gate drive balance simplifies drive circuitry.
2. 600V floating gate drivers with individual UVLO.
3. Active standby operation eliminates a weak point of symmetric LLC that is unsatisfactory efficiency at light load condition.
4. Anti-capacitive protection
5. Various protections are installed. (Peak current limit / Timer delayed latching / Thermal shutdown)

1.2 Internal block diagram

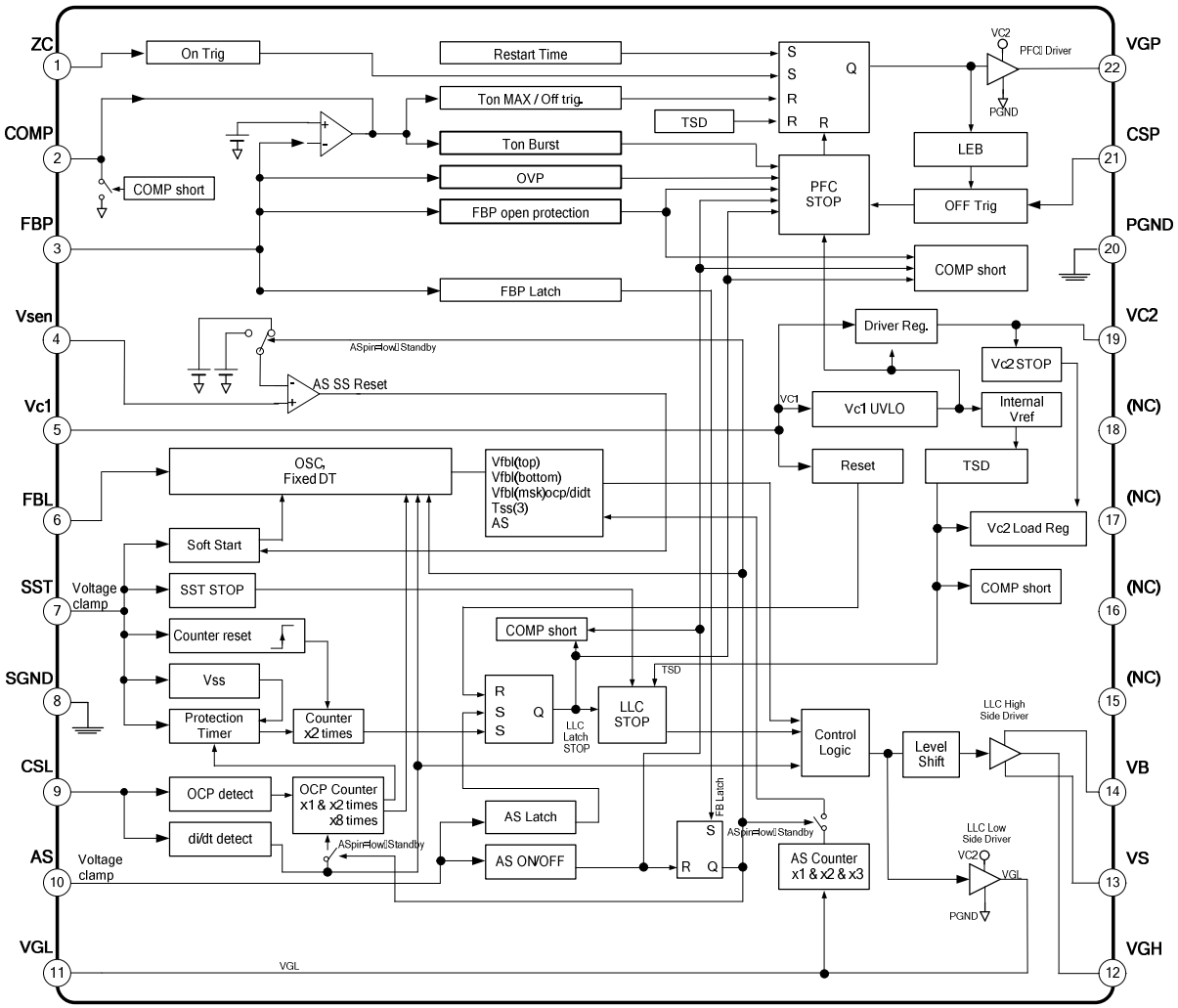


Fig.1 MCZ5205SE internal block diagram

1.3 Pin assignment

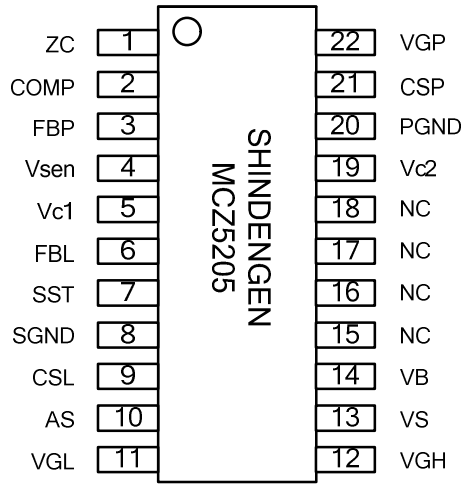


Fig.2 MCZ5205SE Pin assignment

1.4 Functions

PIN NO.	symbol	converter	Function
1	ZC	PFC	**Z**ero **C**urrent detection to determine turn on timing
2	COMP	PFC	Output of PFC feedback amp for phase **COMP**ensation and soft start
3	FBP	PFC	Input of **P**FC **F**eed**B**ack amp
4	Vsen	LLC	Line **V**oltage **sen**sing for brownout protection
5	Vc1	Common	Voltage source input for control circuit with 12.6V/8.5V UVLO
6	FBL	LLC	**L**LC operating frequency and duty setting **F**eed**B**ack terminal
7	SST	LLC	**S**oft **S**tart and protection **T**imer
8	SGND	Common	**S**ignal **GND** terminal
9	CSL	LLC	**L**LC resonant **C**urrent **S**ensing
10	AS	Common	Terminal for **A**ctive **S**tandby mode / external latch signals input
11	VGL	LLC	**G**ate drive output for **L**ow side mosfet
12	VGH	LLC	**G**ate drive output for **H**igh side mosfet
13	VS	LLC	Floating high side gate driver reference voltage (: connect with **S**ource terminal of high side mosfet)
14	VB	LLC	Floating Vcc **B**ootstrapping input
15-18	NC	-	Non connection
19	Vc2	Common	Output terminal of supply for PFC and LLC driver
20	PGND	Common	**P**ower **GND**
21	CSP	PFC	**P**FC mosfet source **C**urrent **S**ensing
22	VGP	PFC	**G**ate drive output for **P**FC mosfet

1.5 Application circuits

Fig.3 Basic circuit example

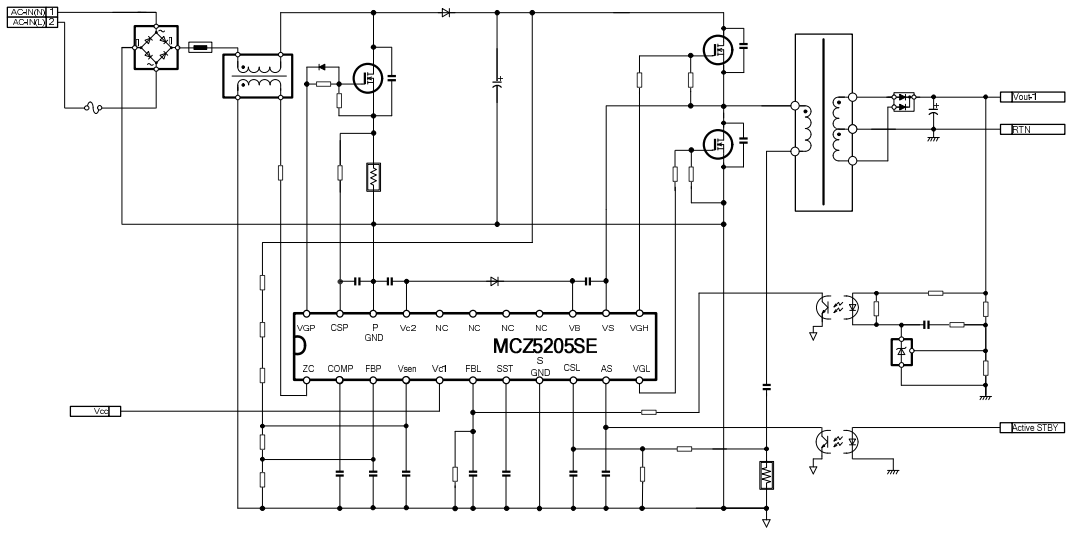
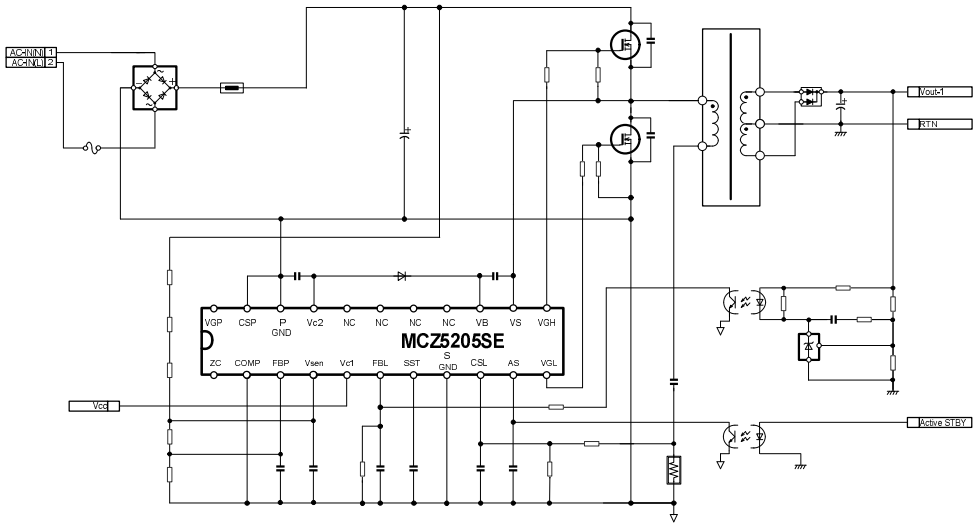


Fig.4 Basic circuit example (Without PFC)



2 Functional description

Values described in this document such as Threshold are typical, unless otherwise specified.
For details, please refer to characteristic specification.

2.1 Outline

The functionality of the MCZ5205SE can be grouped as follows:

1) Power supply
For details, refer Section **2.2**.

2) PFC Controller
For details, refer Section **2.3**.

3) LLC Controller
For details, refer Section **2.4**.

4) Others (Active Standby, Common Protection)
For details, refer Section **2.5**.

2.2 Power supply block

2.2.1 Power supply for controller (Vc1)

Vc1 is power supply input terminal for controller. Connect a capacitor between Vc1 and GND close to the terminals to supply stable voltage.
Select the capacitance value to stabilize transient conditions. (For example, start up and shut down.)
If malfunction of MCZ5205SE occurs due to noise on **Vc1**, insert a **MLCC** of 1 to 4.7uF between Vc1 and GND close to the terminal.

If **Vc1** voltage reaches **Vc1(start) 12.6V**, **Vc2** start charging. If **Vc1** voltage falls below **Vc1(stop) 8.5V**, **Vc2** starts discharging and controller stops its operation. If the latch-stop works due to an abnormal state, it is necessary for restarting to release the latch by reducing Vc1 voltage to less than latch reset voltage of **Vc1(latch reset) 8.1V**.

2.2.2 Power supply for gate driver (Vc2)

Vc2 is output terminal of supply for PFC and LLC driver. **Vc2** supplies stable voltage to gate drivers of PFC and LLC controllers. Connect a capacitor between **Vc2** and **GND** close to the terminals to secure the stable driving in general and also transient conditions such as start up and shut down. Capacitance of **4.7 to 22uF** is recommended.

When **Vc2** voltage reaches **Vc2(start) 9.6V**, oscillator (connected with **FBL**) starts operation and driving is ready. Refer to section **2.3** and **2.4** for the condition to start gate driving of PFC and LLC controllers.

2.2.3 Power supply for LLC High-side gate driver (VB)

VB is output terminal of supply for **LLC** high-side driver. **VB** is connected with **Vc2** via the bootstrap diode. Connect a capacitor between **VB** and **VS**. Select a capacitor with considering stable driving in transient conditions such as start up and shut down. Capacitance of **0.1 to 0.47uF** is recommended.
Bootstrap diode requires fast and soft recovery characteristics. For example, select a diode of 600V or higher when PFC output voltage is 400V. **D1NK60**(Shindengen) is recommended.

VB is equipped with an independent UVLO (under voltage lock out). If **VB** voltage reaches **VB-VS(start) 7.4V**, high-side gate driving starts. If VB voltage falls below **VB-VS(stop) 5.3V**, high-side gate driving stops. This hysteresis provides stable driving at transient condition of start up and shut down.

2.3 PFC block

2.3.1 PFC gate driver (VGP)

VGP drives a gate of PFC, and the voltage is supplied by stabilized voltage source **Vc2**,10.2V.

Fig. 5 shows some examples of the drive circuit.
In typical circuits shown in **A)** and **B)**, Select the small type Schottky Barrier Diode, not hard recovery diodes. **D1NS4** or **M1FM3** (Shindengen) is recommended.

In case of using a MOSFET with large Qg, use PNP transistor as shown in **Fig. 5 C)**.

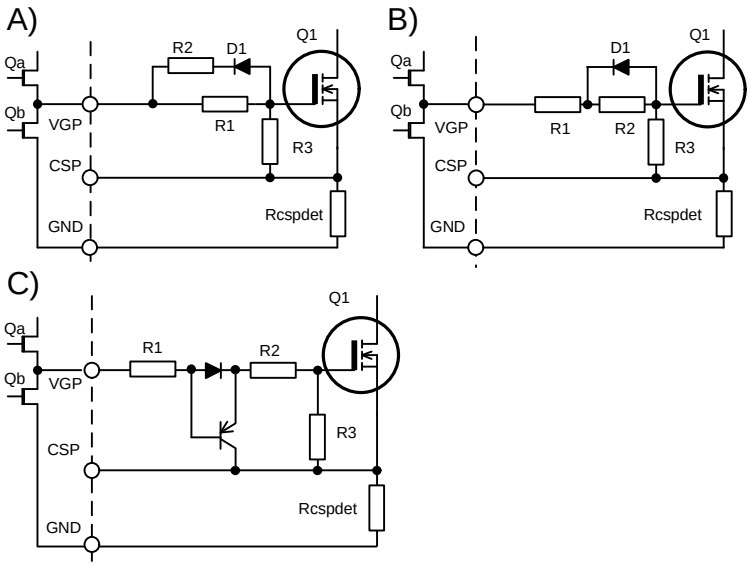


Fig.5 PFC gate drive circuit

2.3.2 PFC output voltage control and over-voltage protection

PFC output voltage is stabilized by controlling the On-duty of PFC gate driving.
Shown in **Fig.6**, PFC output voltage is monitored by **FBP**, and is stabilized by feeding-back the **FBP** voltage by comparison with internal reference voltage **Vo(ref), 2.5V**.
COMP controls charge and discharge so that **FBP** voltage becomes 2.5V, consequently PFC output voltage becomes stable.
(**FBP** voltage<2.5V --> **COMP** capacitor charges. and **FBP** voltage>2.5V --> **COMP** capacitor discharges.)

PFC has an over-voltage protective function to protect components (e.g. capacitors) from damage due to excessive voltage. If **FBP** voltage exceeds **Vfb(H)**, that is **Vo(ref)×1.10**, the gate driving stops (not latch-stop).

Connect a capacitor of around **1000pF** between **FBP** and **GND** close to the terminals for noise reduction.

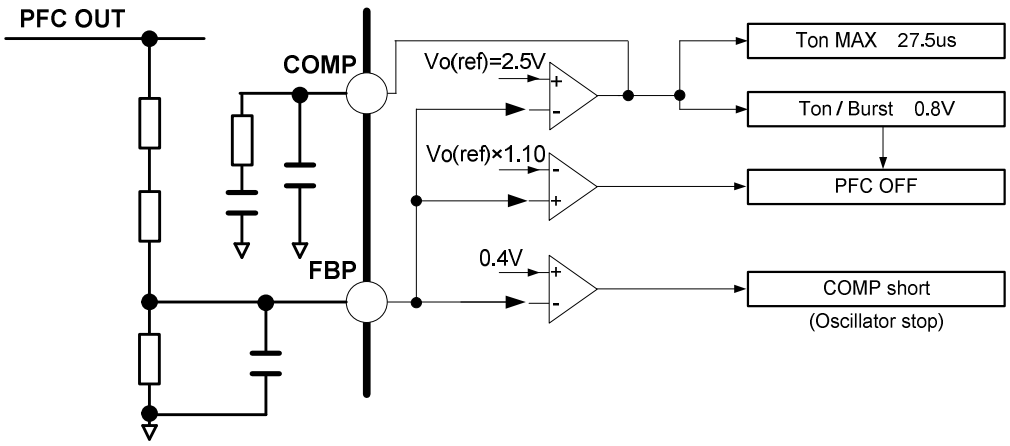


Fig.6 PFC gate drive circuit

2.3.3 PFC phase compensation

COMP is feedback amplifier output terminal. Phase compensation is adjusted by capacitor of **0.1-1.0uF** connected between **COMP** and **GND**.
Fig. 7 shows an example of the **COMP** phase compensation. For details of phase adjustment, refer to section **3.2**.

The relationship between **VGP** ON-time and **COMP** voltage is shown in **Fig. 8**.
Maximum ON-time is fixed as **Ton(max) 27.5us**. When **COMP** voltage decreases to **0.8V** or less, On-time becomes zero, consequently to prevent the increase of output voltage.

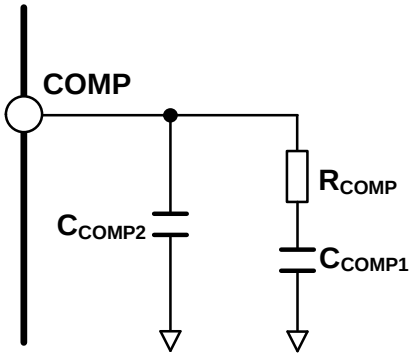


Fig.7 Example circuit connected with COMP

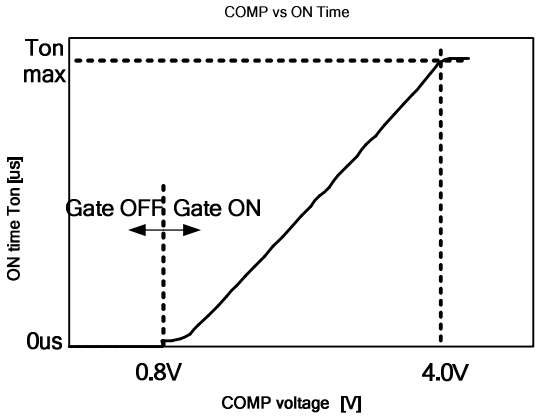


Fig.8 COMP VS ON Time

2.3.4 PFC critical conduction mode

PFC block adopts critical conduction mode. PFC MOSFET turns ON by detecting the voltage across a control winding of main choke. Gate ON timing is determined by **ZC** signal as shown in **Fig.9**.

Once VZC reaches **ZC** comparator threshold voltage(H) **V_{ZC}(H), 1.55V**, and then decreases beyond **ZC** comparator threshold voltage(L) **Vzc(L), 0.55V**, MOSFET turns ON by detecting the negative edge.
This hysteresis (:VZC(H) – VZC(L)) provides the higher noise immunity.

Ton dead time of **800ns** is adopted in order to prevent malfunction of MOSFET caused by ringing voltage at the timing of gate-OFF.

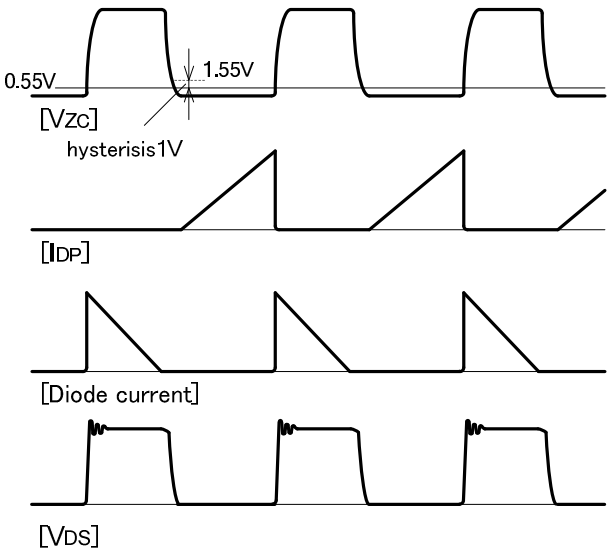


Fig.9 PFC block timing diagram (ZC)

Insert a limiting resistor between control winging and **ZC**. This resistance has following two roles.

1. Turn on the gate at the lowest point of the Drain-Source voltage of MOSFET.
2. The resistor limits the current on **ZC** to +/-5mA or less, that is maximum allowable current on **ZC**.

2.3.5 PFC over current protection

PFC over current protection is provided by monitoring the **CSP** voltage determined by resistors . Connected between source of PFC MOSFET and GND. MOSFET turns OFF by detecting **CSP** voltage exceeding the over-current threshold voltage as shown in **Fig.10**.
To prevent malfunction of over-current protection caused by noise just after turn ON, Leading edge blank time (LEB) is adopted.

Connect a capacitor of around **0.1uF** close to **CSP** to prevent malfunctions due to noise.
Adding a resistor $\mathbf{R_{CSP2}}$ of around 10ohm is more effective for the prevention.

For designing the circuit, refer to section **3.4**.

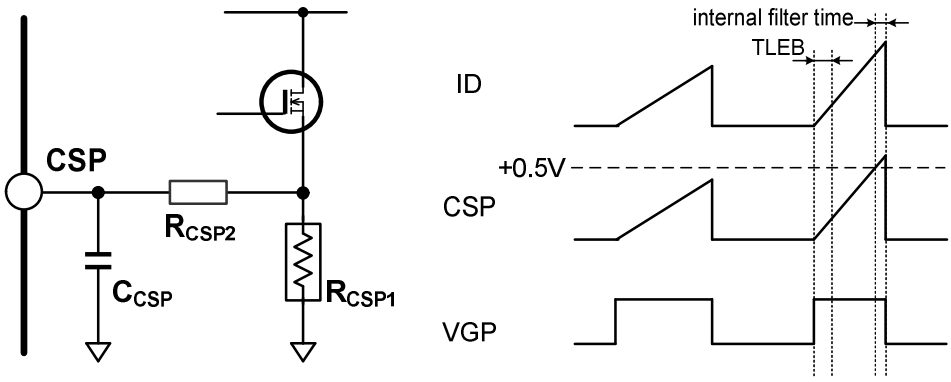


Fig.10 CSP circuit example and timing diagram

2.3.6 PFC FBP open/short protection

If **FBP** voltage decreases to **Vfb(L) 0.4V** or less, PFC stops operation.
Therefore, if **FBP** is shorted circuit to **GND**, PFC safely stops operation.

PFC also stops operation on condition of **FBP** open circuit, as **FBP** voltage to zero.

2.3.7 PFC low input voltage protection

The **MCZ5205SE** does not directly monitor the input voltage. Therefore, if **FBP** voltage exceeds 0.4V even in low input voltage condition, PFC continues the operation.
However, **MCZ5205SE** has the limiting function for maximum ON-time internally fixed as **27.5us**. decreases output current to prevent the excessive stress on MOSFET or other components.

2.3.8 PFC output over voltage protection (light load)

At light load condition, the output voltage is stabilizes by narrowing the ON-time width of gate driving. However, in the case where the output voltage increases even if the ON-time width reaches the minimum set value, a function that the oscillation stops where COMP voltage decreases to **$V_{th(burst)}$, 0.8V** or less operates to prevent the over voltage of output.

2.4 LLC block

2.4.1 LLC gate driver (VGL,VGH)

The gate drivers have 0.18A sourcing and 0.38A sinking current capability at **Vc2=10.2V**.
Typical example circuits are shown in **Fig.11 A)**. When using a diode for discharging as shown in **Fig. 11 B) C)**, small type SBD(Schottky Barrier Diode). **D1NS4**(Shindengen) or **M1FM3**(Shindengen) are recommended.

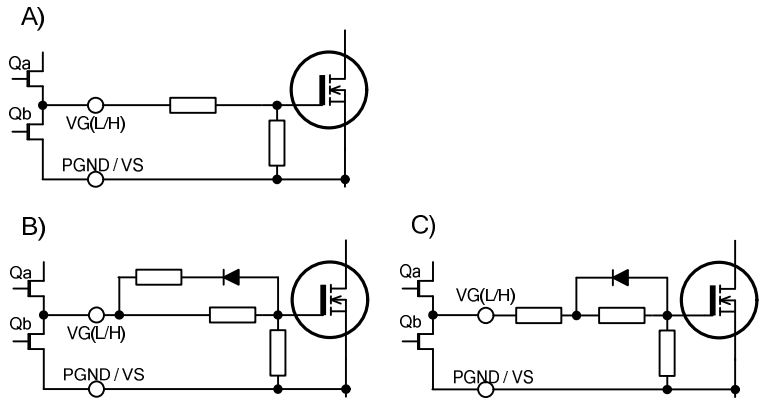


Fig.11 LLC Gate drive circuits

2.4.2 LLC Oscillator (FBL)

The timing of gate drive pulse **VGL** and **VGH** is determined by charging and discharging of a timing capacitor **Ct**. (The timing capacitor **Ct** is connected with **FBL**.)
Gate outputs are ON during the period of **Ct** discharging. **VGL** and **VGH** are alternately outputted to drive MOSFETs. During the time period of **Ct** charging, both VGL and VGH are simultaneously OFF, called as Dead time (DT), to prevent simultaneously ON of MOSFETs.

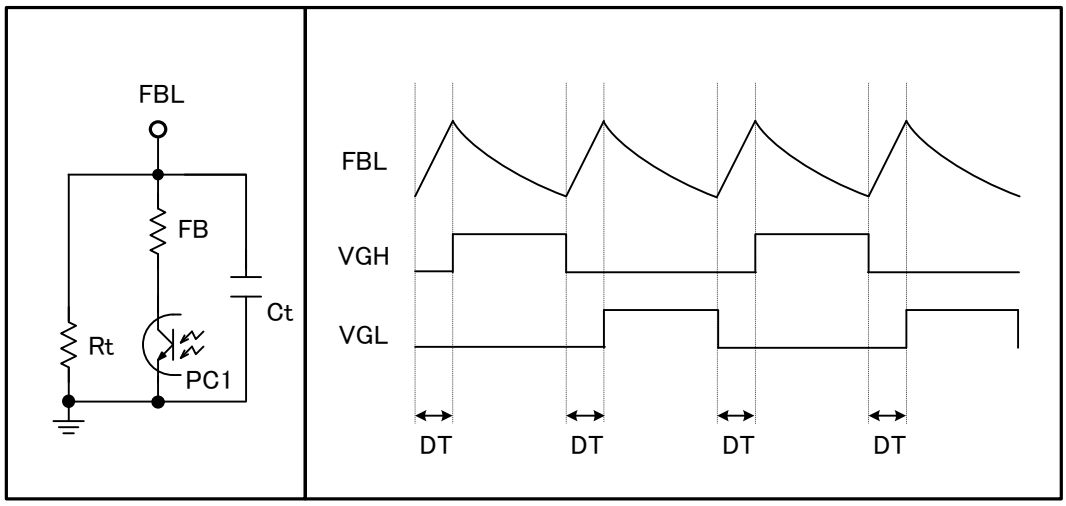


Fig.12 FBL timing diagram

The **MCZ5205SE** is the frequency and ON duty modulation type. The frequency modulates by **FB** current across a current limiting resistor and ON-duty modulates according to the frequency as shown in **Fig. 13**.
Larger dead time in light load condition secures ZVS (Zero Voltage Switching) over a wide frequency range.

Minimum frequency (**fmin**) is determined by the value of **Ct** capacitor and **Rt** resistor.

Maximum frequency (**fmax**) is determined by the value of **Rt** resistor and **FB** resistor.
Maximum frequency (**fmax**) of 300kHz or less is recommended in continual operating condition.
Soft start oscillation frequency (**fss**) varies depending on the value of **Ct** capacitance. (For details, refer to characteristic diagram sheet.)

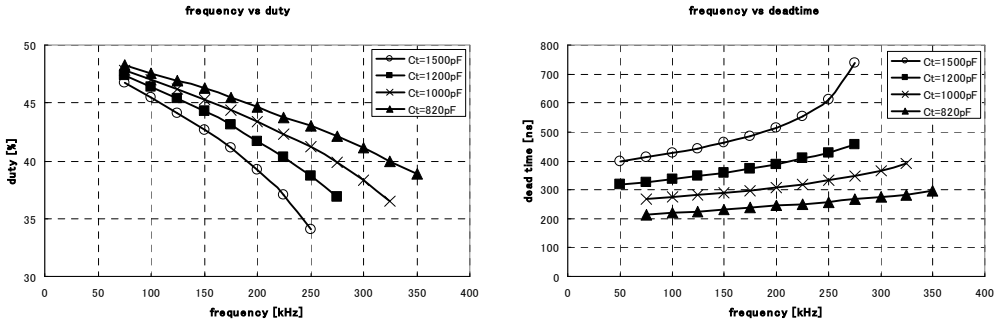


Fig.13 Duty/dead time vs frequency

2.4.3 Vsen brown-out protection (Vsen)

Vsen monitors the PFC output voltage for halting gate drive pulse, varying the frequency. UVLO function avoids below-resonant state caused by Vbulk supply brown-out (quick decrease of input voltage) or black-out (instantaneous interruption).

Timing diagram of **Vsen** brown-out protection is shown in **Fig.14**.

Vsen threshold voltage varies depending on AS mode ON or AS mode OFF. (See section **2.5.1**)
(1) **AS mode OFF** : Vsen1(ss-reset) **3.55V** / Vsen2(ss-reset) **3.25V**
(2) **AS mode ON** : Vsen3(ss-reset) **1.00V** / Vsen4(ss-reset) **0.90V**
Hysteresis characteristics of **Vsen** prevents malfunction of Vsen due to the PFC output voltage ripple.

[Power ON]

(a) **Vsen** voltage exceeds to **3.55V** (AS mode OFF), **SST** capacitor starts charging.
(b) **SST** voltage exceeds to **0.6V**, LLC gate output is starts.
SST is the soft start operated by gradual charging of **SST** capacitor. (For details of **SS**T, refer to section **2.4.4**.)

[Power OFF]

(a) **Vsen** voltage decreases to **3.25V** (AS mode OFF), **SST** capacitor starts discharging. Frequency gradually increases.
(b) **SST** voltage decreases to **0.5V**, LLC gate output stops.

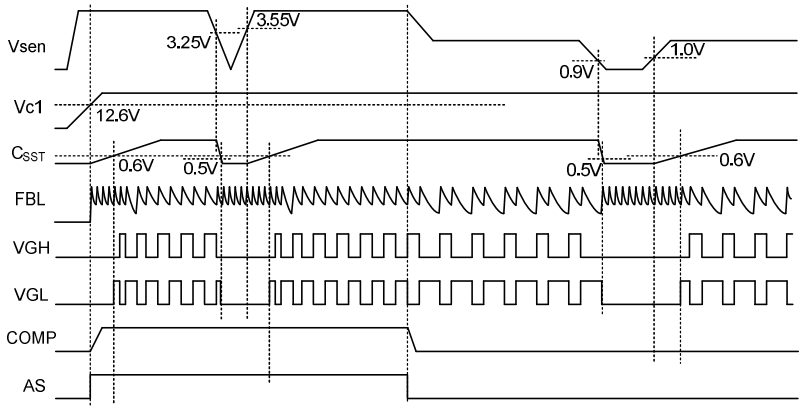


Fig.14 Vsen output timing diagram

2.4.4 Soft start function (SST)

LLC unit has soft-start function. The frequency gradually decreases according to charging of capacitor connected between **SST** and **GND**. **SST** capacitor starts to be charged subject to following two conditions.

(1) **Vc1** voltage exceeds startup threshold voltage **Vc1(start) 12.6V**
(2) **Vsen** voltage exceeds **3.55V** (at AS mode OFF) or **1.00V** (at AS mode ON).

LLC gate output starts when **SST** voltage exceeds **0.6V**, and then **SST** voltage is stabilized in **2.1V**.
LLC gate output stops if SST voltage decreases to **0.5V** or less.
For the relationship between **SST** voltage and frequency, refer to **Fig. 15**.

In addition, **SST** equips a timer latch function to decrease the stress on MOSFETs and/or peripheral components in abnormal conditions.
For details, refer to section **2.4.8**.

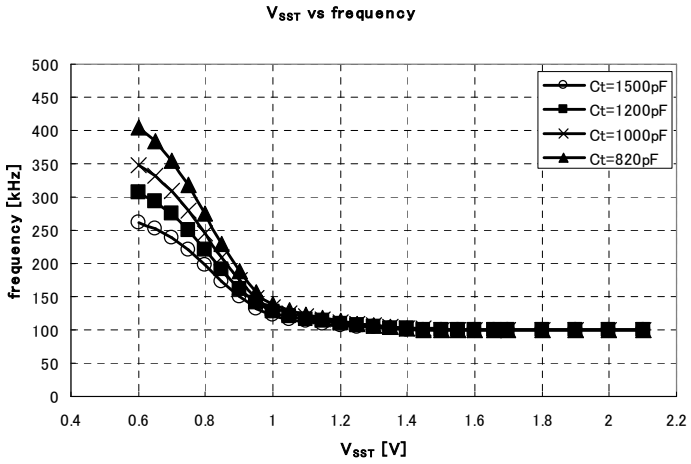


Fig.15 fss characteristics

2.4.5 Over current protection (CSL)

OCP (over current protection) operates by detecting peak current of resonant tank with pulse by pulse at **CSL**. The detection threshold voltage is **+/-0.350V** (**OCP** input threshold voltage.) and is low enough to minimize ineffective power loss of sensing resistor.

When **CSL** voltage exceeds **OCP** input threshold voltage, the gate output turns off and **FBL** capacitor immediately starts charging and simultaneously charging **SST** capacitor, and consequently output current is limited with pulse by pulse. (See **Fig. 16**.)

In next cycle just after **OCP** detection, **FBL** capacitor stops discharging when **FBL** bottom voltage reaches **1.9V**, thus, ON-time is limited to avoid below-resonant. (See **Fig. 16**.)

Note that di/dt threshold is about 1/6 of **OCP** threshold.

In order to prevent malfunction of **OCP** due to switching noise induced by MOSFET, **OCP-mask** period is adopted as shown in **Fig.16**. During the **OCP-mask** period, **OCP** detection does not work (period of **FBL(TOP)** to mask voltage, **2.8V**).
A filter is built-in in **CSL** to prevent malfunction due to random noise, and the filter causes delay time of around 200ns, that is the period of **OCP** detection to **FBL** starting to charge.

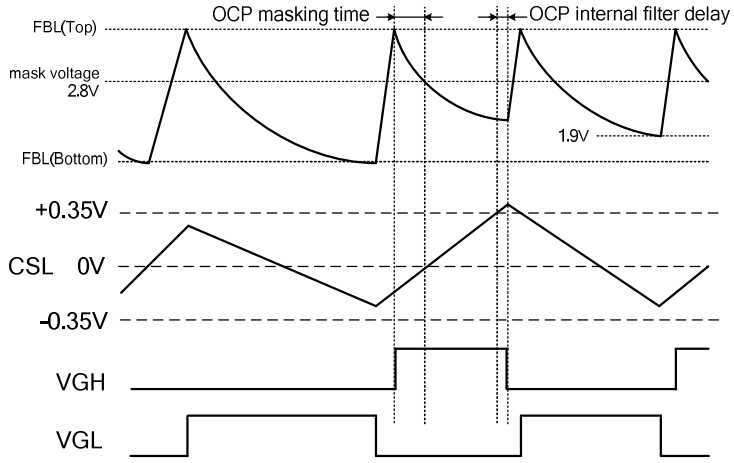


Fig.16 Over current protection

2.4.6 di/dt mode protection (CSL)

The **MCZ5205SE** adopts pulse by pulse bidirectional di/dt protection to avoid below resonant mode operation.
This function helps to avoid di/dt hard switching mode of MOSFETs in below ZVS boundary operation.
When **CSL** voltage decreasing to **60mV,** instantaneously **FBL** starts charging and gate drive turns off. In negative current direction, it operates in the same manner with threshold voltage of **-60mV**.

Di / dt charge timer operation varies depending on **AS** mode ON or **AS** mode OFF. (See section **2.5.1**)
(1) **AS** mode OFF : timer capacitor is not charged.
(2) **AS** mode ON : timer capacitor is charged.

During **OCP-mask** period (**FBL(Top)** to mask voltage, **2.8V**), di/dt detection does not work to prevent the malfunction due to noise.

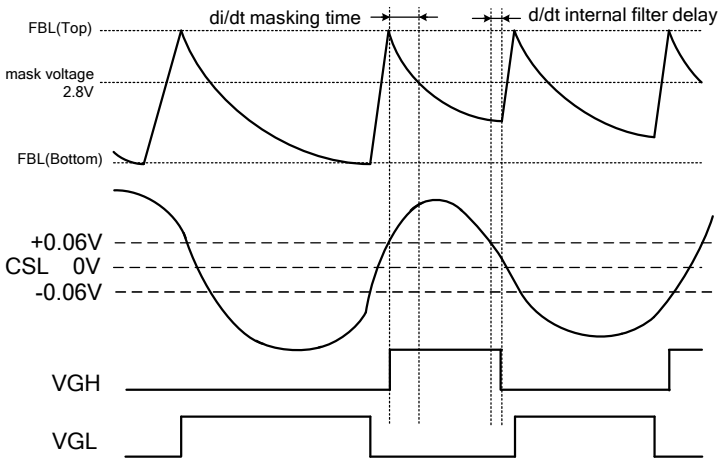


Fig.17 di/dt protection

2.4.7 di/dt protection at startup (Tss(3))

The **MCZ5205SE** has another di/dt protection at startup state to prevent the turn-off of gate drive during period of body diode.
On 2nd **VGL** gate drive pulse, increase the ON-time width by decreasing the voltage to start charging to **0.8V**, consequently the gate drive turns-off after MOSFET current starts to flow.
The operation sequence is shown in **Fig.18**.

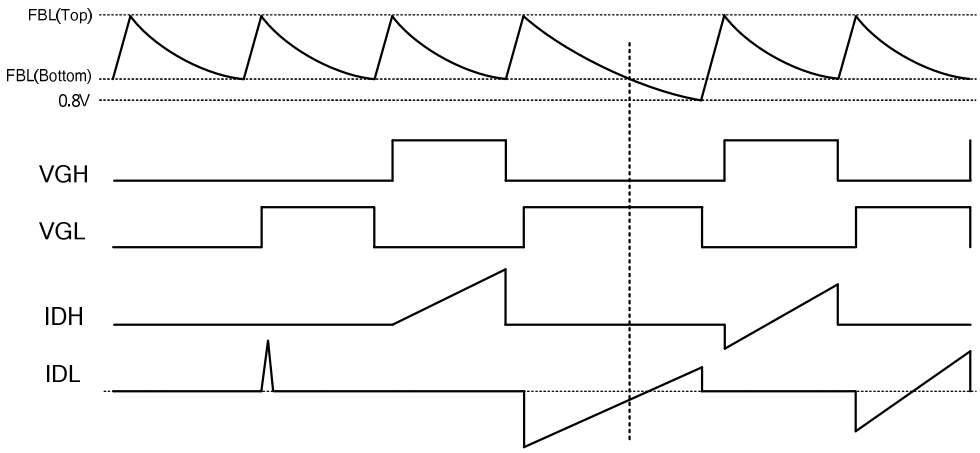


Fig.18 Tss(3) operating sequence

2.4.8 Timer latch protection (SST)

SST capacitor starts charging to either case below.

(1) **OCP** detection
(2) di/dt detection under **AS** mode ON

SST capacitor starts charging and continual abnormal condition keeps charging **SST** capacitor with **40uA** constantly until **SST** voltage reaches **3.6V**.
Once **SST** terminal voltage reaches **3.6V**, gate output stops and **SST** capacitor start discharging with **6uA** constantly until **SST** voltage decreases to **0.35V**. At the moment **SST** voltage reaches **0.35V**, **SST** capacitor restarts charging with **28uA** constantly, then, the soft start operation restarts.

Timer counter counts the number of times of **3.6V** charging. If count is twice, output latches off.
If abnormal condition is eliminated and the controller recovers normal operation before the two counts, **SST** capacitor starts discharging with **500uA** and the counting result is reset.
To release the latch, restart with **Vc1** less than **8.1V**.

Latch counter is reset by either condition below.

(1) **SST** voltage reaches **2.1V** by continual OCP detection.
(2) SS refreshing operation (Vc1 ON/OFF operation)

Timing chart is shown in **Fig.19**.

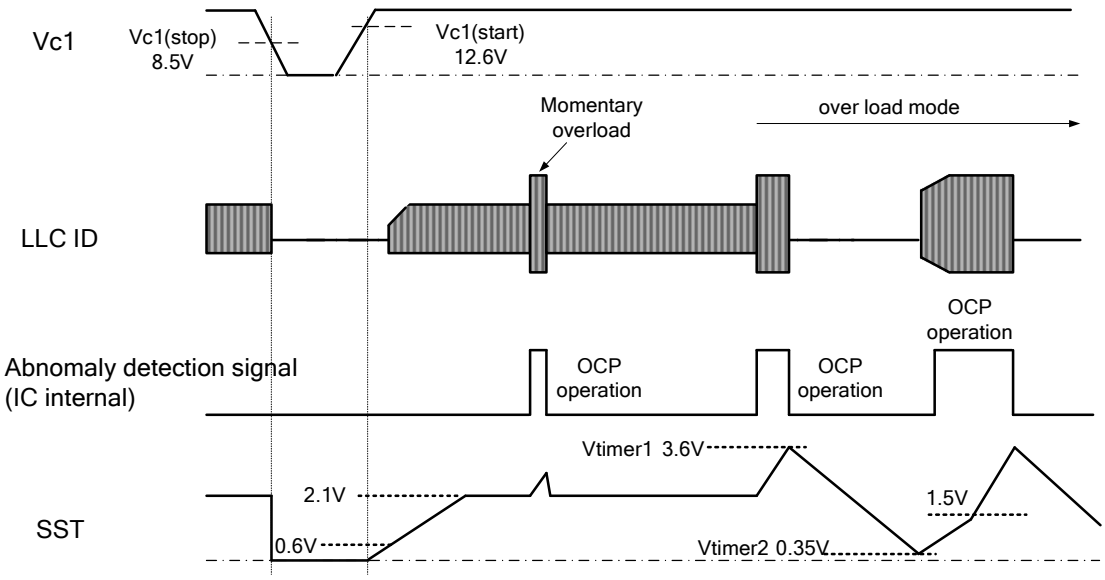


Fig.19 SST operating sequence

2.4.9 High side floating Vcc (VB)

Floating High side gate drive voltage source (**VB**) is produced by stabilized **Vc2** of **10.2V** through bootstrap circuit.

Recommended components at PFC output voltage of **400V** are :

600V soft recovery type UFRD (ultra fast recovery diode) **D1NK60** (Shindengen) or **D1FK60** (Shindengen) for D_{boot}

16V, **0.1** to **1.0uF** MCLL for C_{boot}

VB = Vc2 – Vf (Forward voltage of D_{boot})

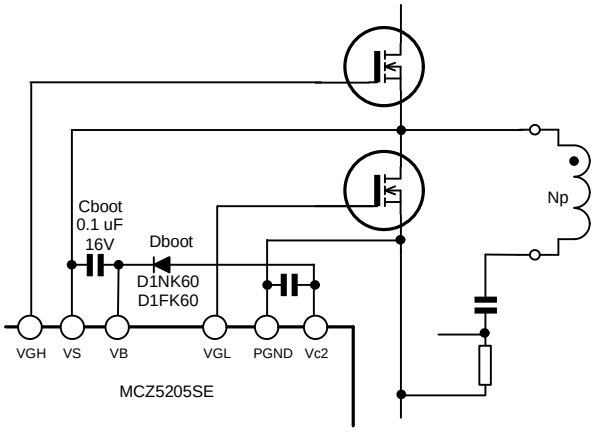


Fig.20 Boot Strapping configuration

2.5 Others

2.5.1 Active Standby (AS)

The **MCZ5205SE** adopts active standby function contributing to loss reduction at light load condition.
The example circuit is shown in **Fig. 21**.

Active standby function operates as below.

(1) AS mode ON : If AS voltage reaches **0.8V** or less.
(2) AS mode OFF : If AS voltage reaches **1.0V** or more.
(3) AS latch stop : If AS voltage reaches **4.5V** or more.
To release the latch, restart with **Vc1** of **8.1V** or less.

Connect a capacitor of **1000** to **10000pF** between **AS** terminals to prevent malfunction due to noise even where **AS** function is not used. Note that **AS** voltage is set to **2.4V** at **AS** load open.

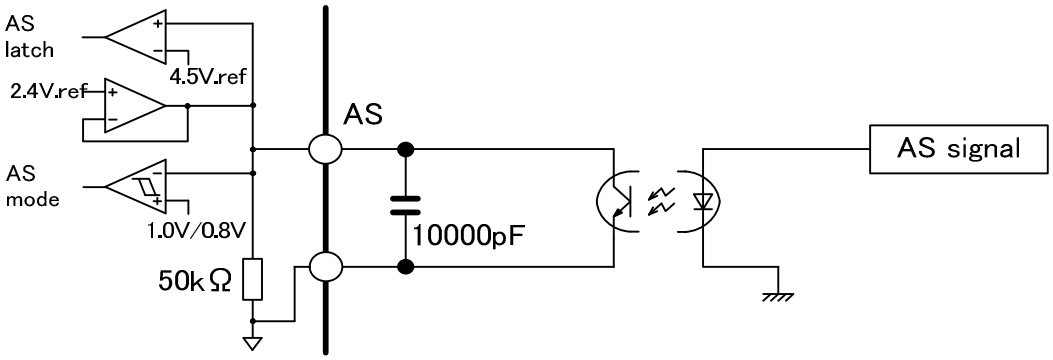


Fig.21 AS mode circuit example

Following operations are provided after shifting to **AS** mode.
For detailed timing diagram, refer to **Fig.22**.

(1) LLC operating mode : Switched from symmetric operation to asymmetric operation.
(2) Vsen SS-reset threshold : Switched from 3.55V/3.25V to 1.0V/0.9V.
(3) Timer charge (di/dt mode) : Switched from 'disable' to 'enable'.
(4) PFC operating mode : Switched from 'Oscillation start' to 'Oscillation stop'.

Asymmetric operation can lower the peak current at light load condition and PFC oscillation stops resulted in significant efficiency improvement at light load.

Vsen SS-reset threshold is automatically switched so that LLC oscillation continues even when the PFC oscillation stops.
This function does not require any additional components.

In addition, **AS** mode ON enables charging **SST** capacitor at di/dt mode to provide **OCP**.

Soon after switching from **AS** mode ON to **AS** mode OFF, **COMP** starts charging and PFC starts operation when **COMP** voltage reaches **0.8V** or more. Then, **FBP** voltage exceeds **2V** and **Vsen** SS-reset threshold switches, LLC operation mode switches to symmetric mode (normal operation mode).

AS has a latch stop function. If **AS** voltage exceeds **AS** latch stop voltage 4.5V,
PFC and LLC oscillation immediately stops unlike **SST** timer latch.
To release the latch, restart at **Vc1** of 8.1V or less.

Active Standby mode sequence

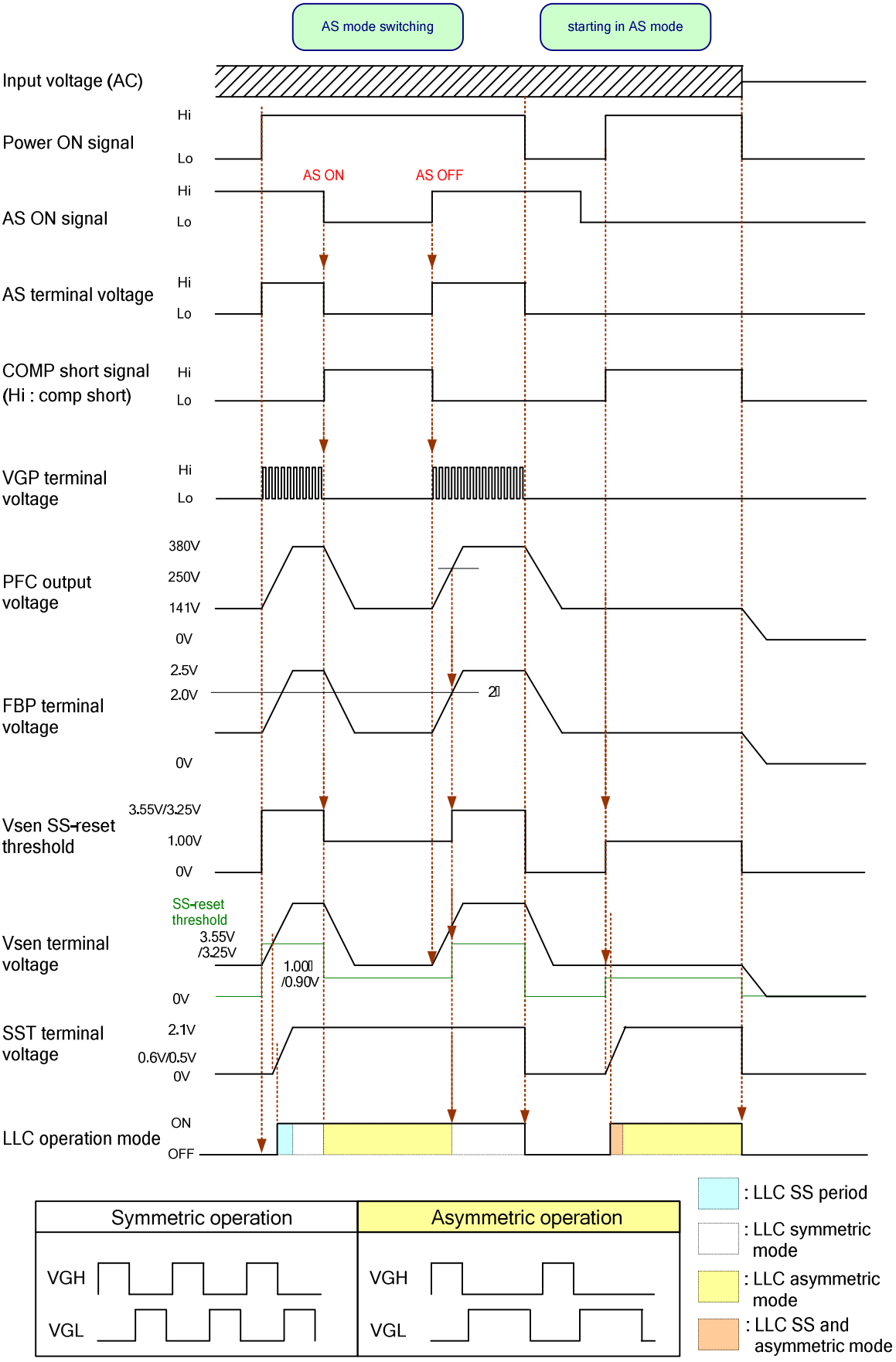


Fig.22 AS mode sequence

2.5.2 Over temperature protection (TSD)

The **MCZ5205SE** adopts over temperature protection. (**TSD**: thermal shut down) that stops the oscillation of PFC and also LLC.
The operating condition is minimum **140 C**. **TSD** is released on condition that the temperature decreases by **40 C** less than the temperature at which **TSD** operated.

2.6 Remarks

2.6.1 PFC stand-alone operation

Connect **SST to GND** to disable LLC.

2.6.2 LLC stand-alone operation

Connect **COMP to GND** to disable PFC.

To operate the LLC, **Vsen**>3.55V should be applied. (**AS** mode OFF)
If intending to start LLC operation at low input voltage, apply 3.55V or more on **Vsen**.
Vsen sink current should be limited to around 2mA.
Note that this operation should be for test purpose only. Do not switch on/off the Vbulk when **Vsen** is externally biased to protect MOSFET from undesired heavy switching stress especially in mid/heavy load condition.

If using the **AS** mode, **FBP**>**2.0V** should be applied.

3 Peripheral components setting

3.1 PFC ZCS turn on timing (ZC)

PFC ON timing is determined by the current limiting resistor **Rzc** as shown in **Fig. 23**.
ZC sink/source current limit is +/-5mA. The resistor limits the current to +/-5mA or less.

The polarity of NC winding should be designed according to **Fig. 23**.
The voltage of NC winding at maximum input voltage must be greater than 1.55V. Design the number of turns of Nc winding on the minimum integer according to an formula(1).

For example, in case of Vin (AC) max = 264V, Vo = 390V and Np=50 turns, Nc=4.5 is obtained from formula, therefore it should be 5 turns. Estimated number of turns Np and Nc is 10:1. (Vin max=264V cases.)

$$Nc > 1.5 \times \frac{Np}{Vo - [\sqrt{2} \times Vin(AC)max]} \quad \text{---- (1)}$$

If designing **ZC** current as **+ /-4mA** (80% of maximum value), select a value of **Rzc** greater than the value calculated from the formula (2) and (3) below.

A resistor of **700** ohms is built in **ZC** in series.

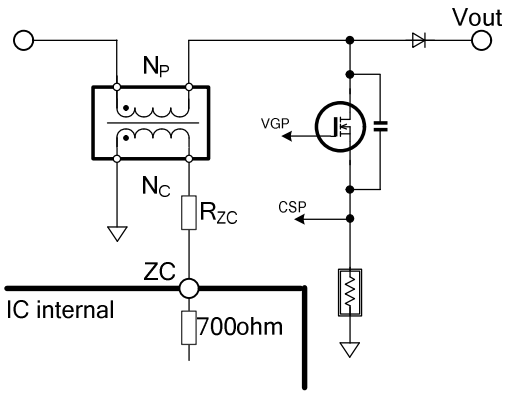


Fig.23 ZC limiting resistance

[Control winding pulse side]

$$R_{ZC}+ = \frac{(Vo - Vinmin) \times \left(\frac{Nc}{Np}\right) - 6}{4 \times 10^{-3}} - 700 \text{ [ohm] ---- (2)}$$

* 6V : ZC built-in zener voltage

[Control winding minus side]

$$R_{ZC}- = \frac{(- Vinmax) \times \left(\frac{Nc}{Np}\right)}{-4 \times 10^{-3}} - 700 \quad \text{[ohm] ---- (3)}$$

[Design example]

At Vo=400[V], Vin(AC)max=276[V] , Np=50[turns] , Nc=5[turns] ,

[Control winding pulse side]

$$R_{ZC}+ = \frac{(400 - 0) \times \left(\frac{5}{50}\right) - 6}{4 \times 10^{-3}} - 700 = 7.8 \text{[kohm]}$$

[Control winding minus side]

$$R_{ZC}- = \frac{\left(-276 \times \sqrt{2}\right) \times \left(\frac{5}{50}\right)}{-4 \times 10^{-3}} - 700 = 9.1 \text{[kohm]}$$

Thus, **ZC** current limiting resistor R_{ZC} can be designed as 9.1kohm or greater.

3.2 PFC Phase compensation (COMP)

PFC feedback amp is trans-conductance amplifier (gm amp).

Fig.24 shows a circuit for pfc phase compensation. The value of Ccomp1, Ccomp2, and Rcomp are calculated from following formula.
Finally adjust the values in actual circuit.

Determine the value of Ccomp1 and Ccomp2 according to formula (4), so that fc(cut off frequency) is 20Hz or less.

$$fc = \frac{140u}{2\pi \times (Ccomp1 + Ccomp2)} \quad [Hz] \quad \cdots(4)$$

* 140u: the conductance of gm amp

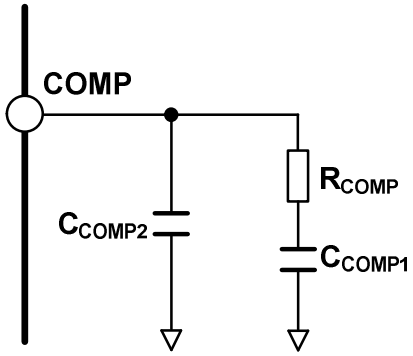


Fig.24 COMP circuit

Recommended value of **Ccomp2** is around **0.1uF**, and **Rcomp** is **4.7k** to **47kohm** respectively.

3.3 PFC output voltage / OVP threshold (FBP terminal)

PFC output voltage is determined by resistance divider (Refer to **Fig. 25**) and is obtained from formula (5).
R_{FBPH} value of about **2Mohm** is recommended for PFC output voltage of **400**V.

It is effective to connect a capacitor(**C_{FBP}**) of around **1000pF** between FBP and GND for avoiding malfunction due to noise.

*Note :
Capacitance of C_{FBP} may affect feedback characteristic and it is necessary to check and adjust the value in actual operating circuit.

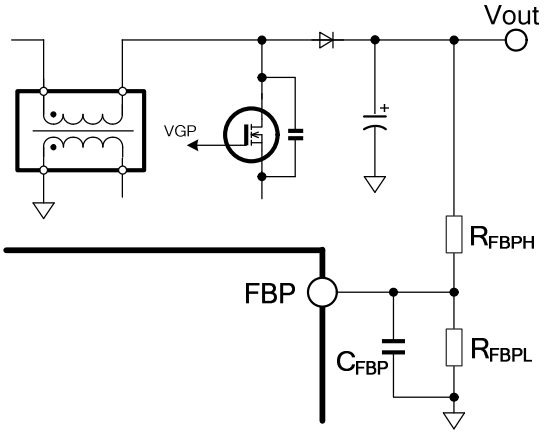


Fig.25 FBP resistance divider

$$PFC \quad Vo = \frac{2.5 \times (R_{FBPH} + R_{FBPL})}{R_{FBPL}} \quad [V] \text{ ----(5)}$$

PFC OVP detection voltage is obtained from formula (6).
Rated voltage of PFC output capacitor should be selected with considering the detection voltage pulse margin.

$$PFC \quad Vo(OVP) = \frac{2.75 \times (R_{FBPH} + R_{FBPL})}{R_{FBPL}}$$

----(6)

3.4 PFC OCP setting (CSP)

PFC over current protection points is obtained from formula (7).
Ps is output power of PFC at the point on which over-current protection works.
n is efficiency of PFC.

$$R_{CSP} = 0.5 \times \frac{\eta \times AC_{min} \times \sqrt{\frac{Vo - (AC_{min} \times 1.2)}{3Vo}}}{\sqrt{2} \times Ps} \text{ [ohm]} \quad \text{---- (7)}$$

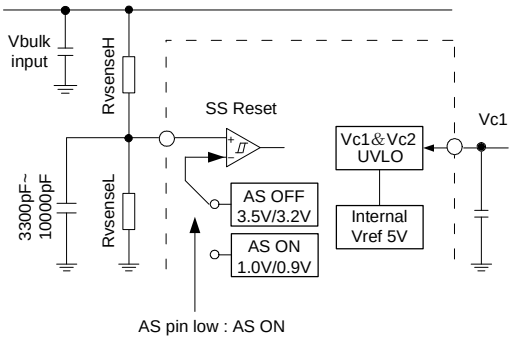
3.5 LLC Brown out protection (Vsen)

Vsen SS reset threshold voltage is **3.55V/3.25V**. (AS mode OFF)
Vsen SS reset threshold voltage is **1.0V/0.9V**. (AS mode ON)

0.2uA is required for **Vsen** sink current and **20uA** or more is recommended not to be affected by the sink current.
If PFC output voltage is 400V, RvsenseH value of **2Mohm** is recommended.
Connect a capacitor of **3300** to **10000pF** between **Vsen** and **GND** for noise reduction.

Low side resistor, RvsenseL(init) is obtained from formula (8). Correct value of Vbulkreset threshold is obtained from formula (9) by using actual value of RvsenseL.

AS mode ON is obtained from formula (10).



$$R_{VsenseL\ (init)} = \frac{3.25 \times R_{VsenseH}}{V_{bulkreset} - 3.25} \quad \text{---- (8)}$$

$$V_{bulkreset} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 3.25 \quad \text{---- (9)}$$

$$V_{bulkreset\ (AS\ ON)} = \frac{R_{VsenseH} + R_{VsenseL}}{R_{VsenseL}} \times 0.9 \quad \text{---- (10)}$$

Fig.26 Vsen internal circuit

3.6 LLC Oscillator / Feedback (FBL)

LLC oscillator frequency is controlled by FBL. FBL sets dead time and soft start (**fss**), max frequency (**fmax**) and min frequency (**fmin**).

3.6.1 dead time and soft start frequency (Ct capacitor)

Dead time and soft start frequency **fss** are determined by **Ct** capacitance. Select a **Ct** capacitance from characteristic specification sheet.

Capacitance value of **Ct** of **820pF** to **2200pF** is recommended due to the relation with dead time.

3.6.2 Minimum frequency fmin (Rt resistance)

Minimum frequency **fmin** is determined by **Rt** resistance. (Connect between **FBL** and **GND**.)
Relation between **Rt** resistance and frequency is shown in characteristic specification sheet.

The estimated value of **fmin** is obtained from formula (11) to (13). **tcharge** is dead time and **tdischarge** is turn on time of VGL/VGH. The exact value should be adjusted by using characteristic specification sheet after checking the frequency at actual circuit operation.

VFBL(bottom) : 1.70V , VFBL(top) : 3.15V

*Note :
This value does not include overshooting and the response delay. Response delay is about 100ns.

$$t_{charge} = \frac{Rt \times Ct \times VFBL_{(top)}}{Rt \times 5.5 \times 10^{-3} - VFBL_{(top)}} - \frac{Rt \times Ct \times VFBL_{(bottom)}}{Rt \times 5.5 \times 10^{-3} - VFBL_{(bottom)}} \quad \text{---- (11)}$$

$$t_{discharge} = -Rt \times Ct \times \ln \frac{VFBL_{(bottom)}}{VFBL_{(top)}} \quad \text{---- (12)}$$

$$f_{min} = \frac{1}{2 \times \left(t_{charge} + t_{discharge} \right)} \quad \text{---- (13)}$$

3.6.3 Maximum frequency fmax (FB resistance)

Maximum frequency **fmax** is determined **Rt** resistance and **FB** resistance.
Check the characteristic specification sheet and determine the maximum frequency.

3.7 LLC Soft start / protection delay timer (SST)

Soft start charging current is **28uA**. When SST voltage rises to **0.6V**, gate output starts and timer charging is enabled when **SST** voltage rises to **1.5V**.
Soft start time **tss** is a time in which SST voltage rises from **0.6V** to **1.5V**.
Soft start time **tss** is obtained from formula (14).

$$t_{ss} = \frac{0.9 \times C_{ss}}{28 \times 10^{-6}} \quad \text{----(14)}$$

Timer charging current is **40uA** and timer threshold voltage is **3.6V**.
Thus, Timer charging time **ttimer** is obtained from formula (15).

$$t_{timer} = \frac{1.5 \times C_{ss}}{40 \times 10^{-6}} \quad \text{----(15)}$$

Timer discharge current is **6uA**.
Timer intermittent operation time is obtained from formula (16)

$$t_{timer(intermittent)} = \frac{3.25 \times C_{ss}}{6 \times 10^{-6}} \quad \text{----(16)}$$

3.8 LLC Current limiting / capacitive mode protection (CSL)

Rocpdet is calculated from desired **OCP** threshold Ipk by using formula (17).
Tentative value of **RocpL(init)** is obtained from formula(18) and correct value of **Id** is calculated from formula(19) by using actual value of **RocpL**.

RocpH of **10** to **47 ohm** is recommended considering **OCP** terminal sourcing current (95uA).
Id value should be determined with care to have enough margins in low input voltage / Pomax or switching load condition.

Connect a noise reduction capacitor of around **1000pF** to **10000pF** between **CSL** to **GND**.

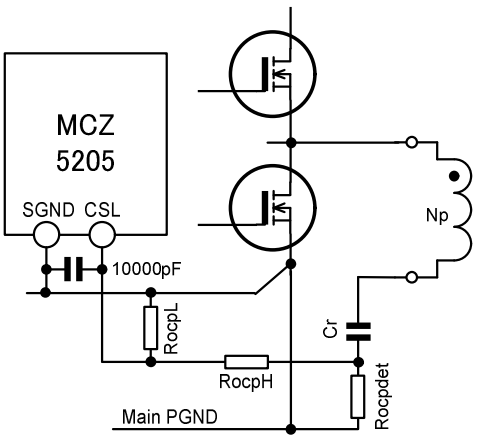


Fig.27 CSL peripheral circuit

$$R_{ocp\,det} > \frac{0.35}{Ipk} \quad \text{[ohm]} \quad \cdots(17)$$

$$R_{ocpL(init)} = \frac{0.35 \times R_{ocpH}}{Ipk \times R_{ocp\,det} - 0.35} \quad \text{[ohm]} \quad \cdots(18)$$

$$I_d = \frac{R_{ocpH} + R_{ocpL}}{R_{ocpL} \times R_{ocp\,det}} \times 0.35 \quad \text{[A]} \quad \cdots(19)$$

3.9 PFC Output voltage and LLC Brown out protection (In case of common sensing line for FBP and Vsen)

If **Vsen** and **FBP** have a common sensing line, circuit diagram is shown in **Fig. 28.**
RH value of **2Mohm** is recommended in case of 400V of PFC output voltage.

1000pF is recommended as $\mathbf{C_{Vsen}}$ capacitance value and also $\mathbf{C_{FBP}}$ capacitance value.

*Note :
Capacitance value of $\mathbf{C_{Vsen}}$ and $\mathbf{C_{FBP}}$ is related to feedback characteristic, and it is necessary to check and adjust the value by actual operating circuit.

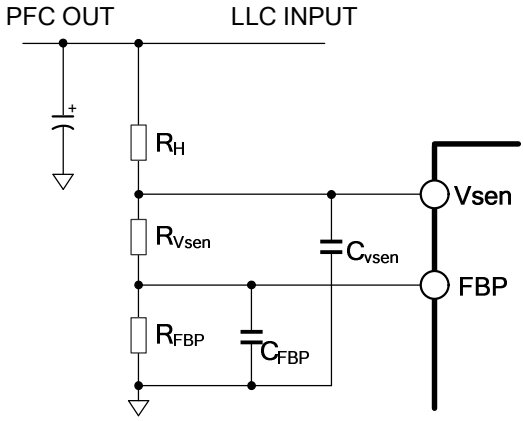


Fig.28 Vsen FBP voltage dividing resistors

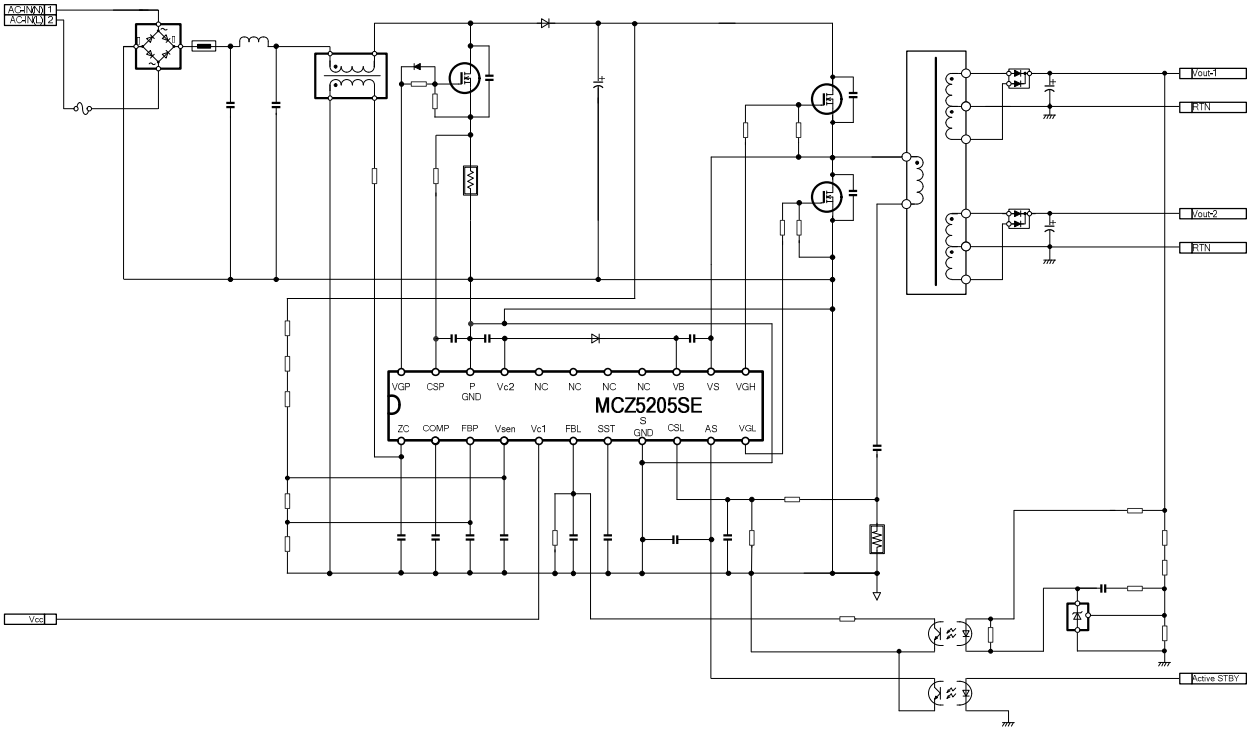
Value of R_{FBP} is obtained from formula (20).
Value of R_{Vsen} is obtained from formula (21).

$$R_{FBP} = \frac{2.5 \times R_H \times V_{bulkreset}}{PFC\ \ Vo \times (V_{bulkreset} - 3.25)} \text{ ---- (20)}$$

$$R_{vsen} = \frac{3.25 \times R_H}{V_{bulkreset} - 3.25} - R_{FBP} \text{ ----(21)}$$

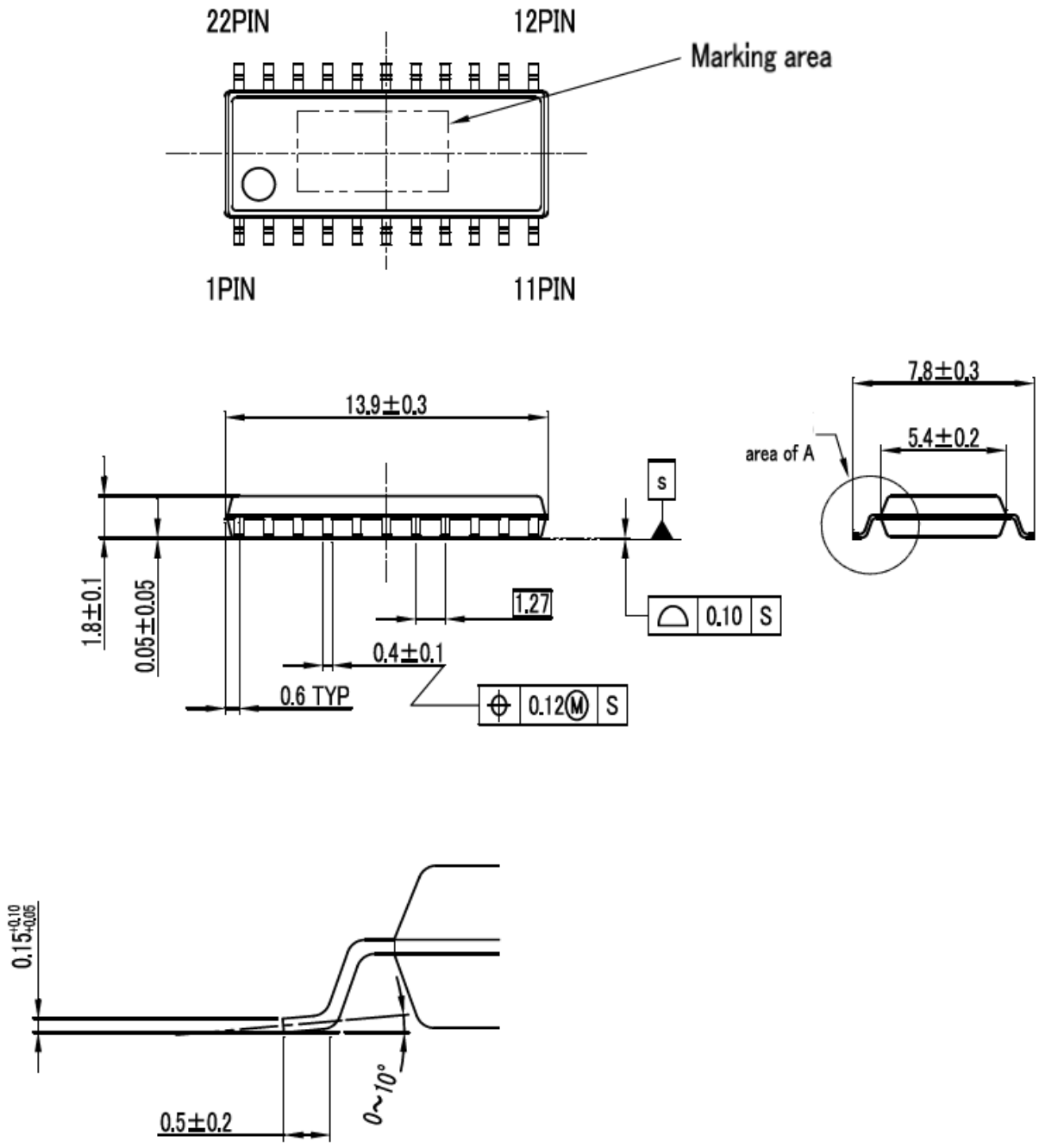
4 Circuit diagram

4.1 Typical application circuit (LLC dual output)



5 Dimension

5.1 SOP22 (MCZ5205SE)



Notes: