Converter Topologies in Telecom and Server Power

Sober Hu

Agenda

- Technical Features
- PFC Stage
  - Lossless Snubber PFC
  - ZVT PFC
  - Interleaving PFC
  - Bridgeless PFC
- DC/DC Stage
  - ZVS PS-FB
  - Resonant Converters
  - Buck Pre-Regulated Open Loop Resonant Converters
  - 2-FETs Forward
  - Active-Clamped Forward

Technical Features

Data Centre and Server System

Example --- Emerson DS Series Server Power

Example --- Eltek Flatpak2 Telecom Rectifier

Power Supply Driving

Trend of Power Density and Efficiency

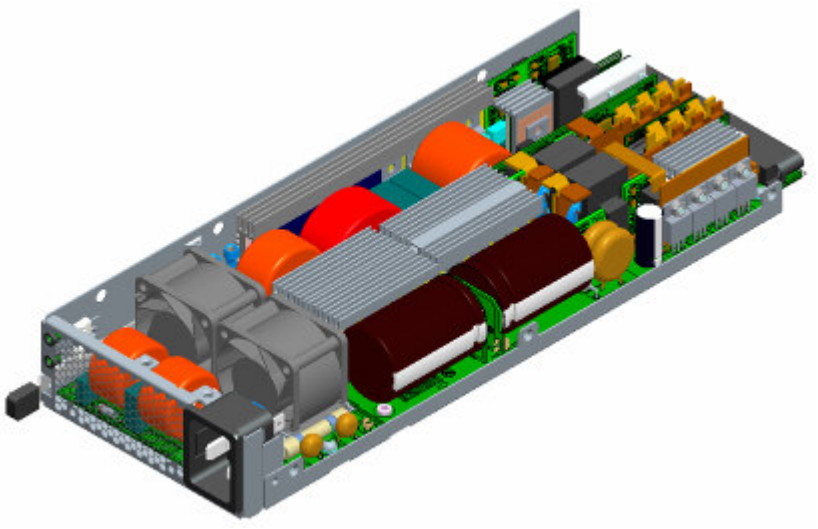
Data Center and Server System

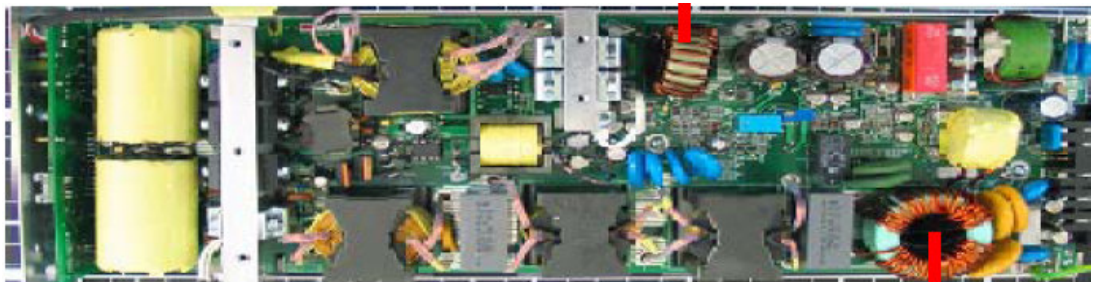
NeoBuzz Data Center

Server Farm

Power consumption in data centers increased drastically, and new data centers with tens of thousands of servers consume mega, even tens of mega watts power.

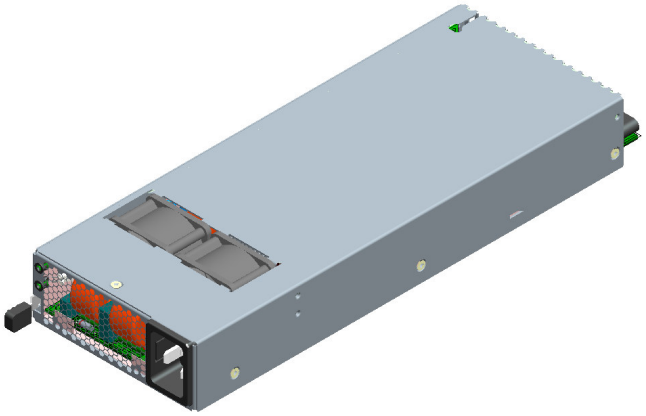
Telecom and Server Power





Example --- Emerson DS Series Server Power

- Input AC: 90 - 264V 50/60Hz
- Output Power: 2000W
- Outputs: 12V /164.2A max, 3V3SB/9A
- EMI: EN55022 CLASS B
- Cooling: 2 x 40mm Internal fans
- Full digital control implementation
- Dimension: 295.7*106.7*40 (11.000" x 4.200" x 1.570")
- Power density: 26.14W/cu. Inch.
- Efficiency: 93% nominal input voltage



- http://www.powerconversion.com/products/websheet/314/DS1800-2000

Example --- Eltek Flatpak2 Telecom Rectifier

- 1U high, narrow width
- 2000W, 185Vac to 275Vac

  Derated down to 85Vac
- -40C to +75C operating
- Internal fans
- Front to back air flow
- Dimension: 327*109*41.5 (13.000" x 4.250" x 1.690")
- Power density: 21.42W/cu. Inch
- 96.5% efficiency “typical”

- http://www.eltekvalere.com/wip4/detail.epl?cat=14742

Flatpack2
Switch Mode Power Supply 48VDC

Flatpack2 HE
Rectifier Module 48/2000

The most efficient rectifier in the industry!

Power Supply Driving

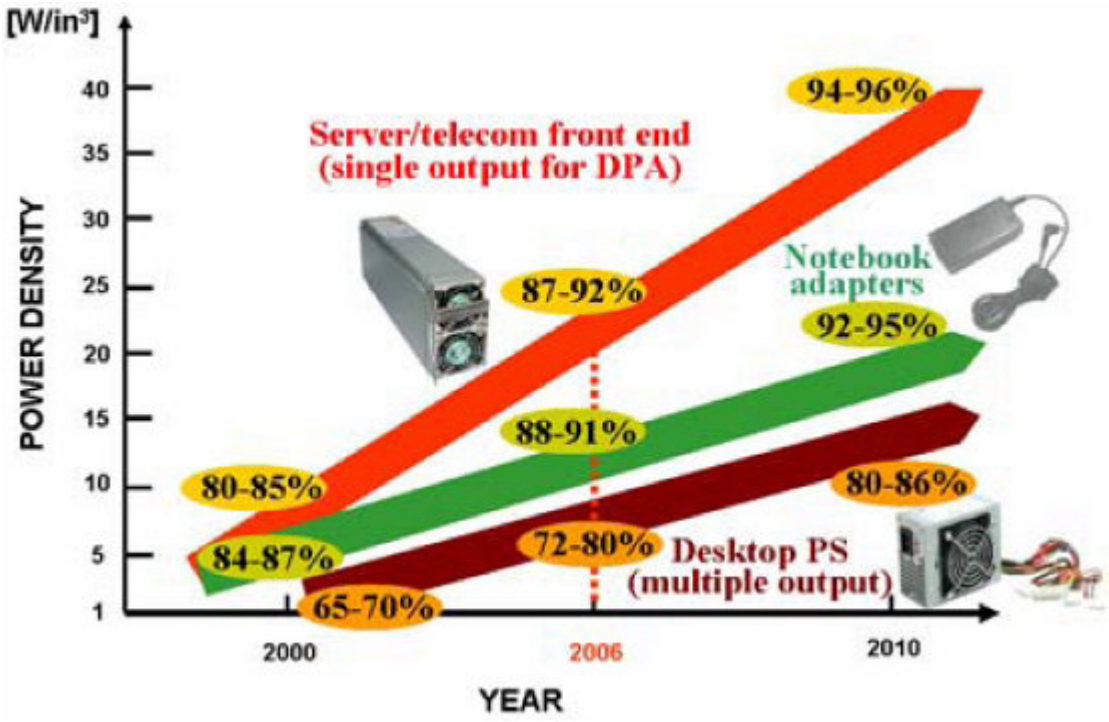
What customers care about?

Higher Efficiency!

Higher Density!

Lower Cost!

Trend of Power Density and Efficiency



Trend of power density and efficiency

PFC Stage

Hard-Switching with Silicon Carbide Diode

Lossless Snubber PFC

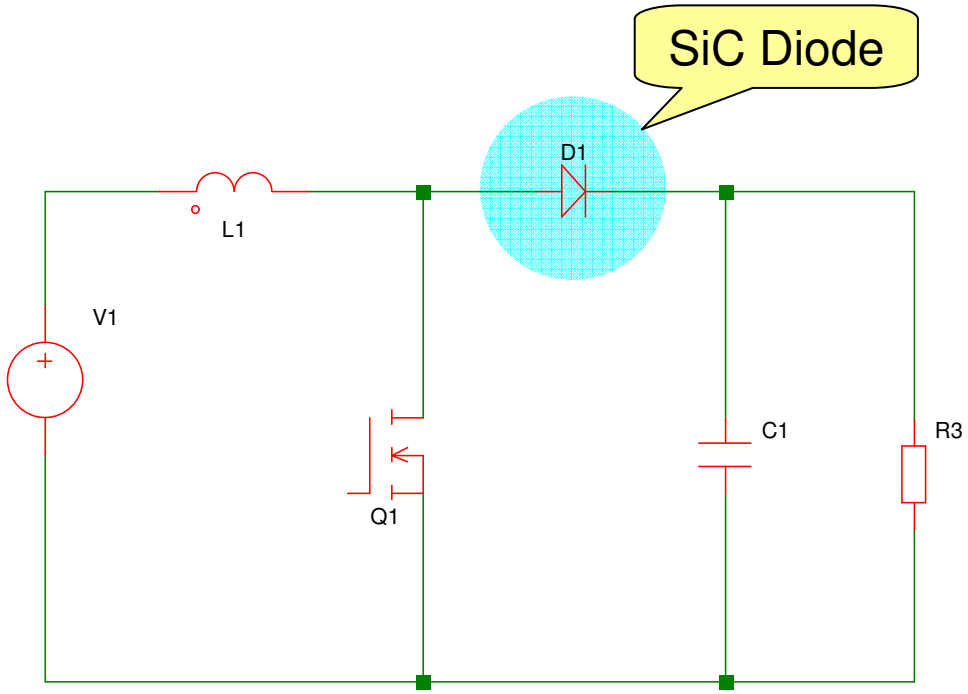
ZVT PFC

Bridgeless PFC

Interleaving PFC

Some Ideas in PFC Controller

Hard-Switching with Silicon Carbide Diode



Nearly zero Trr, high efficiency

Hard-Switching with Silicon Carbide Diode

Field Failure Phenomenon:

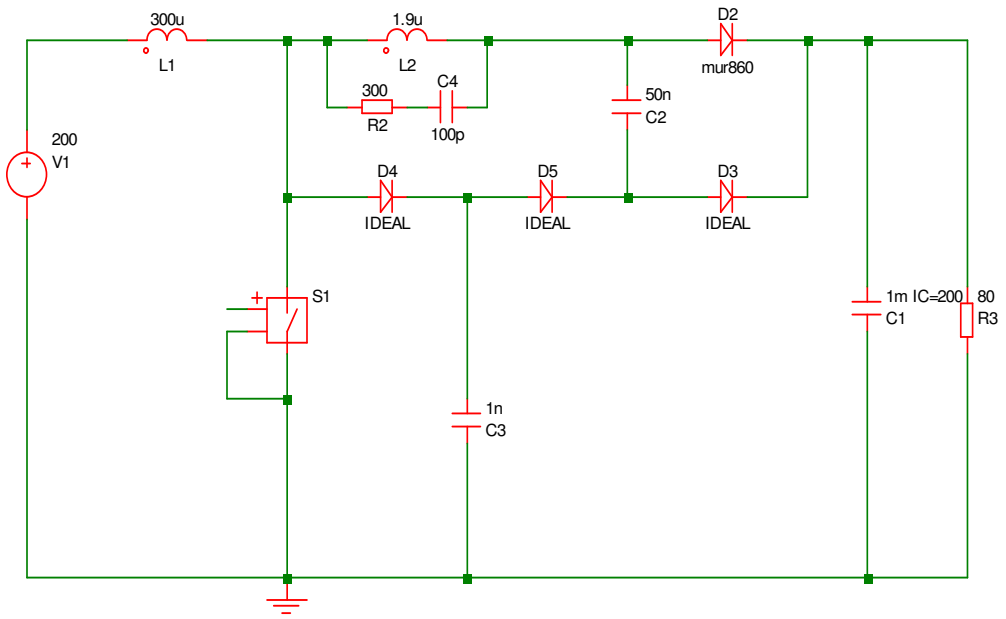
- SiC diode can achieve high efficiencies at higher operating frequencies to improve the power density.
- Field failures are seen with the applications after 6 months and the root cause is related to silicon structure.
- Silicon vendor, Cree, focuses SiC material on LED lighting application.

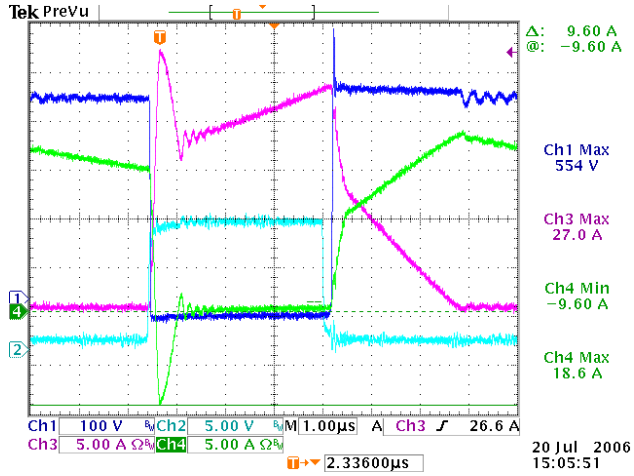
Hard-Switching with Silicon Carbide Diode

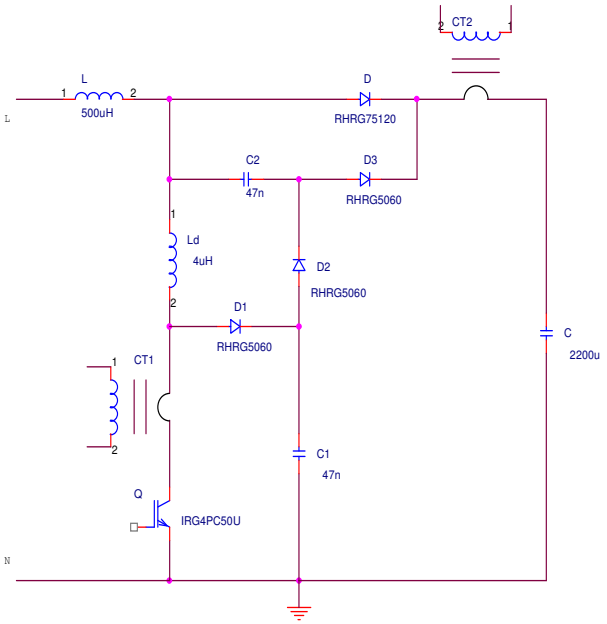
Design Notes:

- Be never over the current rating under all practical operating conditions.
- AC input is lost for 20mSec and then it recovers at 90° phase at 275Vac. In this condition, boost choke is subjected to high voltage and high duty cycle at the same time. A strong possibility of saturation and high peak currents in diode, even at light loads.
- Be never over the voltage rating, especially at the high ambient temperature condition.

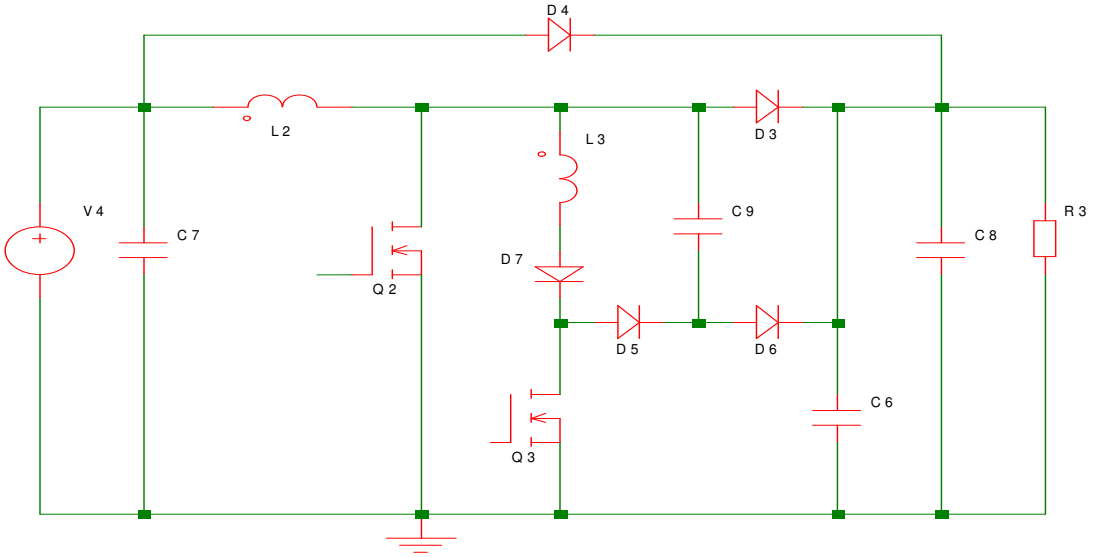
Lossless Snubber PFC

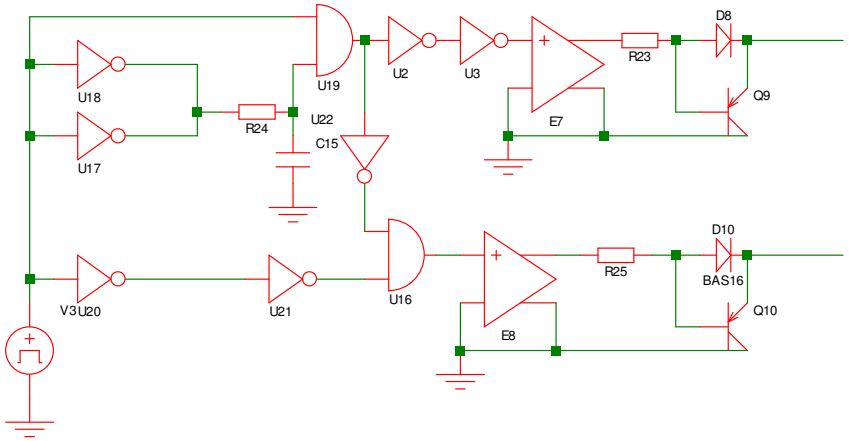


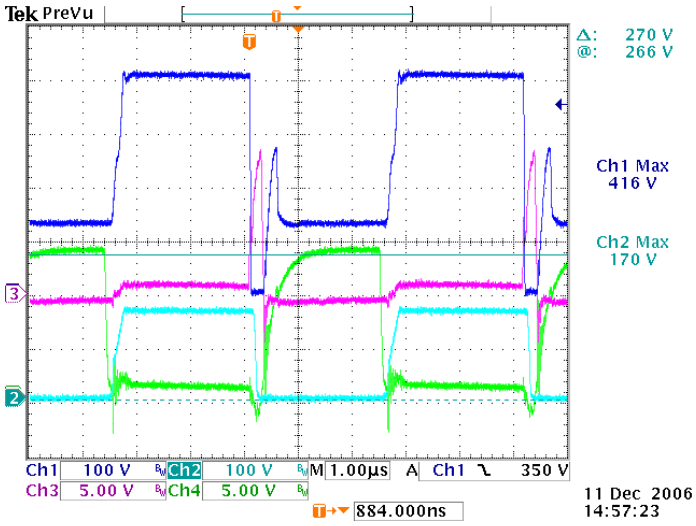




ZVT PFC

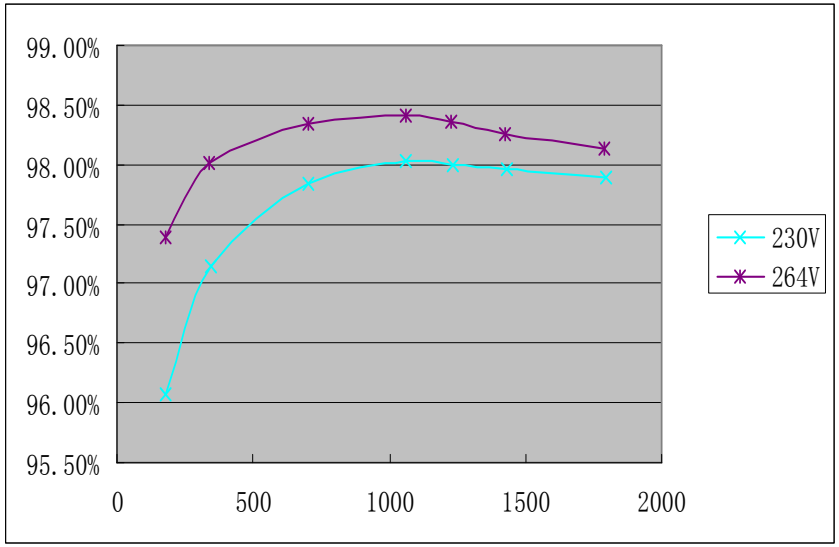

D 4
L 2
L 3
D 3
V 4
C 7
C 9
C 8
R 3
Q 2
D 7
D 5
D 6
C 6
Q 3

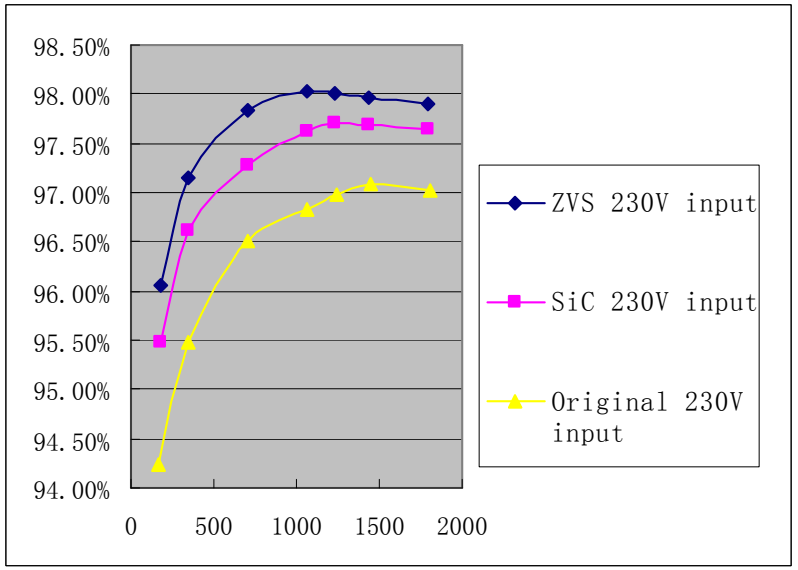

U18
U17
U19
U22
C15
R24
U2
U3
E7
R23
D8
Q9
V3
U20
U21
U16
E8
R25
D10
BAS16
Q10


Tek PreVu
Δ: 270 V
@: 266 V
Ch1 Max
416 V
Ch2 Max
170 V
Ch1 100 V
Ch2 100 V
M 1.00µs
A Ch1 350 V
Ch3 5.00 V
Ch4 5.00 V
884.000ns
11 Dec 2006
14:57:23

ZVT PFC

Efficiency Curves in CCM

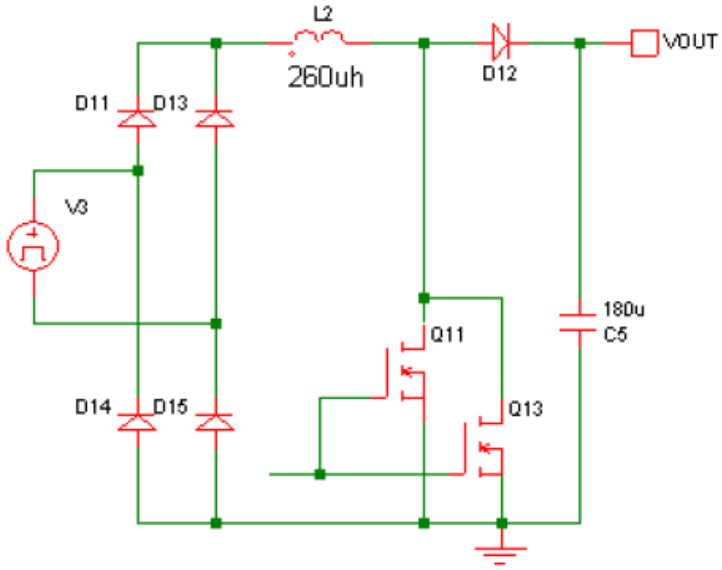


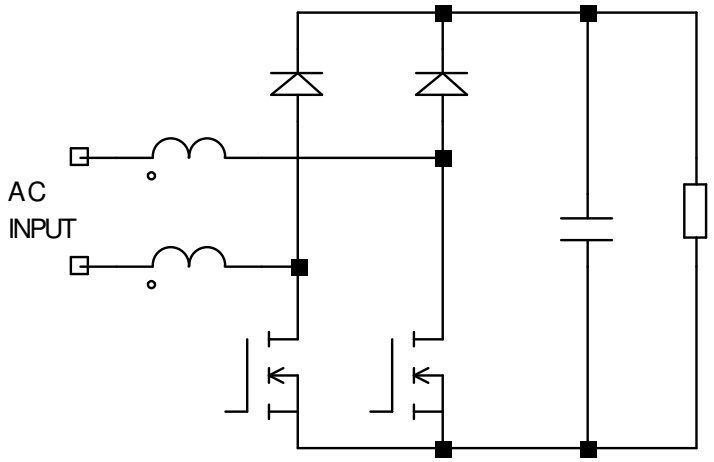


1800W, 200KHz: Effi = 97.9 @ 230Vac

TI business opportunities?! UC3855…

Bridgeless PFC

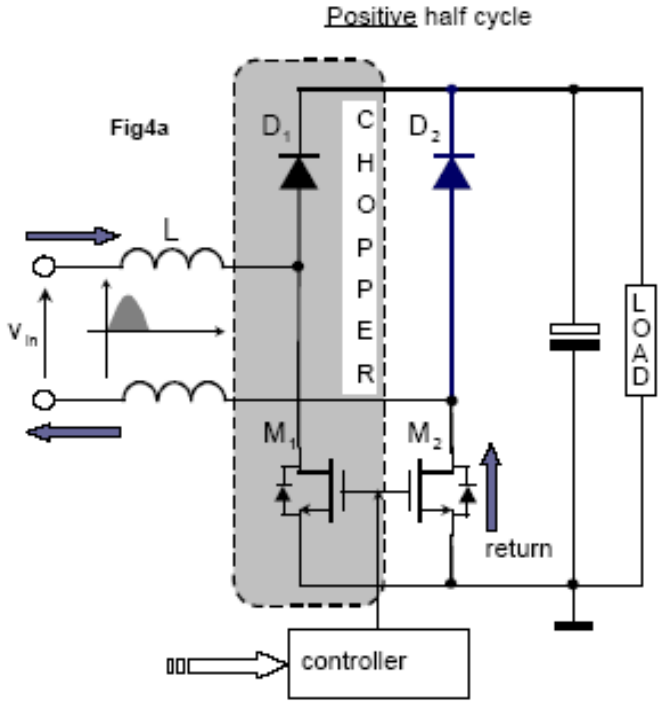


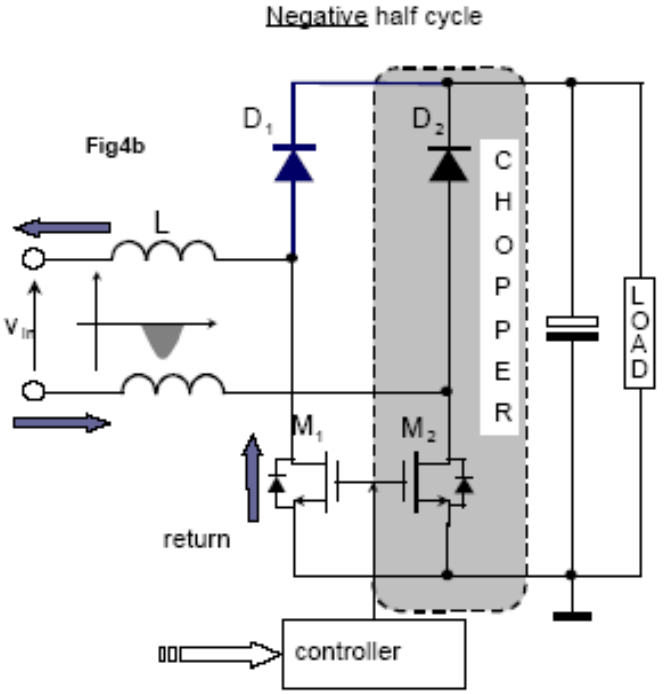


- Rockwell patent, 1983, US # 4,412,277
- Don't need input rectification bridge
- Extremely efficiency, same control signals
- Evenly thermal distribution
- ucc28019, 28060/ucc28070 opportunities
- But severe CM EMI would require complex screening and filtering. and complex filter impact the efficiency?

Bridgeless PFC

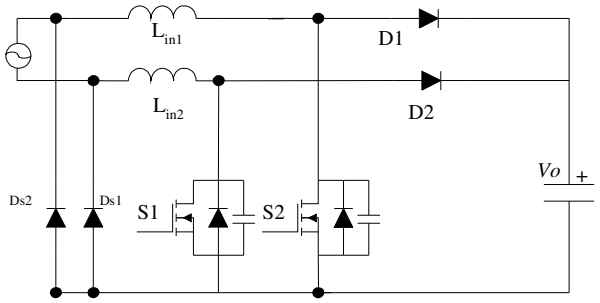
Operation principle

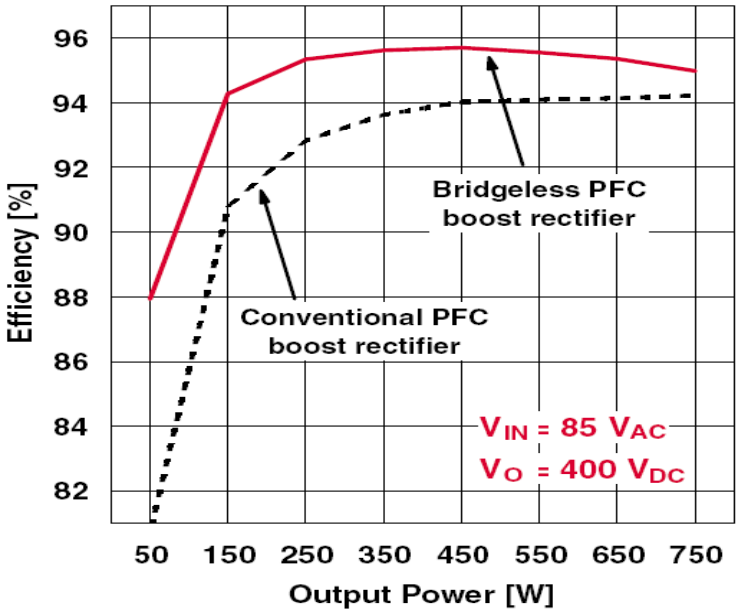


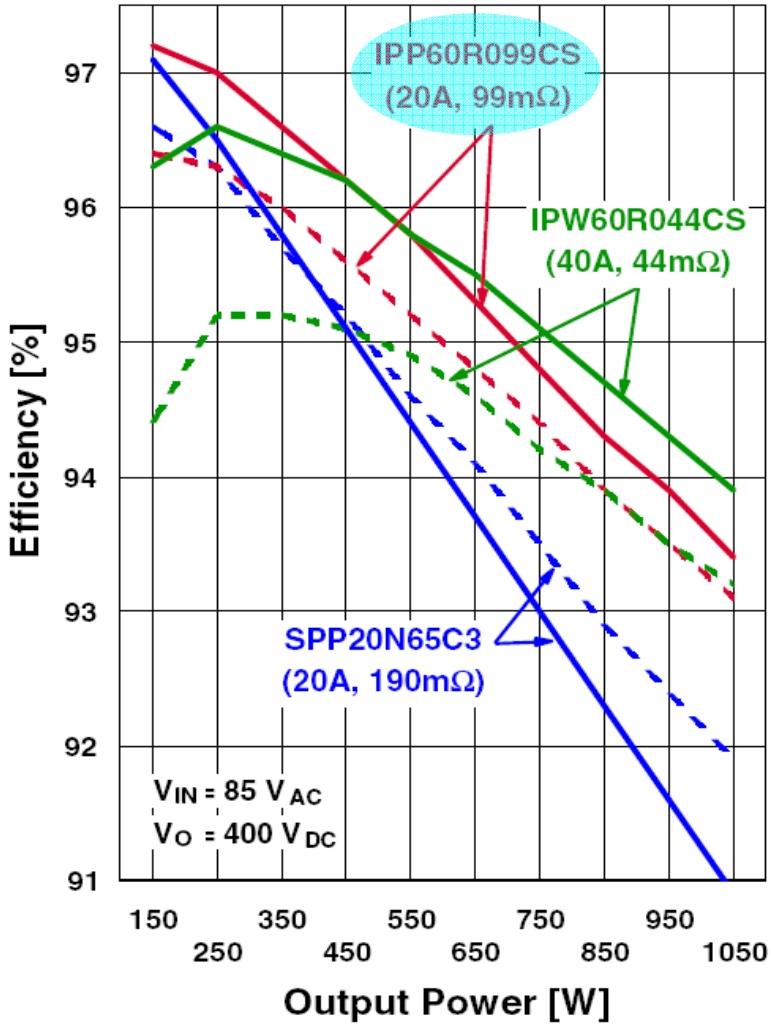


Bridgeless PFC

Performance comparison







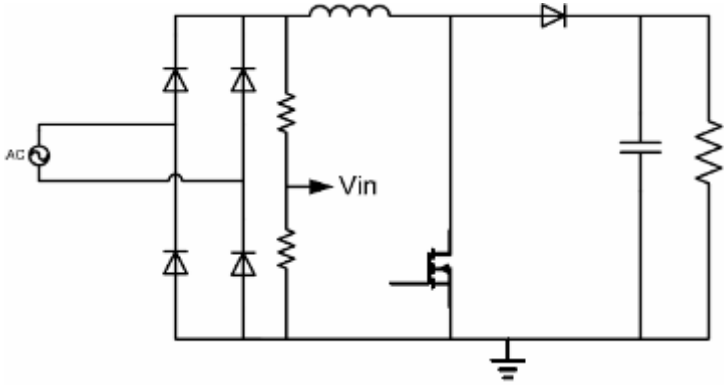
Calculated Result:

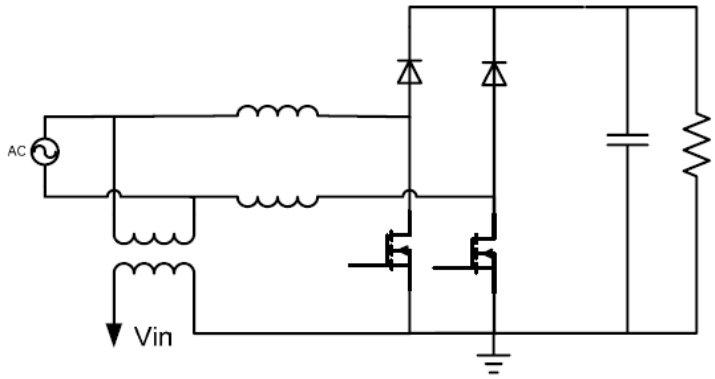
Dashed lines: Single conventional PFC

Solid lines: Bridgeless PFC

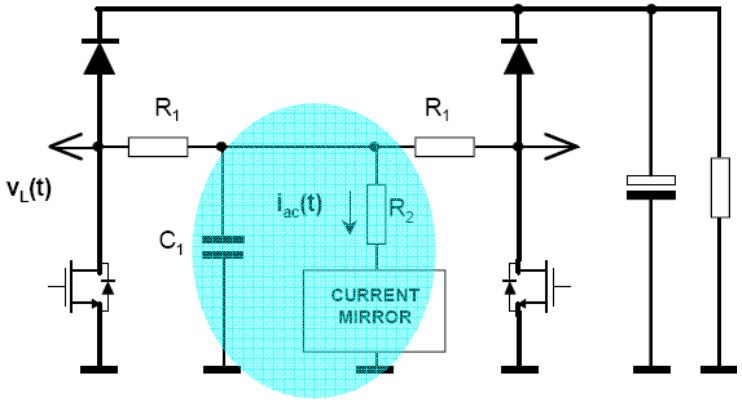
Bridgeless PFC

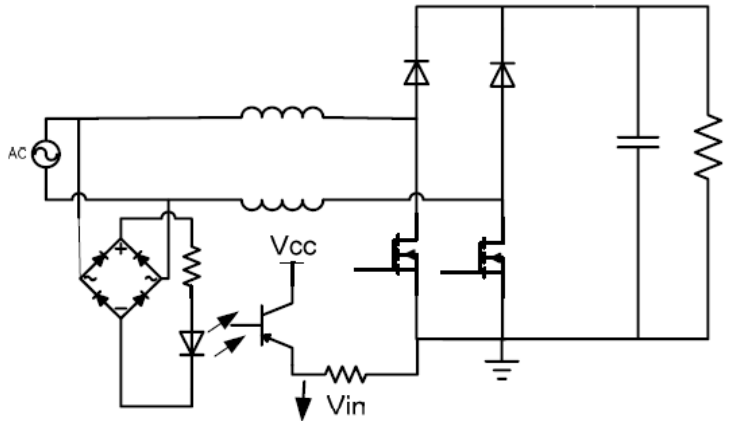
Design Challenges





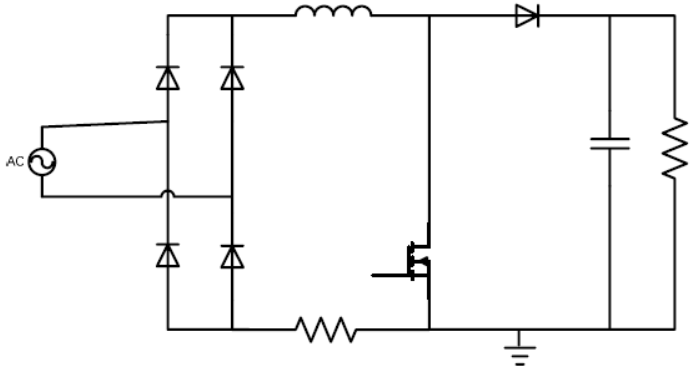
Input voltage sensing



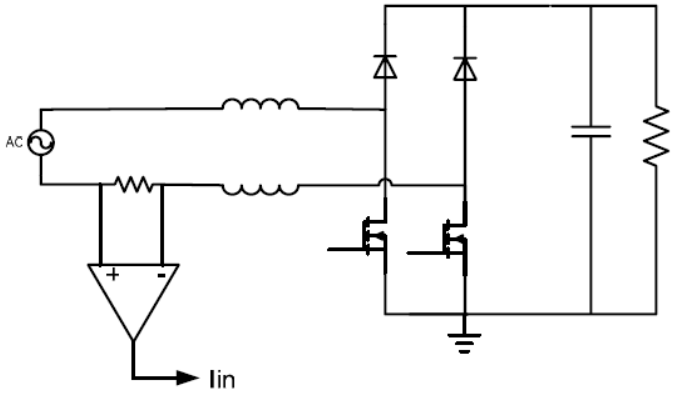


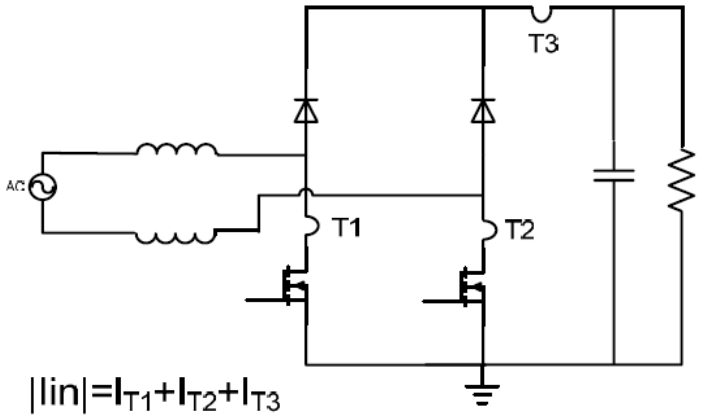
Bridgeless PFC

Design Challenges



Current sensing





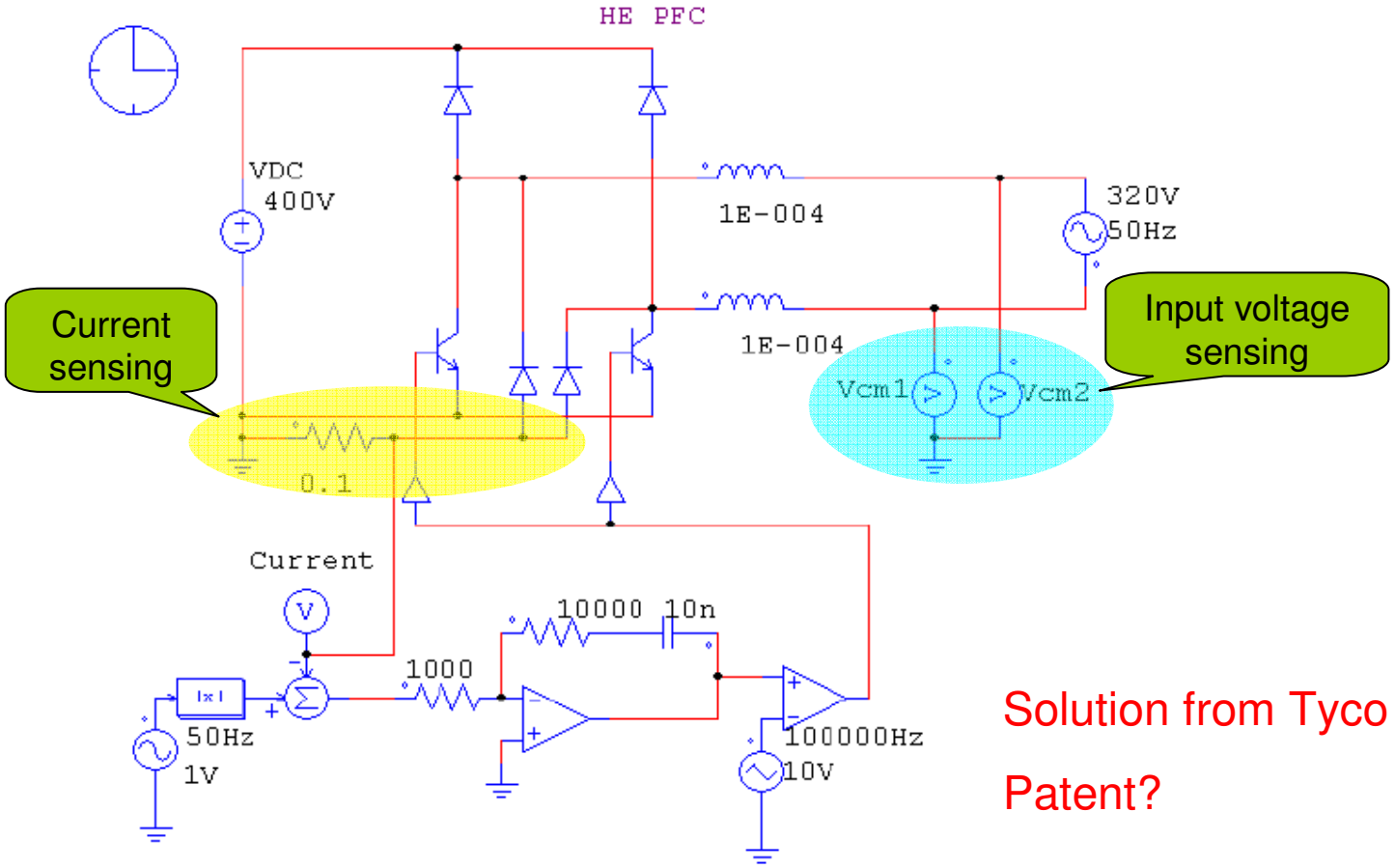
$|Iin|=I_{T1}+I_{T2}+I_{T3}$

The advanced current synthesizer current sensing same in **ucc28070** can be used in the control IC, some CTs will be removed.

Bridgeless PFC

Design Challenges

Ucc28019, ucc28051 improved?



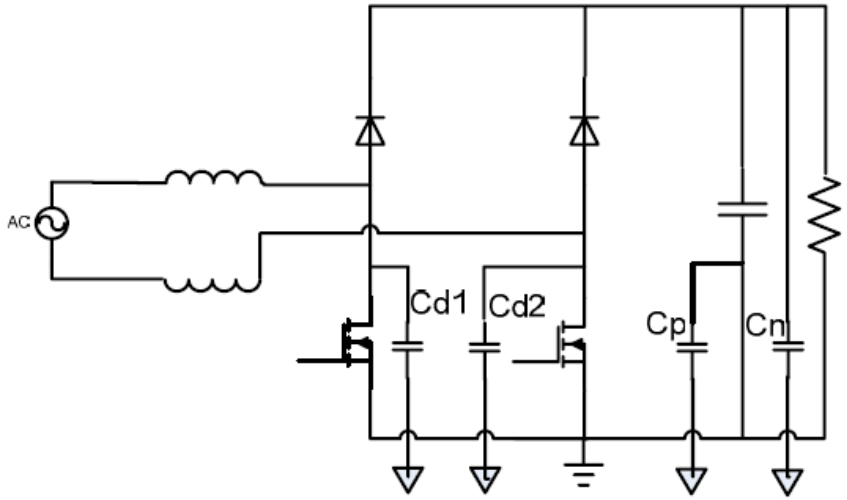
Solution from Tyco

Patent?

Bridgeless PFC

Design Challenges

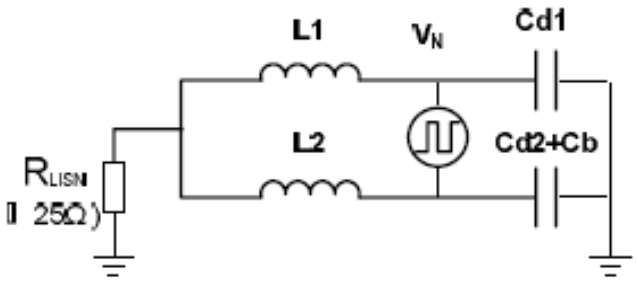
CM EMI



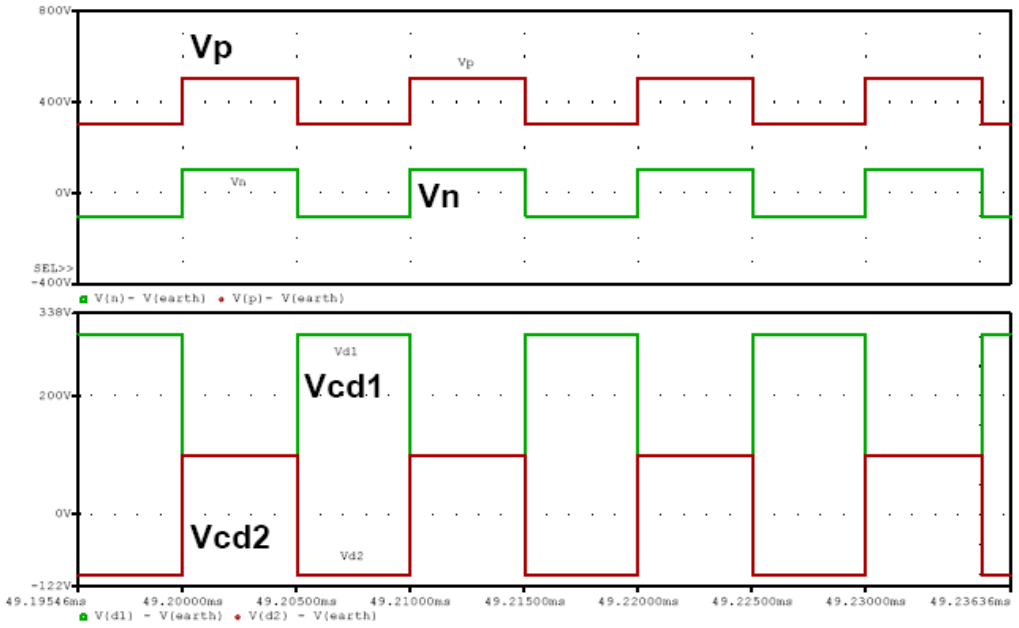
CM noise is mainly caused by high dv/dt on parasitic capacitor to ground.
Cd1 and Cd2 have typical value between 20pF to 50pF. And typical value of Cp and Cn is around 400pF to 500pF.
In conventional single boost PFC, the output bus is always connected to the input power line through the conducting diode of input bridge. The only parasitic capacitor contributing to CM noise is the MOSFET drain to ground capacitor.
In bridgeless PFC, the voltage potential of output bus is pulsating at the amplitude of half output voltage.
Cp and Cn will lead to high common mode noise. Cb equals that Cp is paralleled with Cn.

Bridgeless PFC

CM EMI



Model (positive sub-period)

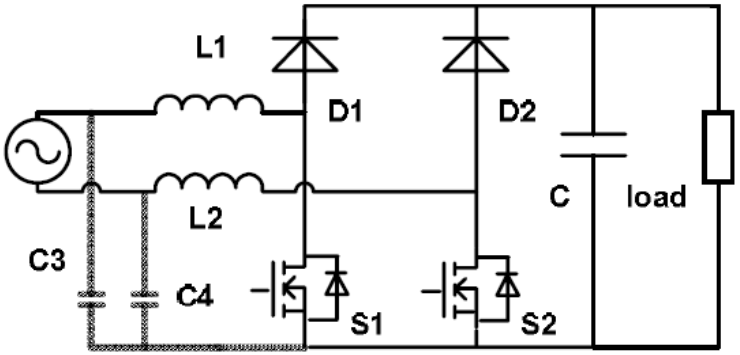


As the dv/dt of the parasitic capacitors between output bus to earth ground, Vp and Vn, are the same, there is no way to achieve noise cancellation.

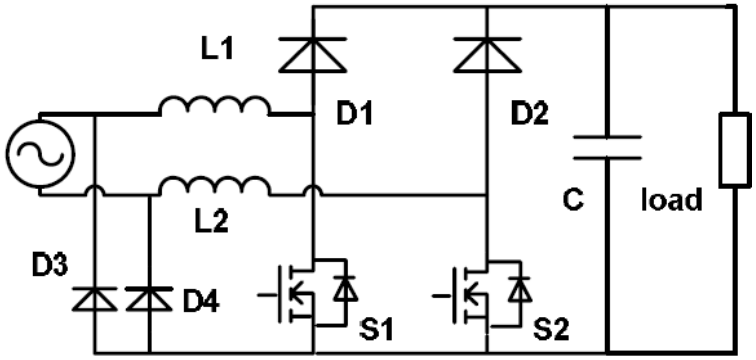
Bridgeless PFC

CM EMI

Existing solutions to improve CM EMI



From CPES



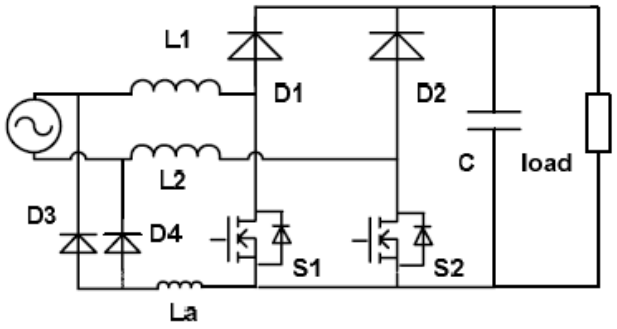
From Tyco

The later solution realizes voltage potential stabilization by disabling one of the inductors.
To keep the same current ripple, the boost inductor size is twice as is needed in a single boost PFC.

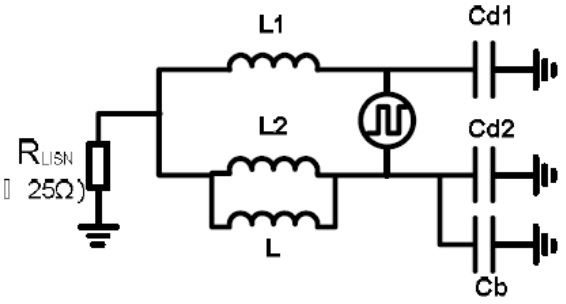
Bridgeless PFC

CM EMI

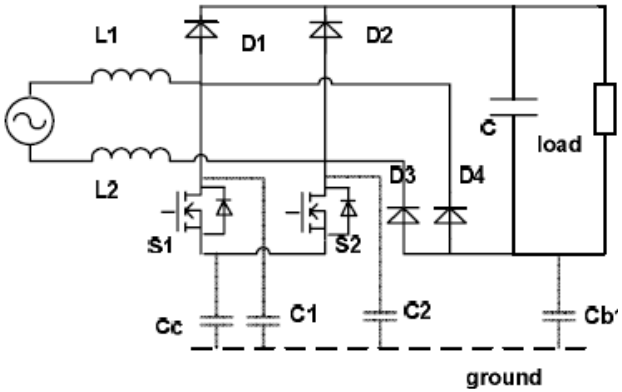
Novel solutions to improve CM EMI



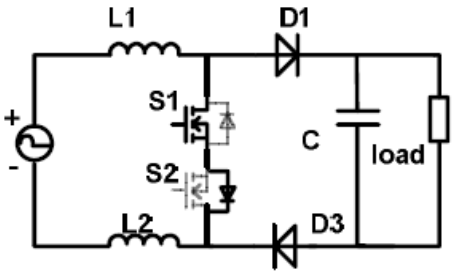
From CPES (Balance technique)

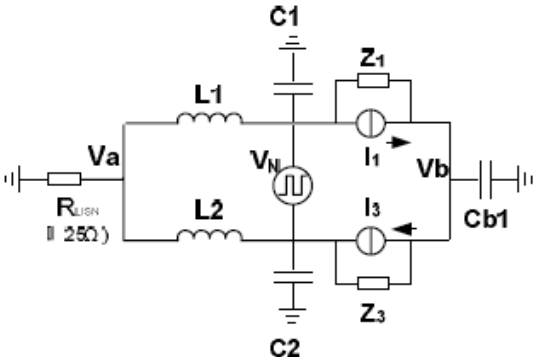


Model (positive sub-period)



Symmetric technology

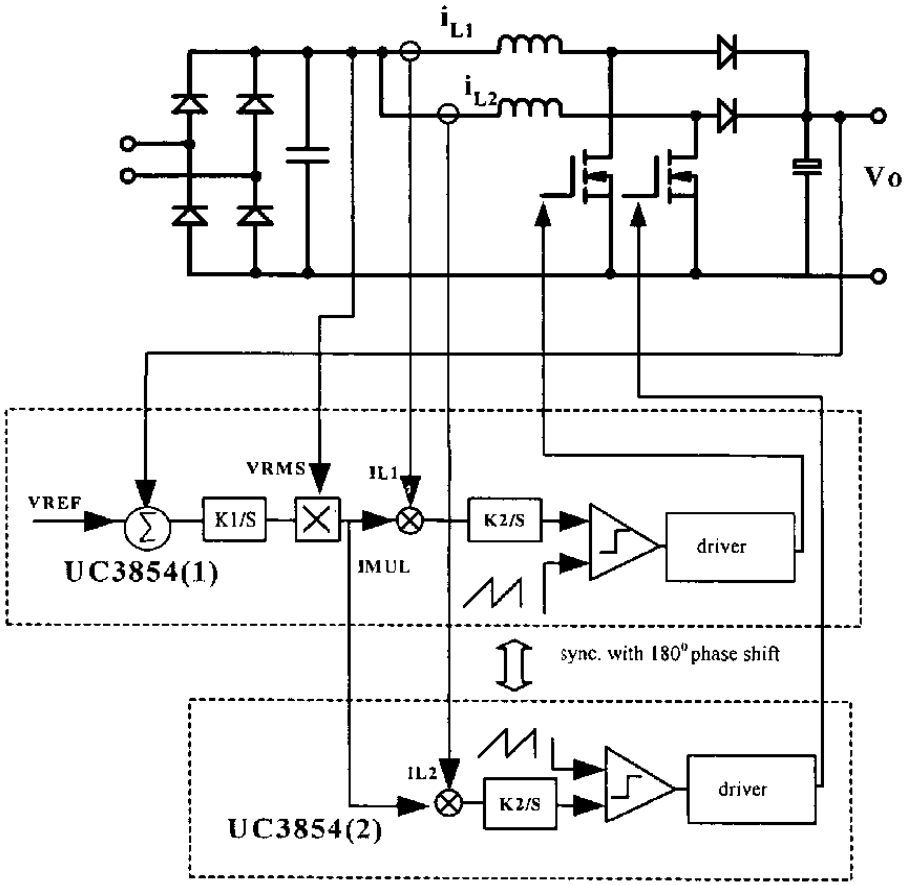




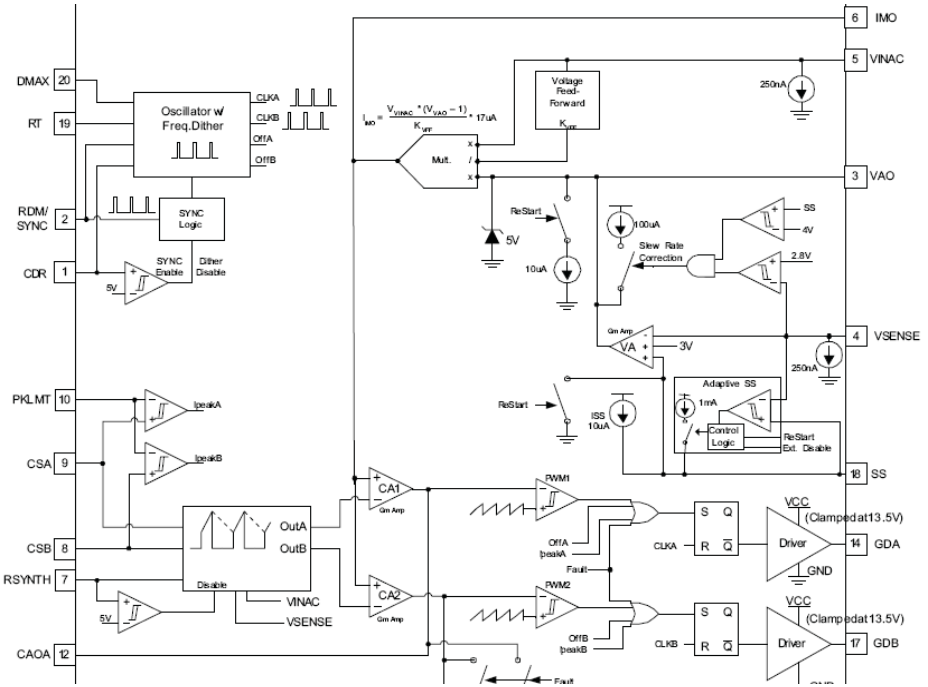
Model (positive sub-period)

Interleaving PFC

Current Sharing



Block diagram in ucc28070

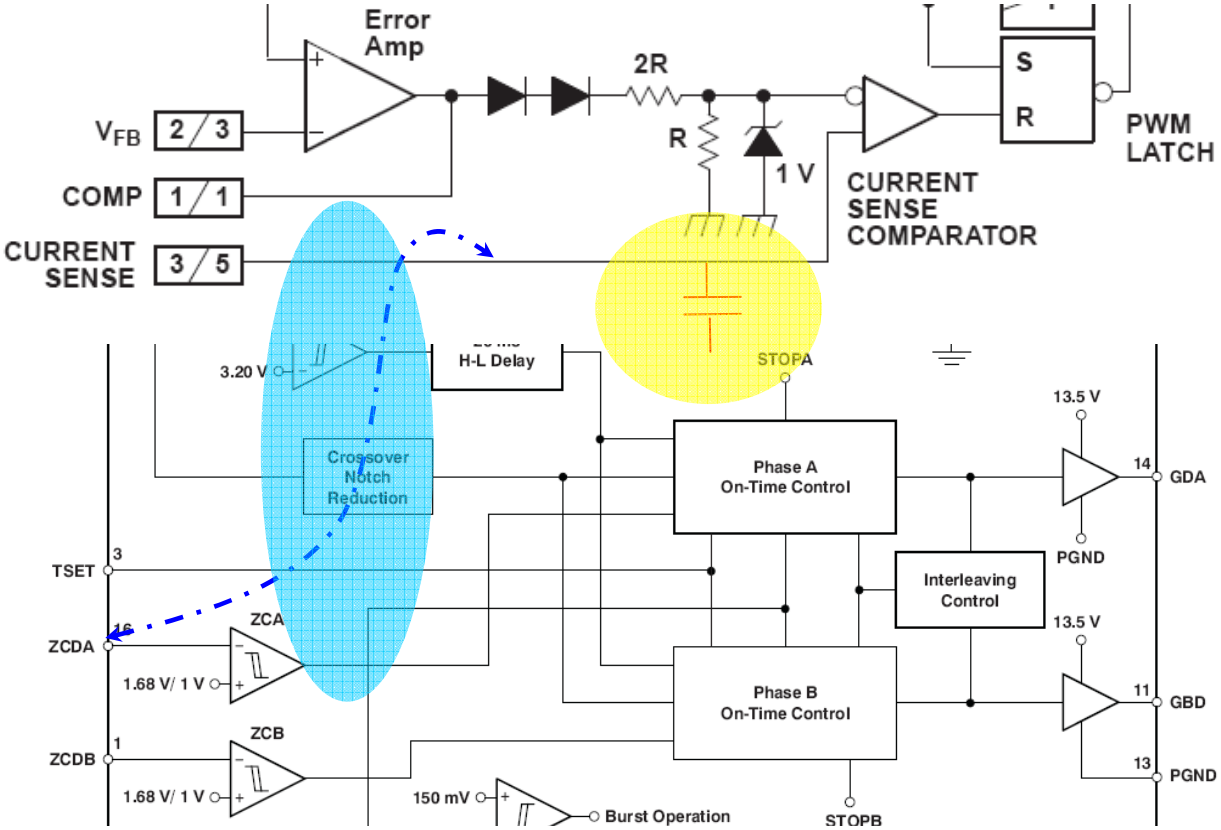


Similar logic function in ucc28070

Current sharing in two channel interleaving Boost PFC circuit

Interleaving PFC

Idea of current sharing improvement in ucc28060

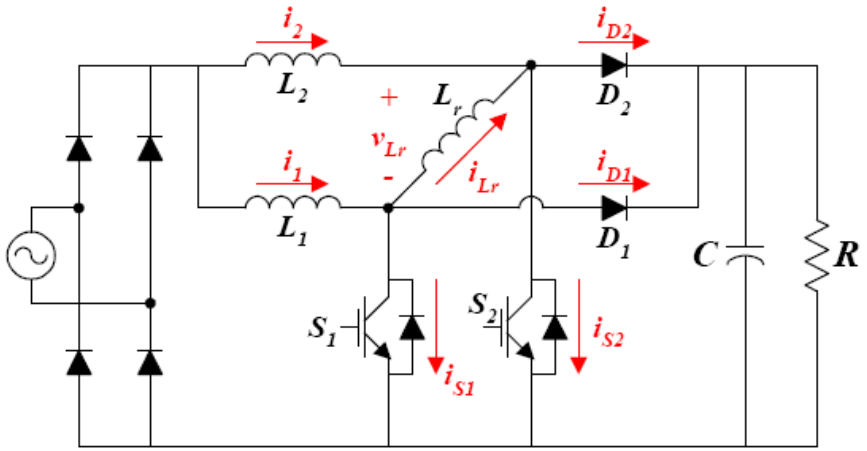


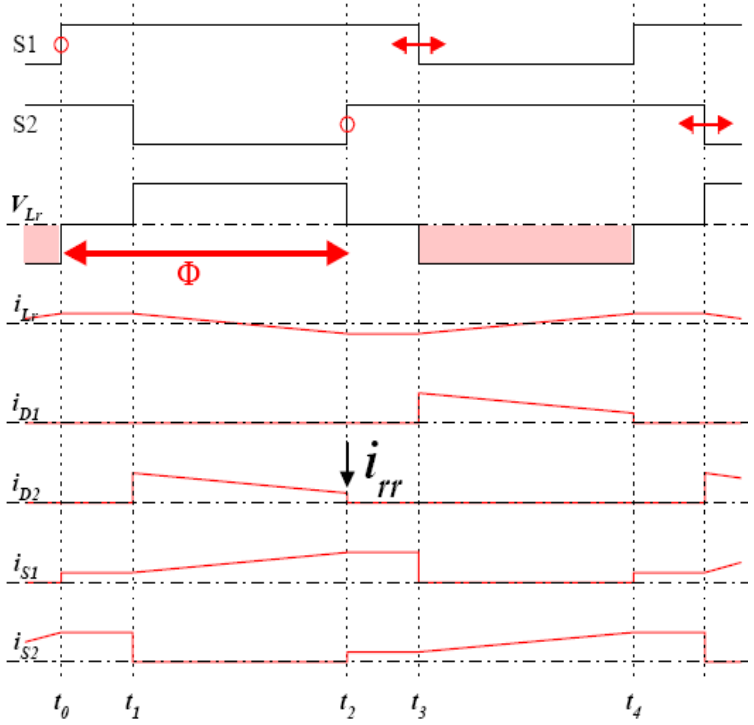
Hybrid current sharing control, try it late!

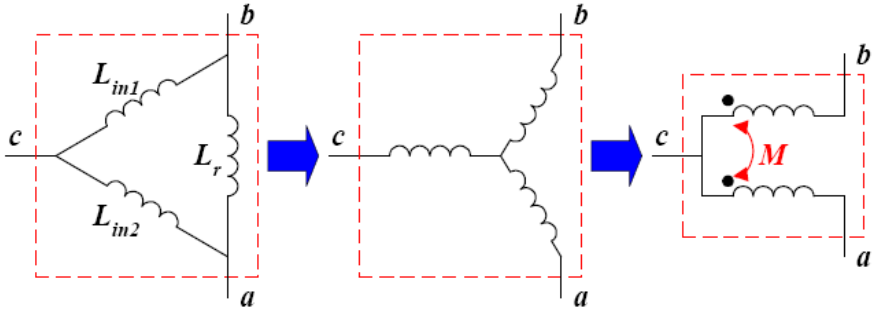
Interleaving PFC

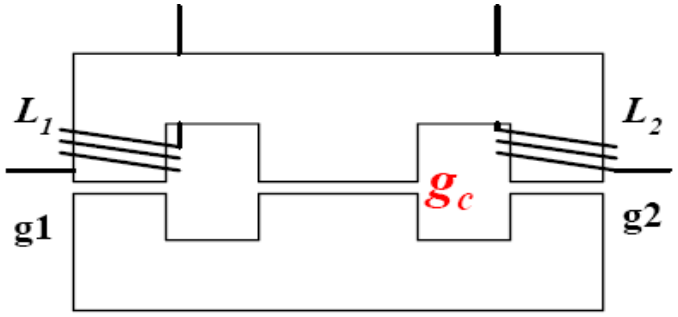
Reduce reverse recovery loss from CPES

Magnetic Integration



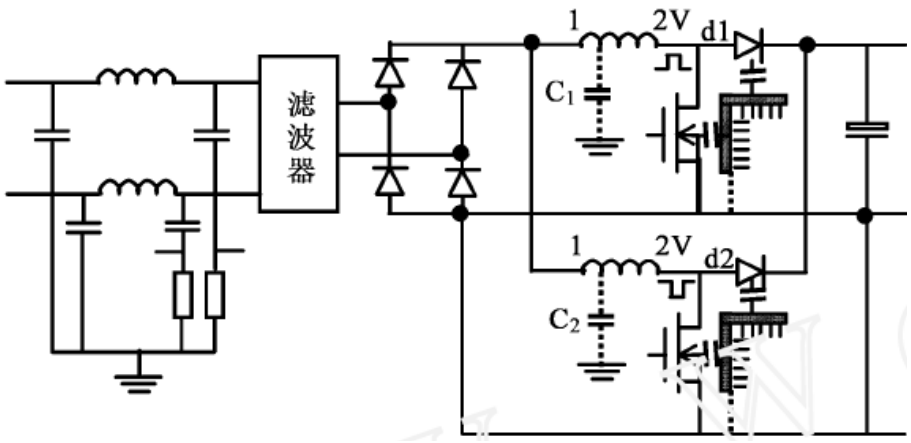




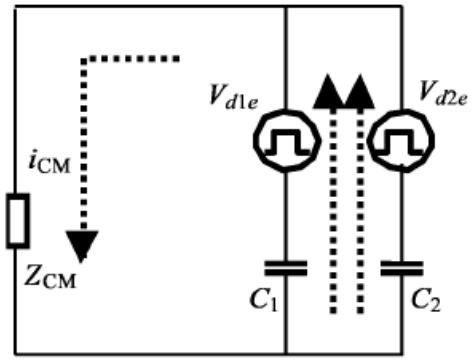


Interleaving PFC

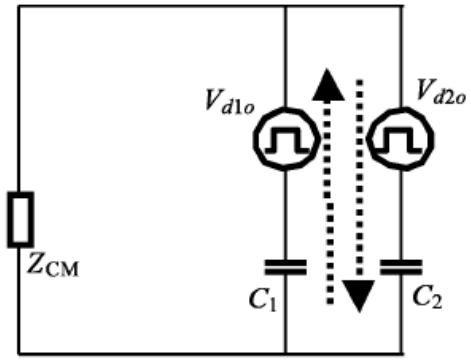
CM EMI



Flourier Analysis



Even harmonics



Odd harmonics

Interleaving technique can improve the input ripple current, reduce DM EMI. But how about CM EMI?

The parasitic capacitors C1 and C2 shall be placed symmetrically with Gnd in order to reduce CM EMI in odd harmonics.

Some Ideas in PFC Controller

- **Bulk Voltage Change with Different Input voltages**
  - Reduced MOSFET switching losses for dc/dc followed and Boost PFC
- **Switching Frequency Change with Different Loads**
  - Reduced MOSFET switching losses for Boost PFC
  - Reduced bias power consumption of PFC drivers
- **Power Saving in Interleaving Operation at light load**
  - Focus on ucc28060/ucc28070
  - Disable one channel operation at light load

DC/DC Stage

ZVS PWM Full-Bridge

ZVS Phase-Shifted Full-Bridge

LLC Series-Resonant Converter

Buck Pre-Regulated Open Loop Resonant Converter

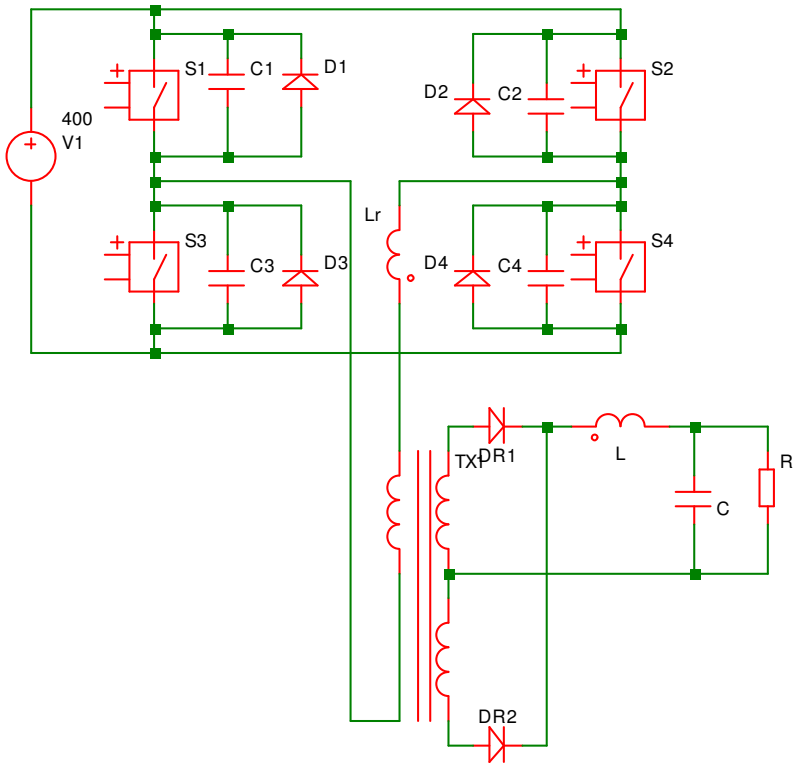
2-FETs Forward

Active-Clamped Forward

ZVS PWM Full-Bridge

Pulse Width Modulation Control (PWM) - Duty cycle is controlled by modulating the pulse width

Intersil: ISL6551, ISL6752



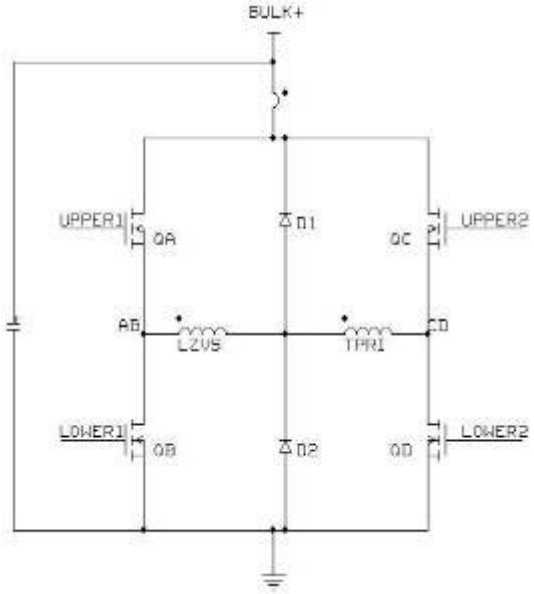
Secondary rectifiers are subjected to spike due to parasitic ringing at the node of primary winding and resonant inductance.

The traditional diode clamp circuit like R. Redl's clamp which are meant for Phase-Shifted Type of control, results in a current imbalance in the main power transformer in PWM control.

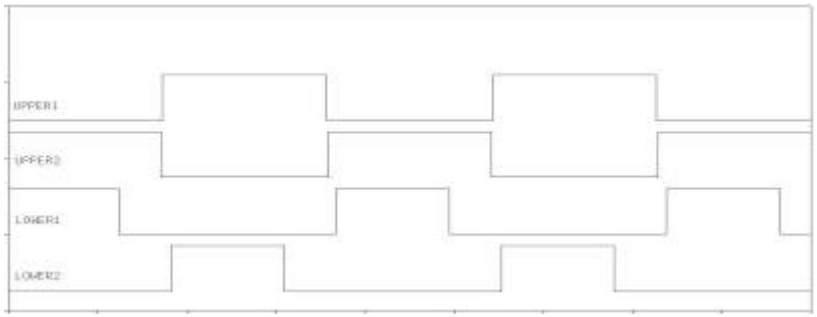
ZVS PWM Full-Bridge

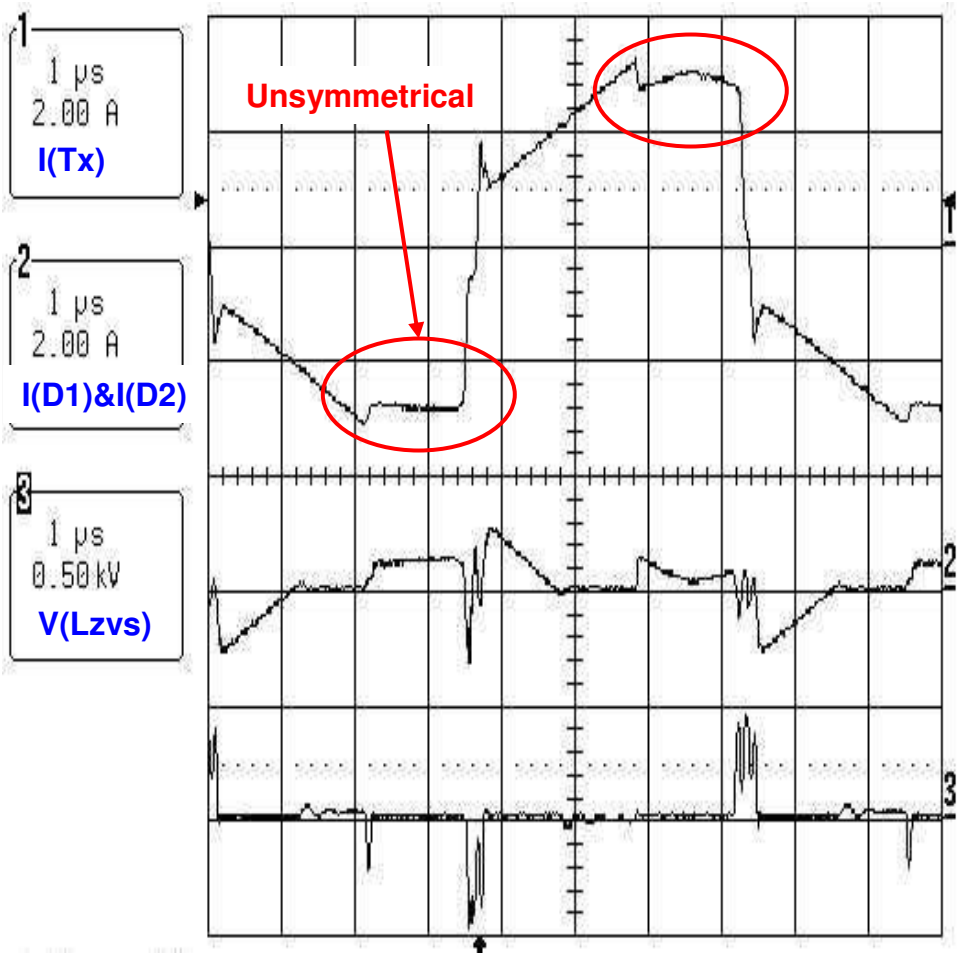
New solution must be found.

- The voltage on resonant inductor shows that there is a volt-second imbalance.



US Patent # 5198969, By Redl

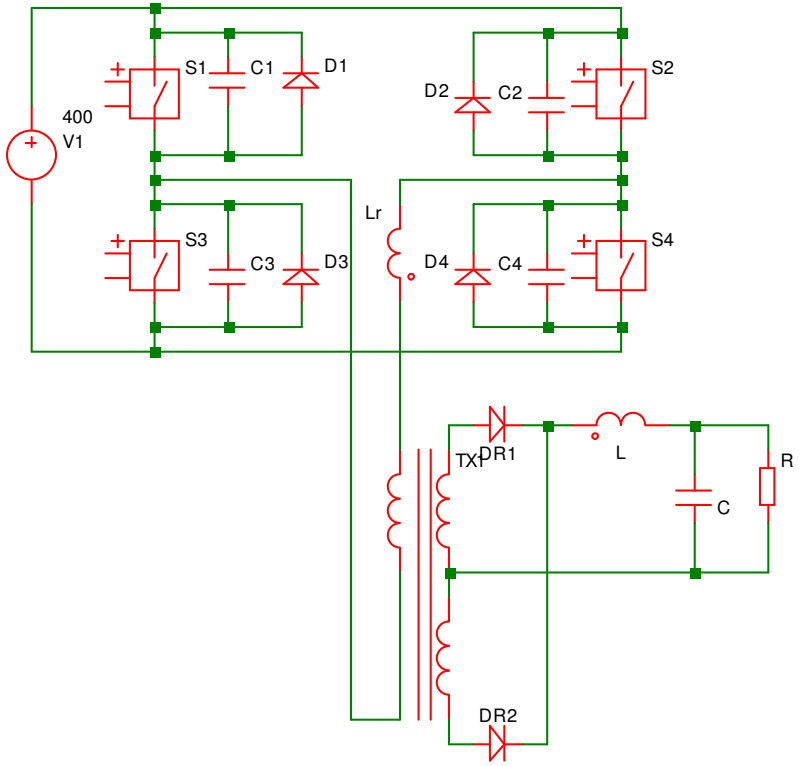




ZVS Phase-Shifted Full-Bridge

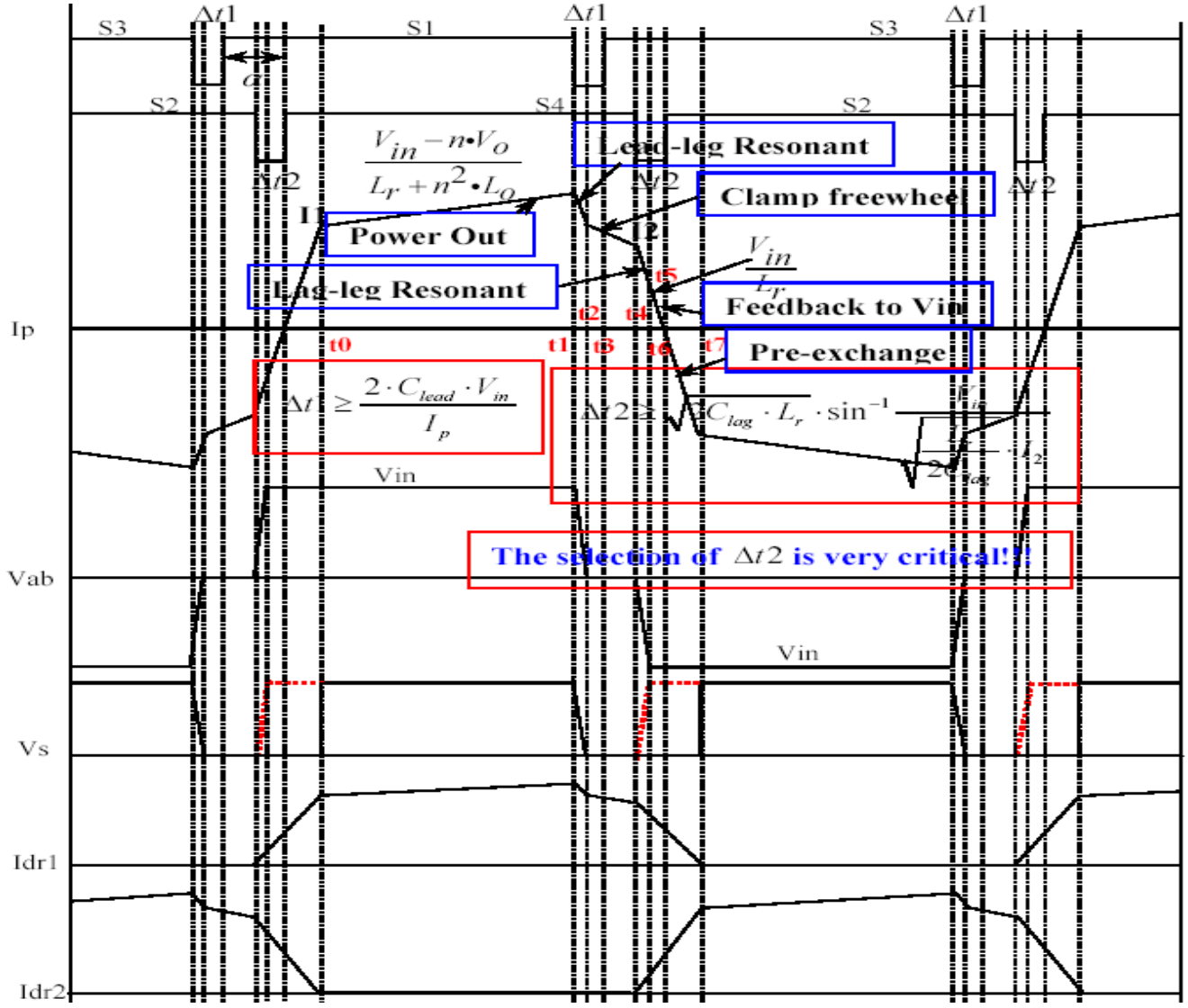
Phase Shift Control - Duty cycle is controlled by phase shifting

TI: UCC3895, UC3879, UC3875



ZVS Phase-Shifted Full-Bridge

Timing



ZVS Phase-Shifted Full-Bridge

Achieve ZVS in Lag-Legs with ucc3895

The lead-legs can get to ZVS easily.

But for lag-legs, it is very difficult, specially at light load condition.

Some approaches

1. Larger magnetizing current

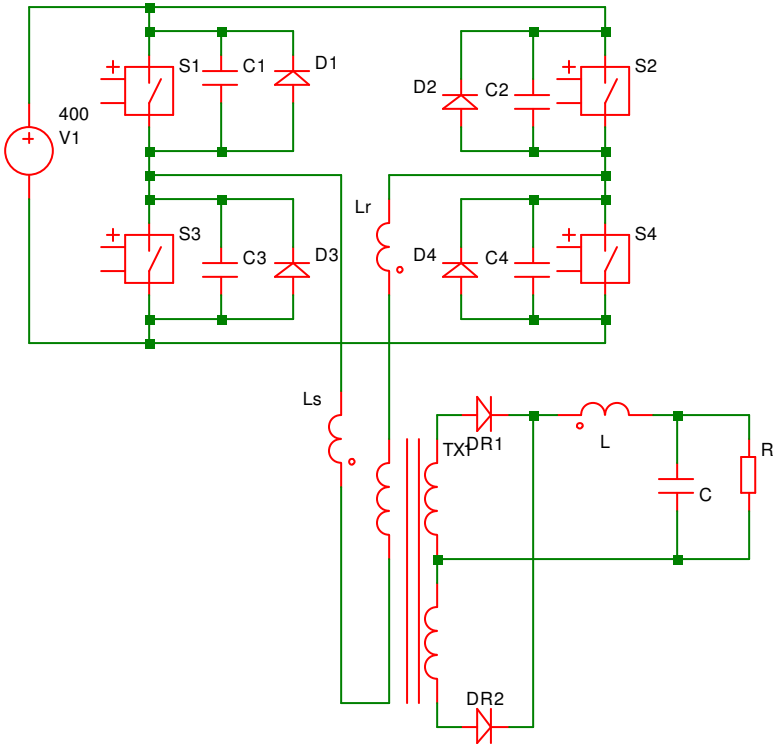
The operation of a full-bridge, zero-voltage-switched pwm converter, VPEC Seminar, 1989

2. Larger resonant inductance

$$\frac{1}{2}\cdot L_r \cdot {I_2}^2 > \frac{1}{2}\cdot C_{oss}\cdot {V_{in}}^2 + \frac{1}{2}\cdot C_{oss}\cdot {V_{in}}^2 + \frac{1}{2}\cdot C_{TXp}\cdot {V_{in}}^2$$

ZVS Phase-Shifted Full-Bridge

3. Improved topology

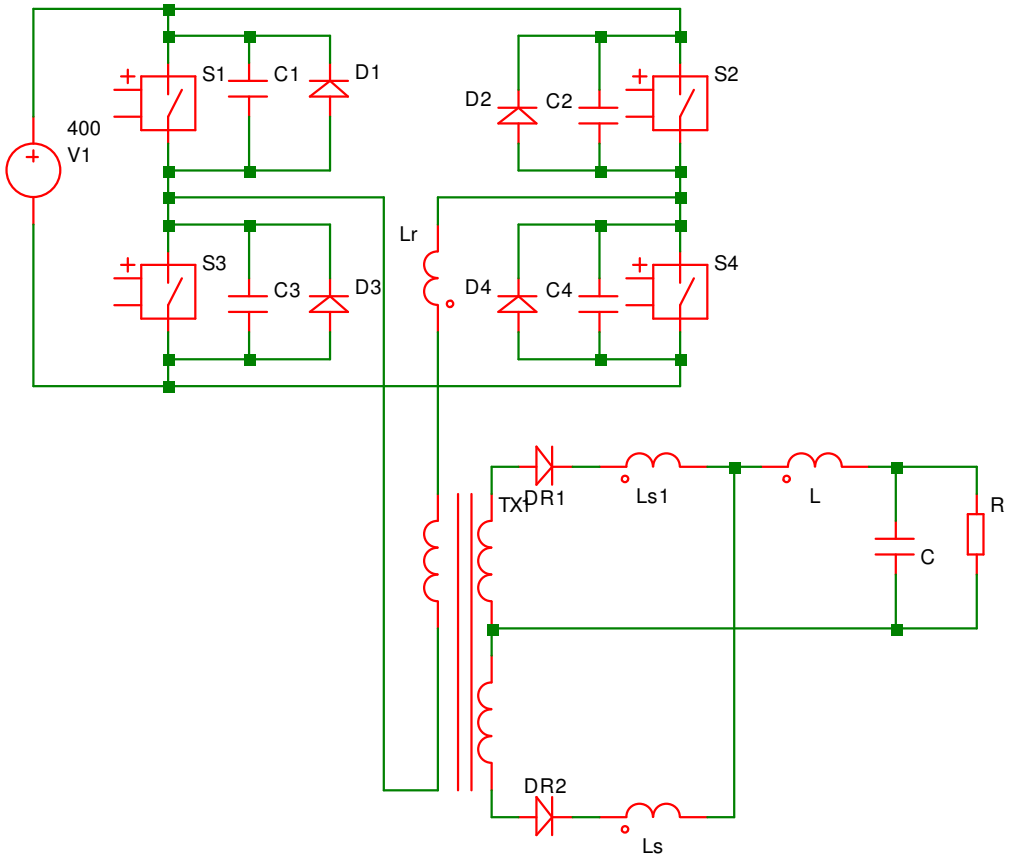


An improved zero-voltage-switched PWM converter using a saturable inductor, PESC 1991

a. Adding the saturable inductance at the primary

ZVS Phase-Shifted Full-Bridge

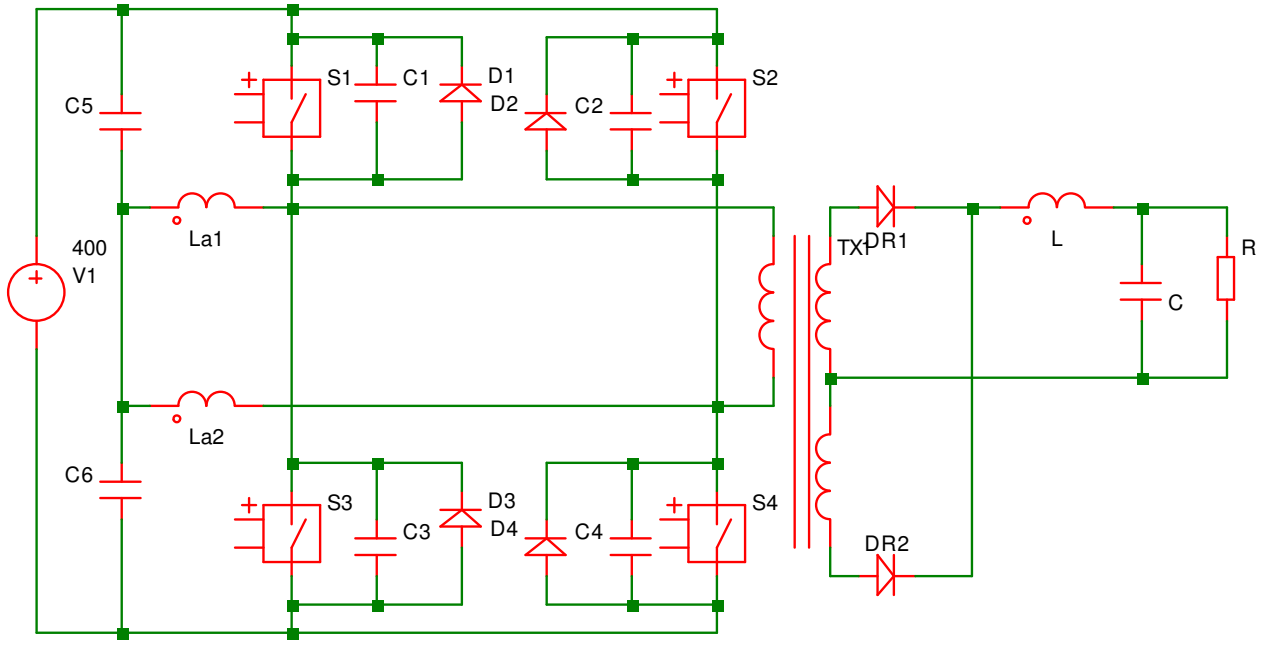
3. Improved topology



b. Utilizing the output filtering inductance

ZVS Phase-Shifted Full-Bridge

3. Improved topology



Analysis and design considerations of a load and line independent zero voltage switching full bridge DC-DC converter topology, IEEE PE 2002, with 97% efficiency

c. Auxiliary network

ZVS Phase-Shifted Full-Bridge

Practical Design Notes

- A series cap can't be added on the transformer primary due to voltage runaway in current mode operation.

- The extra drain capacitors must be returned directly to the source pole in the MOSFETs.

- If the CT located in total input path, the magnetic reset circuit must be used due to single quadrant operation. The CT must be outside any loop.

- Possible failure mode at light load: shoot through & Cdv/dt, at Heavy load: Trr of body diode

ZVS Phase-Shifted Full-Bridge

Limitations of Application

- The secondary switch voltage rating will be less than optimum for lower output voltage setting.

- For a given current, with transformer ratio fixed, the losses will remain same irrespective of the output voltage setting due to circulation current. This results in significant reduction in efficiency at lower output voltage.

- Poor transformer utilization at lower voltage setting

- Body diode conduction losses for primary MOSFETs.

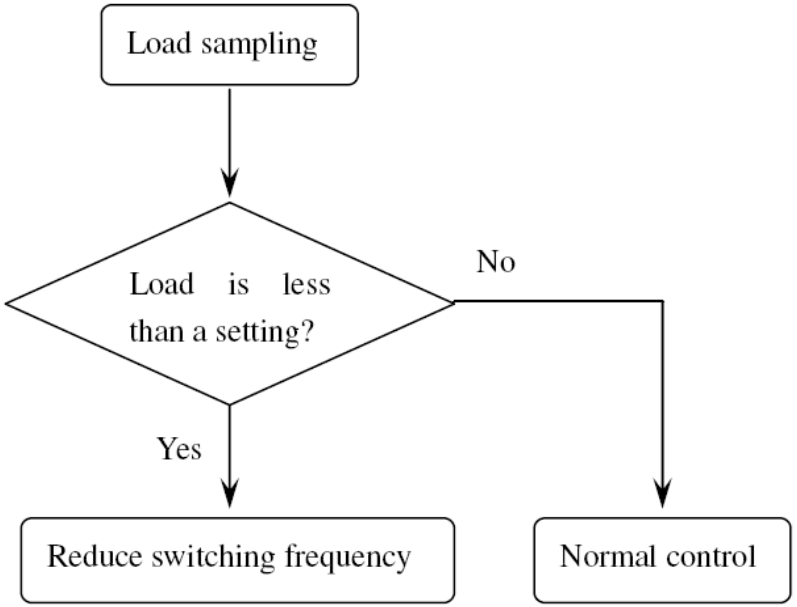
- Achieving ZVS for the entire load range becomes worse at lower output voltage setting due to narrow due to narrow duty cycle.

- Light load losses and primary MOSFET's body diode speed are primary concern at higher switching frequency.

ZVS Phase-Shifted Full-Bridge

Some Ideas in ZVS PS-FB

- **Switching Frequency Reduction at Light Load**
  - Reduced MOSFET switching losses
  - Reduced bias power consumption of drivers



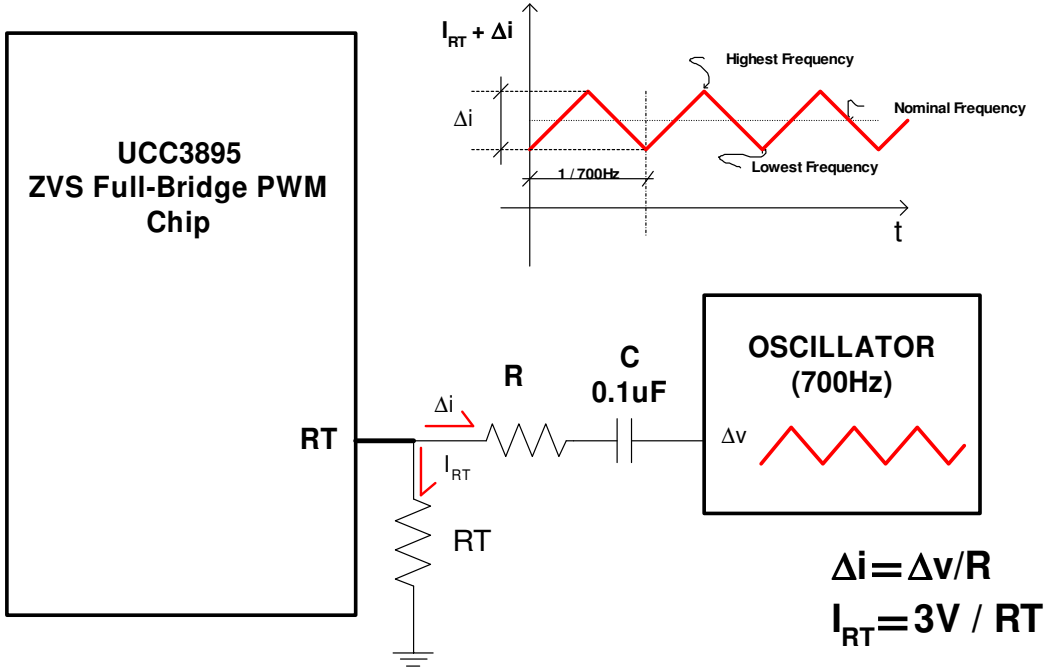
ZVS Phase-Shifted Full-Bridge

Some Ideas in ZVS PS-FB

- **Frequency Jittering**
  - Improve EMI

    . Reduce the average readings specially below 1MHz

    . Reduce the peak, quasi-peak beyond 10MHz



$f_{clk} = 2 \times fsw_{nom} = 1 / \{ [(5V/16) \times Ct / I_{rt}] + 120ns \}$

$fsw_{nom} \alpha I_{RT}$

$\Delta F = fsw_{high} - fsw_{low} = fsw_{nom} \times \Delta i / I_{RT}$

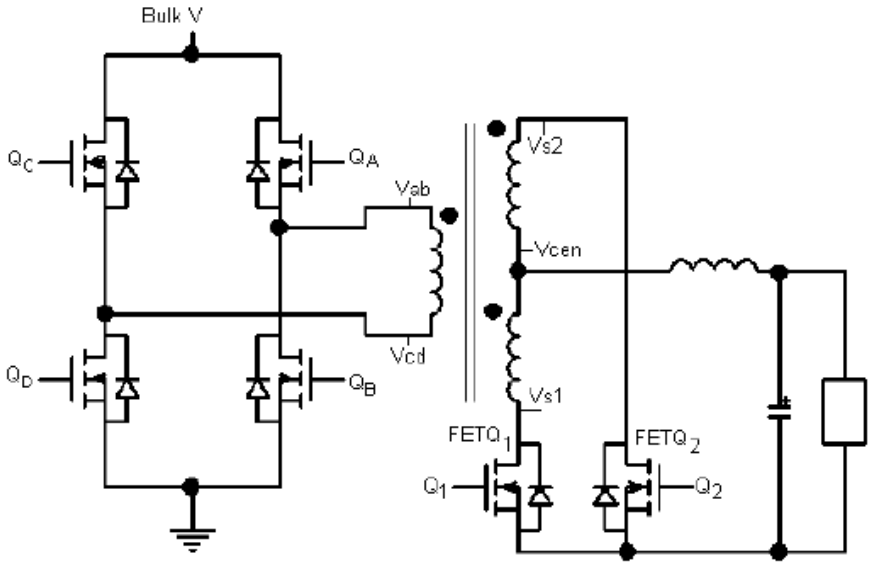
$fsw_{high} = fsw_{nom} \times [1 + (\Delta i / 2) \times (1/I_{RT})] = fsw_{nom} + \Delta F/2$

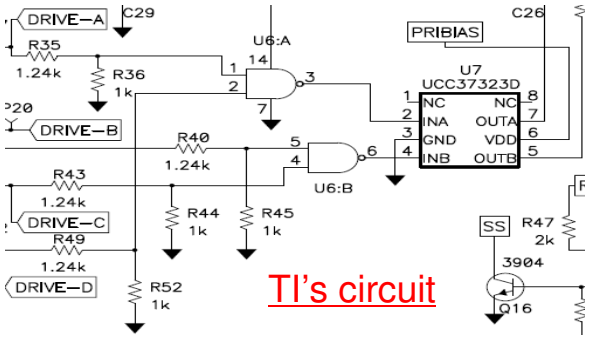
$fsw_{low} = fsw_{nom} \times [1 - (\Delta i / 2) \times (1/I_{RT})] = fsw_{nom} - \Delta F/2$

ZVS Phase-Shifted Full-Bridge

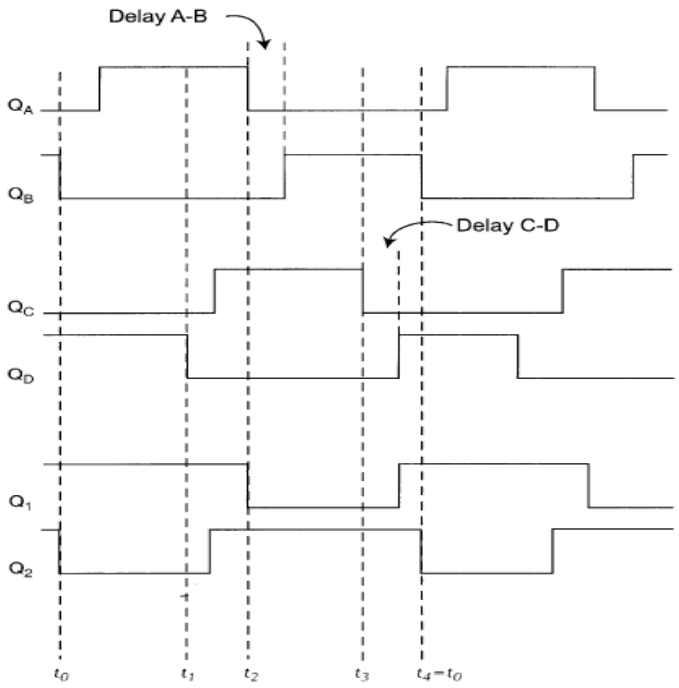
Some Ideas in ZVS PS-FB

- **Synchronous Rectification**



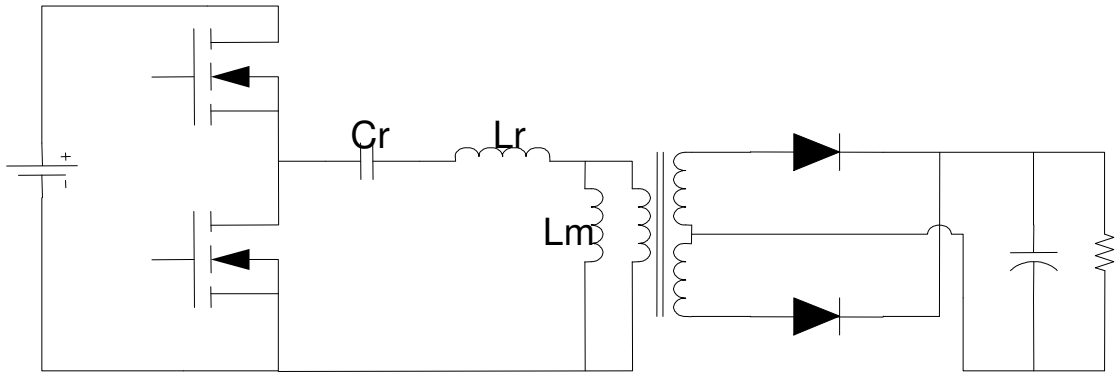


TI's circuit



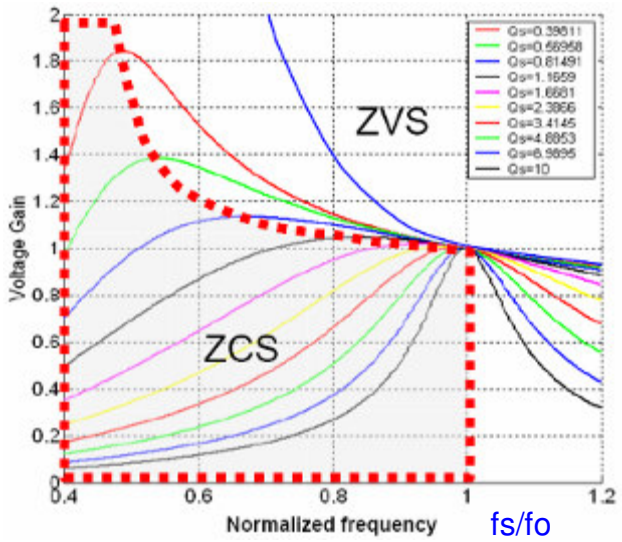
New circuit

LLC Series-Resonant Converter



- ZVS can be achieved by utilizing transformer magnetizing inductor
- Capacitor filter, low voltage stress on rectifiers
- Smaller switching loss due to small turn off current
- Wide operation range without reducing normal operation efficiency
- High operating frequency leads to high power density
- Improve the hold-up time
- Near ZCS for output rectifiers, less reverse recovery loss.

LLC Series-Resonant Converter



Lr, Cr, Lm

Resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}$$

Inductor Ratio

$$L_n = \frac{L_m}{L_r}$$

Characteristic Factor

$$Q = \frac{\sqrt{\frac{L_r}{C_r}}}{n^2 R}$$

LLC Series-Resonant Converter

Design Example

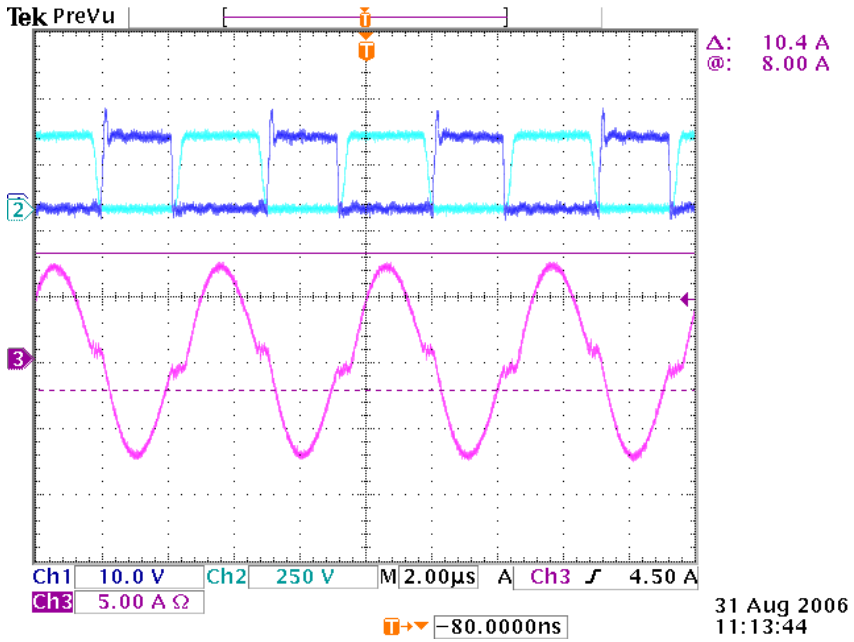
Po=1kW	Vin=260V	Vo=54.5V	fsw=200KHz
Q=0.1	Lm=136uH	Lr=1.1uH	fr=234KHz

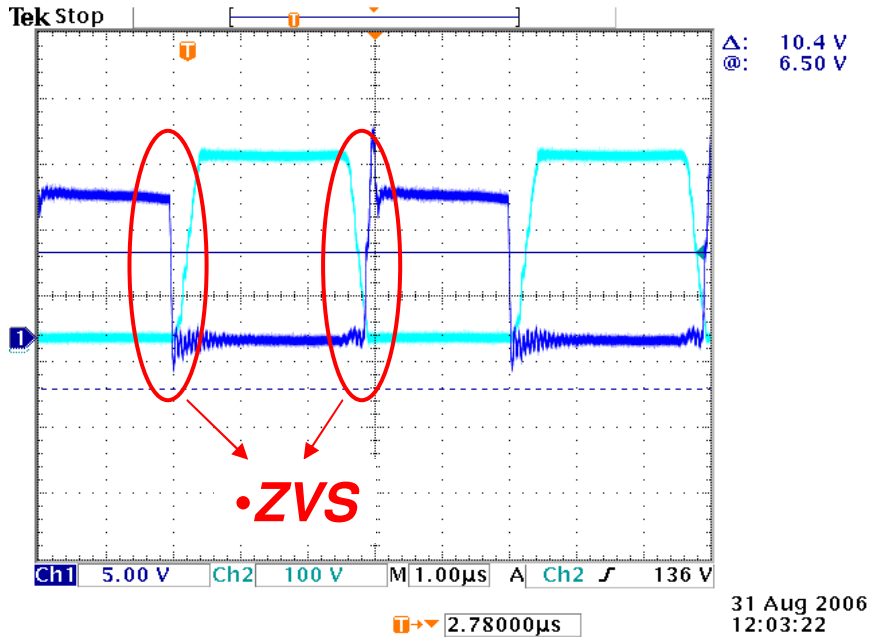
MOSFET	Cr	TX(Including Lm and Lr)	Rectifier	Co
STW26NM60*2	420nF	EE42/21/15 **Lr is the leakage inductance TX**	MUR2020*4	5mF(Single channel operation)

- **Operation efficiency: 96.5%**
- **ZVS has been achieved**
- **Vcr is closed to 160V**

LLC Series-Resonant Converter

Design Example





- Soft switching is achieved at full load low to 25% full load

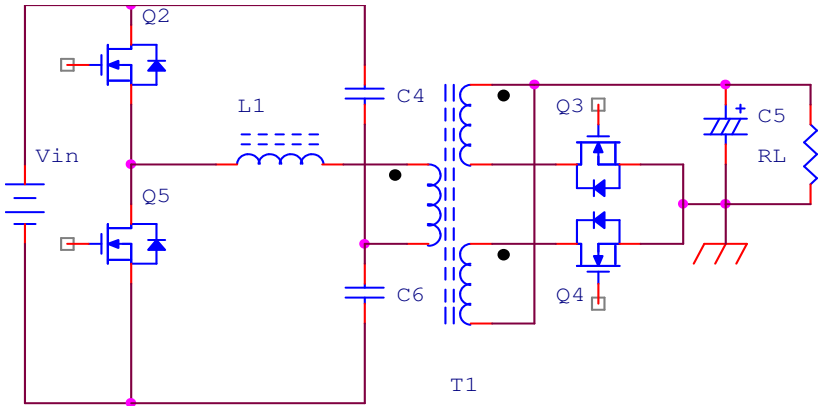
LLC Series-Resonant Converter

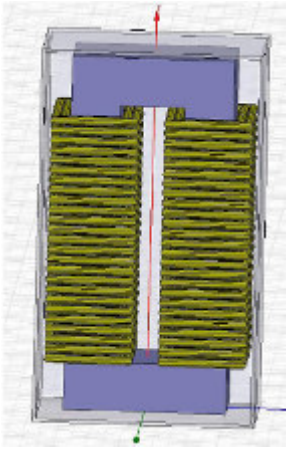
Observations:

- Operates best with fixed buck voltage or narrow range dynamic.
- Narrow regulation range
- High standby loss

Possibilities and variations:

- Burst mode at light load





LLC Series-Resonant Converter

Design Notes

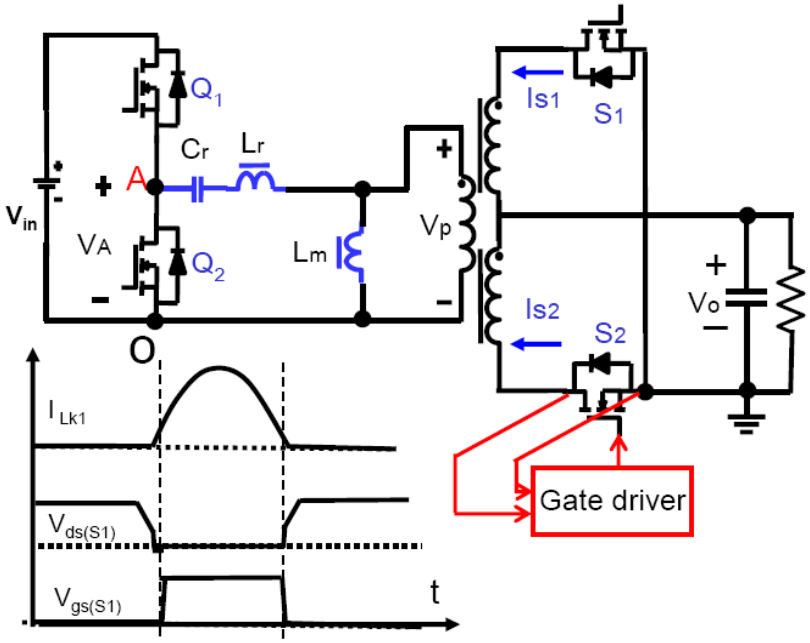
- fs a little lower than fr, main primary MOSFETs ZVS and near ZCS switching-off, secondary rectifiers ZCS, no Irr
- fs too low, bigger primary resonant peak current, effective duty cycle reduction, not good sine wave
- Lm/Lr: 3~5. If Lm/Lr too high, easily enter into ZCS region at heavy load. It will also result in wider operation frequency range.

Design Challenges

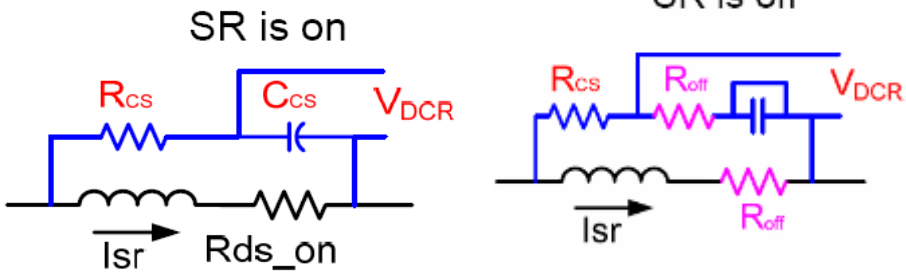
- Design is a iterative process.
- How to achieve resonant tank optical design
- How to achieve the synchronous rectification
- How to solve short-circuit protection
- How to limit operation frequency not too high at low output voltage or light load
- How to regulate the output voltage at light or no load.
- How to solve voltage gain not monotony at the boundary of region 1 and 2

LLC Series-Resonant Converter

SR Driving



The current on SR has different phase with voltage ZVS point A Vao and voltage on transformer Vpo for different fs --- self-driven can't be applied for LLC resonant converter.



$$Vcs(s) = \frac{Isr(s) \cdot Rds \cdot (1 + s \cdot Lsr / Rds)}{1 + s \cdot Rcs \cdot Ccs}$$

$$Rcs \cdot Ccs = \frac{Lsr}{Rds} \Rightarrow V_{cs} = V_{Rds\_on}$$

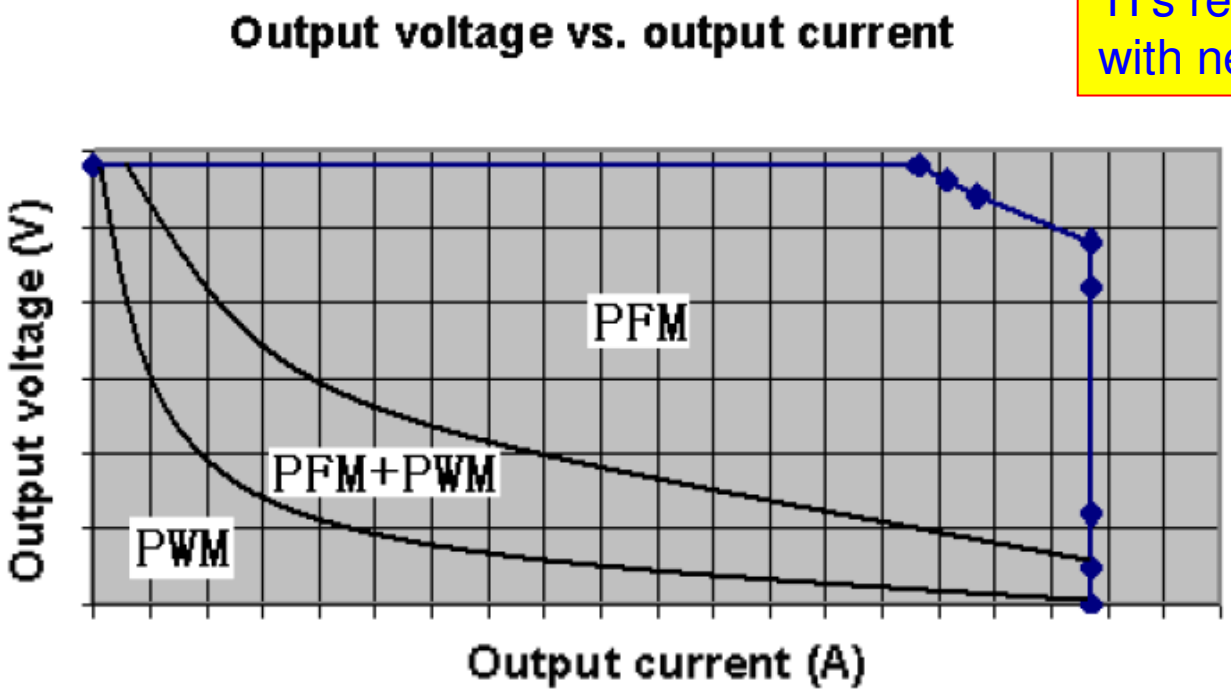
From CPES

- **Sense the Vds on SR**
- **Turn on SR when body diode of SR conducts current (e.g. Vds < -0.5V); Turn off SR when the current is close to zero (e.g. Vds > -5mV)**
- **TI driving IC? TPS28225, and predictive drive ucc27221?**
- **CM6900G from Champion-Micro**

LLC Series-Resonant Converter

Output Regulation at low Vout or light load

TI's resonant IC with new function?

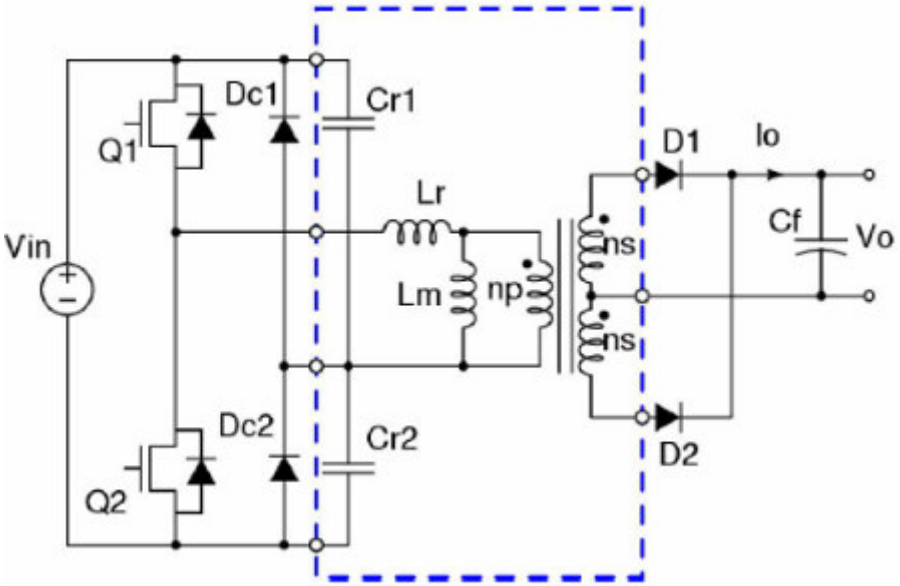


- Also improve voltage gain not monotony at the boundary of region 1 and 2

LLC Series-Resonant Converter

Output Short-Circuit Protection

If fs=fr, output short-circuit, Zall=0, very big primary current. Change operation frequency or resonant tank parameters



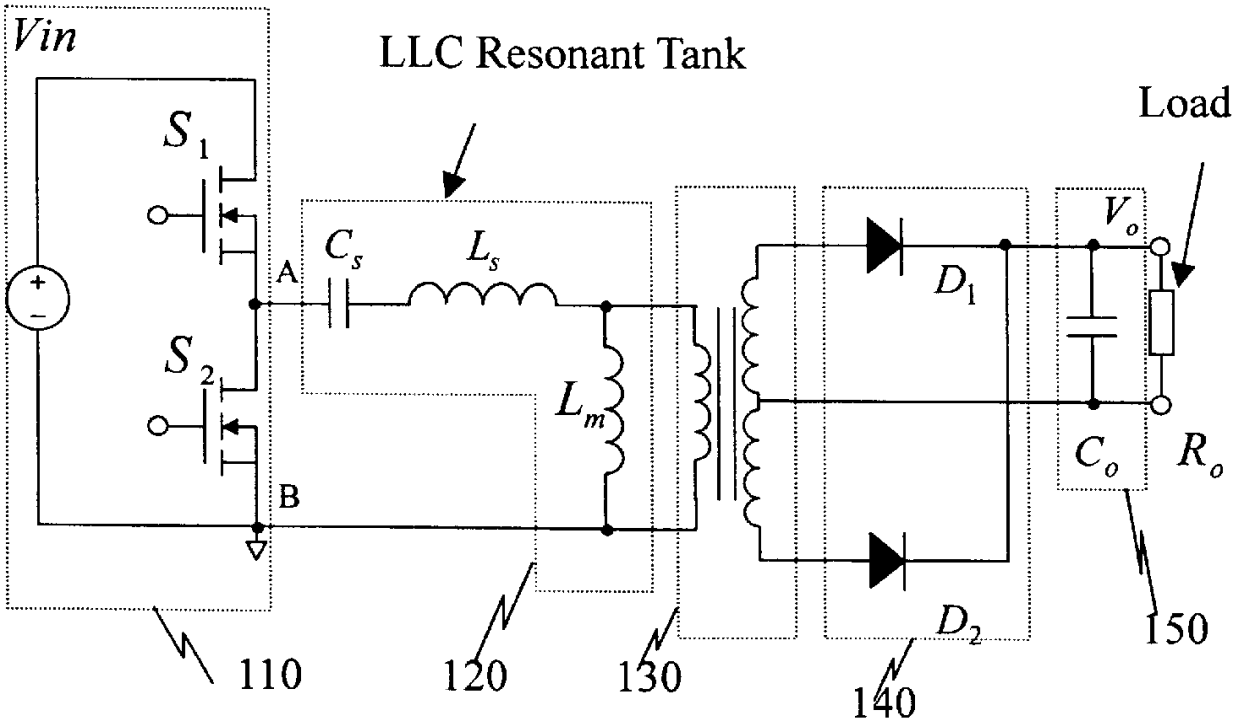
b. Fast outer-current loop and protection circuit, integrated into new control IC…

a. Cycle by cycle protection by clamping the resonant voltage with Dc1 and Dc2. Actually, the resonant capacitance impedance will be changed during output short-circuit (resonant tank), proposed in Yangbo's dissertation in CPES.

At the same time, it will result in lower input ripple current.

LLC Series-Resonant Converter

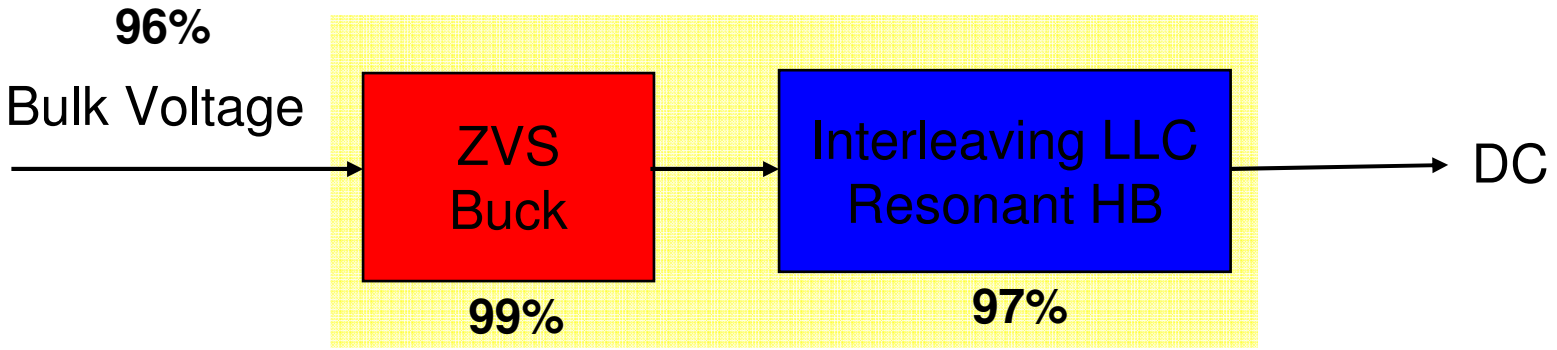
Patent Introduction



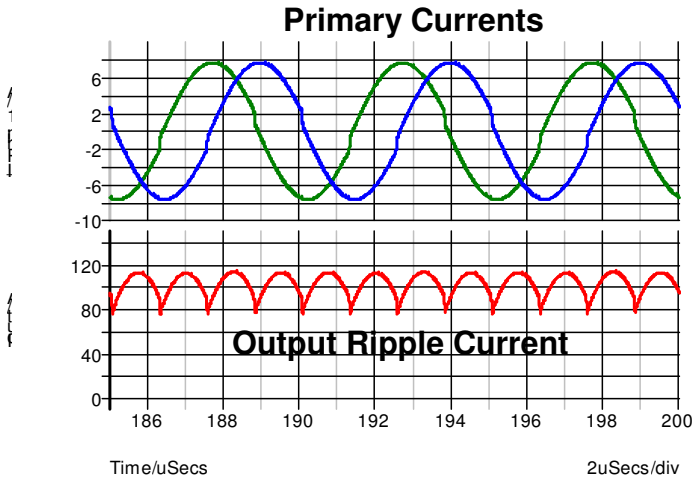
Delta patent, 2002, US # 6,344,979 B1

Buck Pre-Regulated Open Loop Resonant Converter

Circuit Topology



- **Sinusoidal currents**
  - Better EMI performance
  - No voltage spikes on the rectifiers
- **ZCS and ZVS over the full load range**
  - Low reverse recovery loss in the output rectifiers
  - High efficiency both at light load and full load
- **Disadvantages**
  - High output ripple current



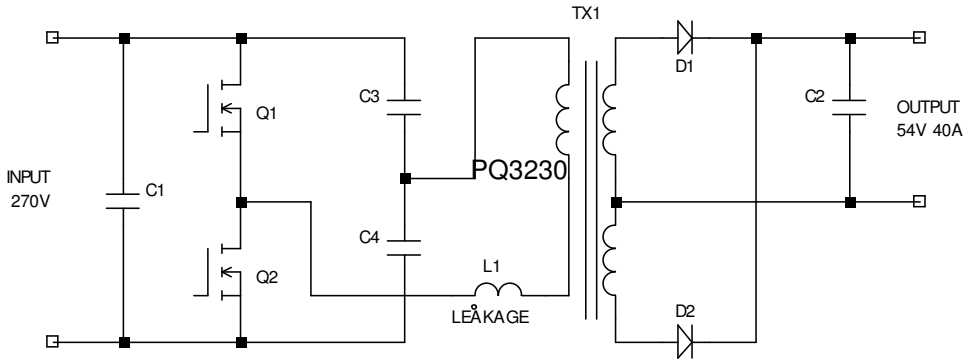
Buck Pre-Regulated Open Loop Resonant Converter

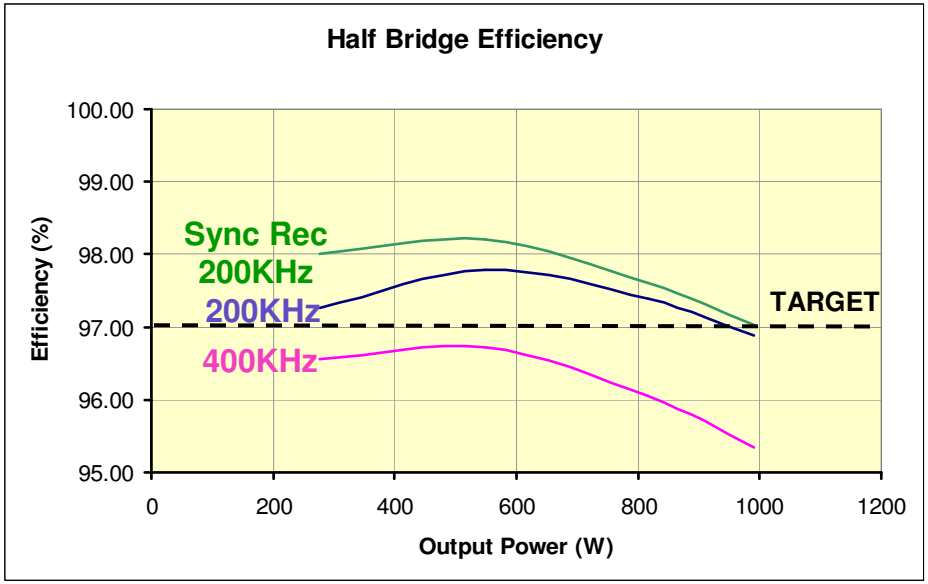
Circuit Topology

- Two resonant half bridges 90 degrees out of phase
  - Reduce output ripple current
- Buck pre-regulator regulates the output voltage
  - The resonant half bridges run at 100% duty cycle
  - Fixed switching frequency
- **The control strategy is very complex.**
  TI business opportunities (controls both of Buck and Resonant with interleaving operation)?

Buck Pre-Regulated Open Loop Resonant Converter

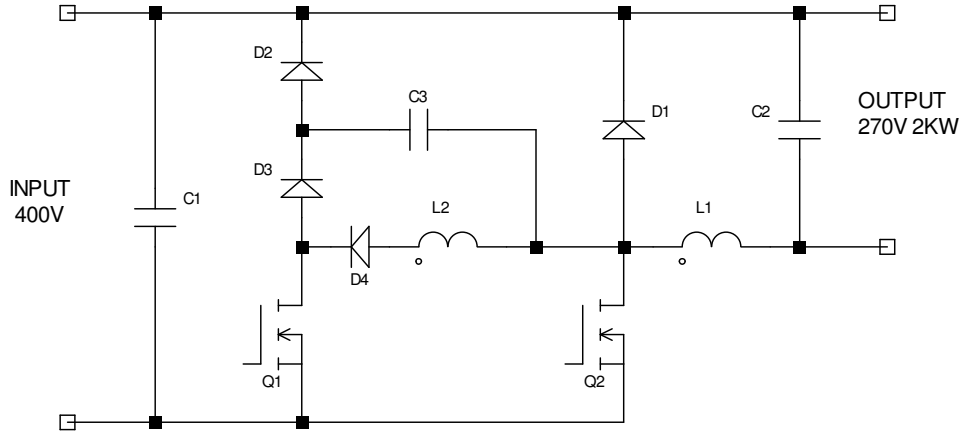
Efficiency of Open Loop LLC Resonant Converter

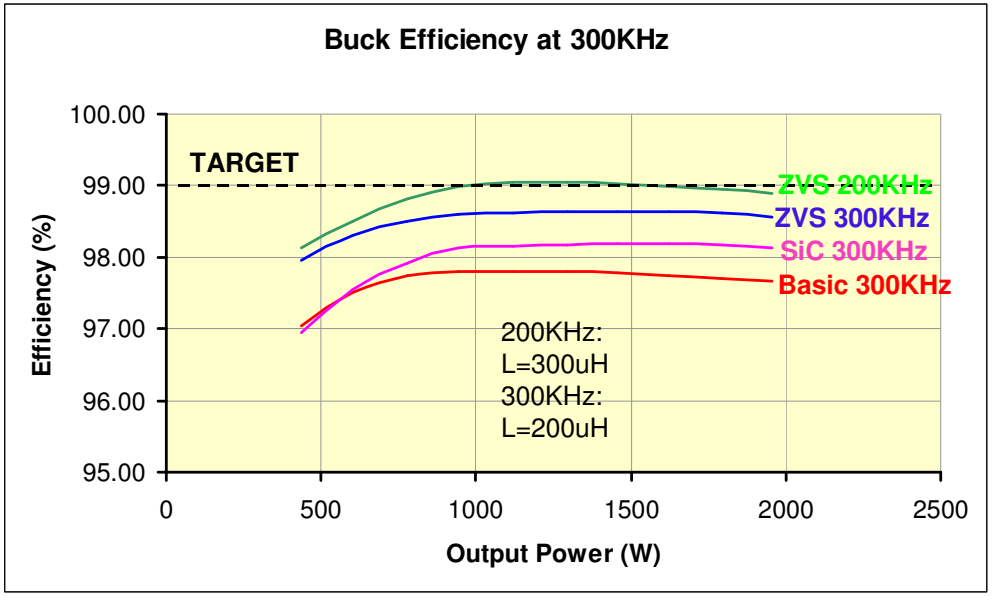




Buck Pre-Regulated Open Loop Resonant Converter

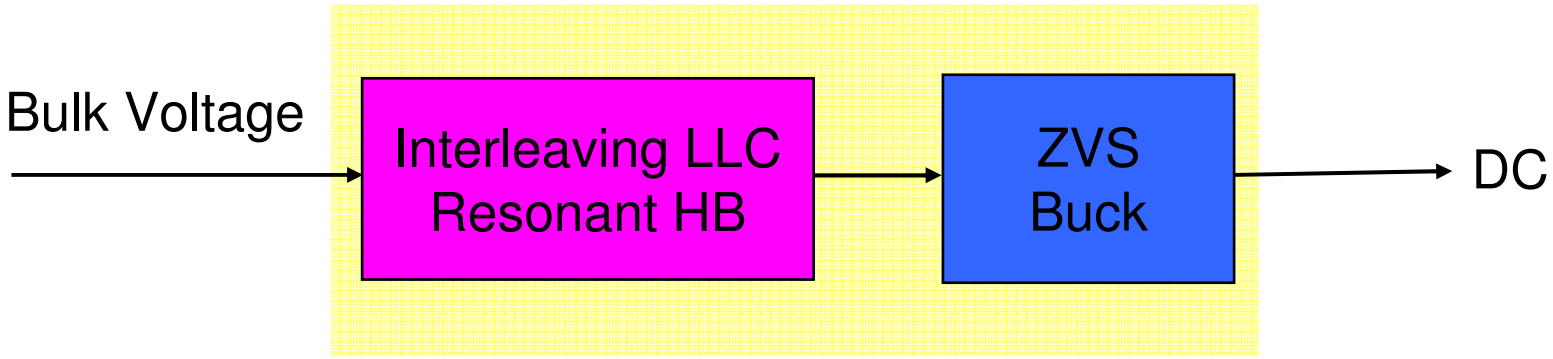
Efficiency of ZVS Buck





Buck Pre-Regulated Open Loop Resonant Converter

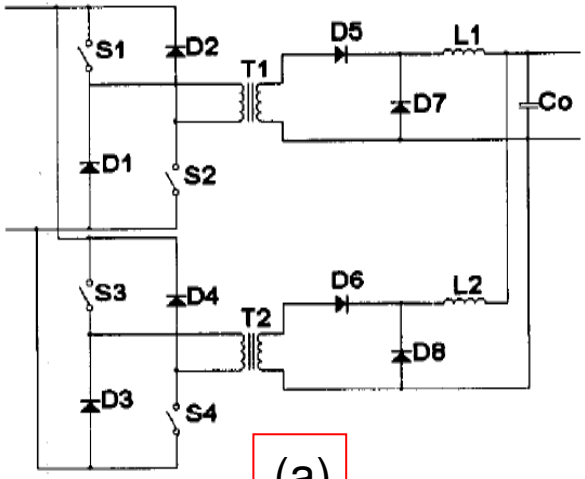
New Idea



Try it late!

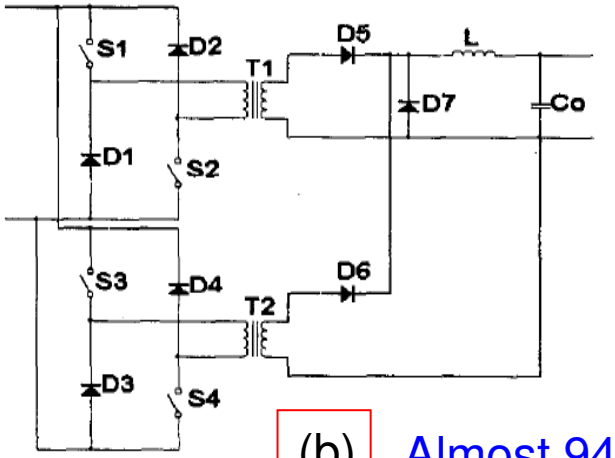
2-FETs Forward

Interleaving Methods



(a)

Ucc28220 new idea For SR!



(b) Almost 94% Effi

Comparison results:

In order to keep the same output ripple current, the inductance in (a) circuit should be twice of that in (b), e.g. L1=L2=2L

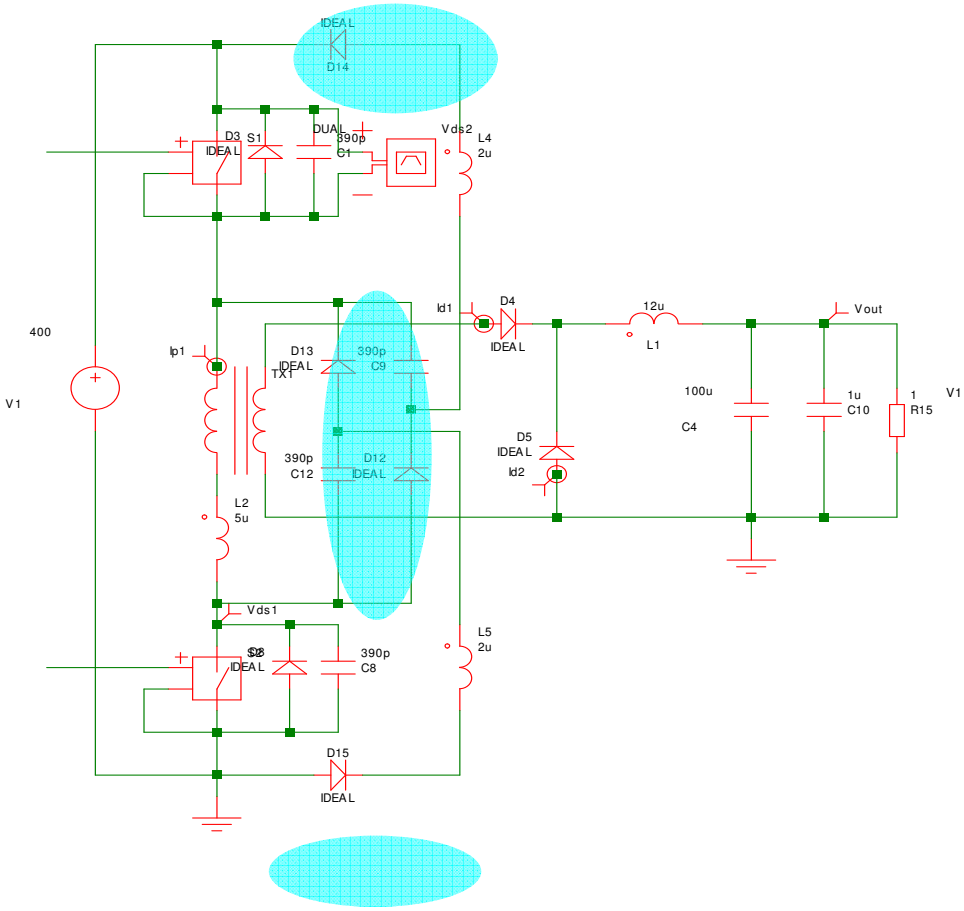
The inductance current frequency in (b) circuit is twice of that in (a) circuit.

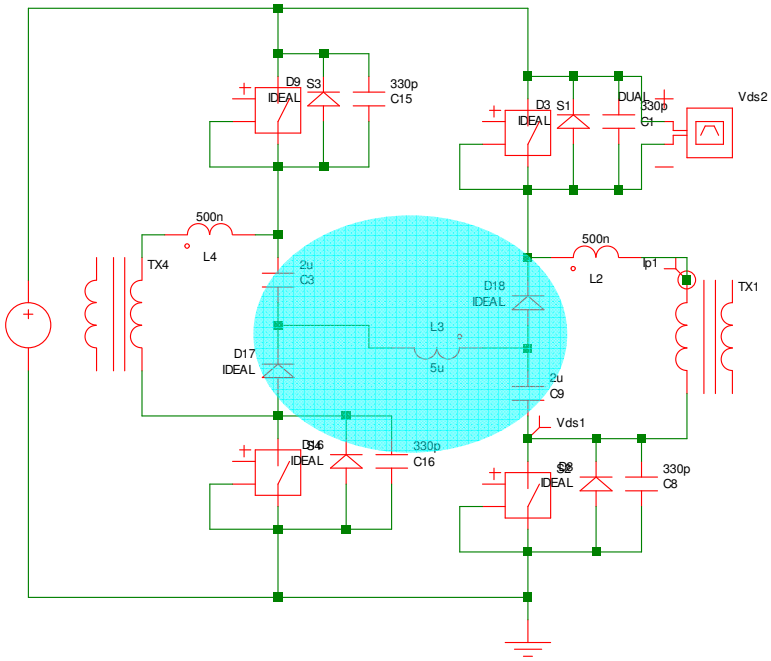
The voltage stresses of the main switches, clamping diodes, and rectifier diodes in both (a) and (b) circuits are the same.

The voltage stresses of freewheel diodes in (b) circuit is just half of that in (a) circuit.

2-FETs Forward

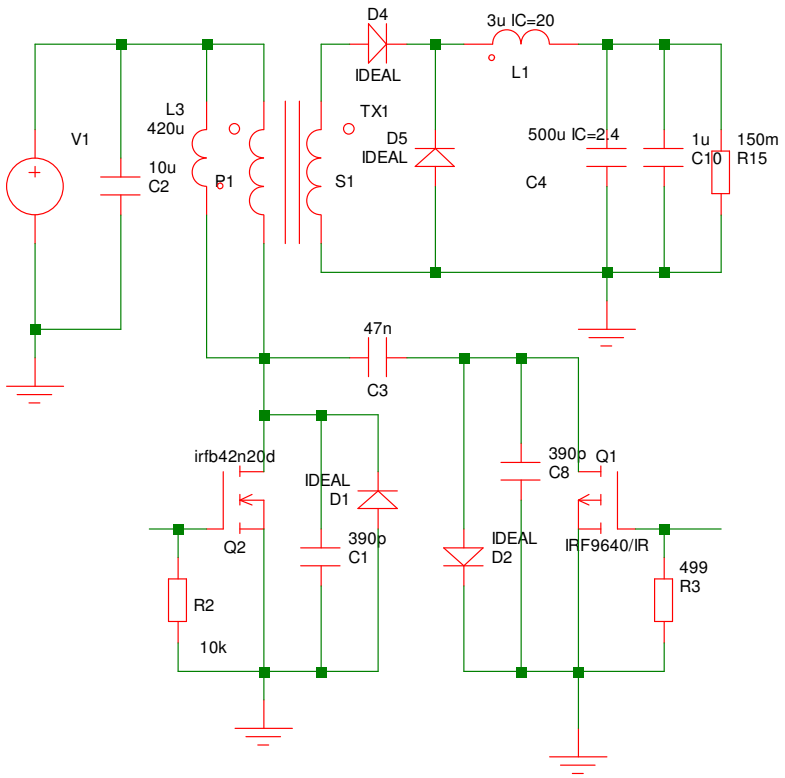
New Idea of Lossless Snubber





Active-Clamped Forward

Saturation Issue at Dynamics



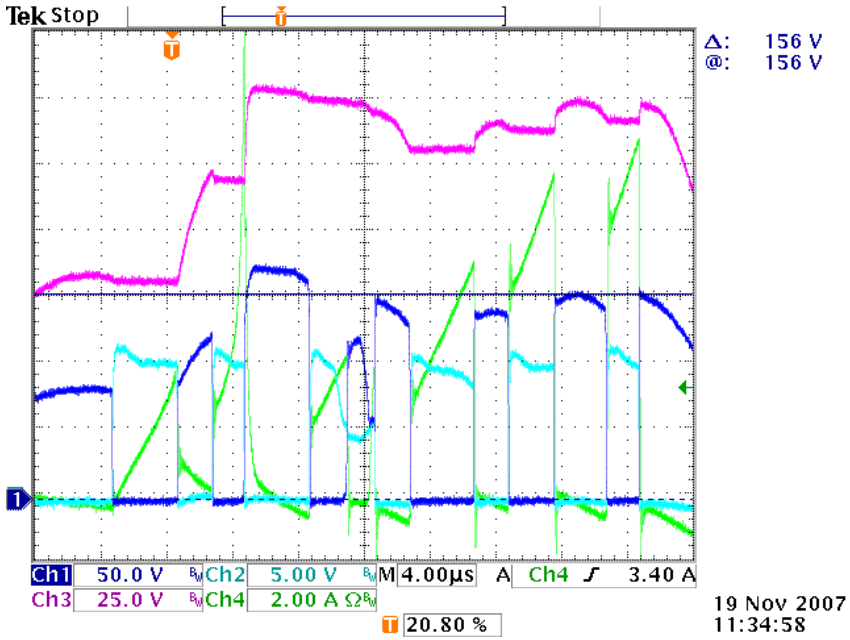
Refer to Huang Hong's presentation for other design considerations, "UCC2897_Design".

New SR Driving:

All signals from primary

Adaptive driving ucc27221?

CH1: main Vds; CH2: main Vgs; CH3: Vcr



Step load from 0 to 100%; Load: 2A/us

Active-Clamped Forward

Saturation Issue at Dynamics

Root Cause: **The saturation is caused by magnetic bias.**

Design conflicts: big Cr to reduce spike between main MOSFET, but deteriorate the dynamic performance. Big duty cycle improve dynamics, but possibly cause the magnetic core to be saturated.

D*Vin=(1-D)*Vcr.

Without load, Vcr is much low while D is very small operated in DCM. If it is instantly changed to heavy load, D will be very big to get to open loop duty with control circuit.

Due to much big Cr, the charging will be very slowly with much small magnetizing current. The v-t balance in the magnetizing inductance will be deteriorated. It will result the magnetic core can't reset, such that the core will close to be saturated.

Solution: **1) add the gap in the core. 2) current mode control**

ucc2891/2/3/4/7 advantages compared to LM5025!

Be careful: **It will also occur in the drive transformer in active-clamped forward!**

Q & A

Thank you!

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