

# 针对与 bq2416x 充电器控制器一起使用的电池管理单元 **Impedance Track™** 电量计

查询样品: **bq27530-G1**

## 特性

- 针对单节锂离子电池应用的电池电量计
- 驻留在系统主板上
- 基于已获专利的 **Impedance Track™** 技术的电池电量计
  - 可为准确续航时间预测建模电池放电曲线
  - 可针对电池老化、电池自放电以及温度/速率低效情况进行自动调节
  - 低值感应电阻器 (**5mΩ** 至 **20mΩ**)
- 具有可定制充电配置的电池充电器管理器
  - 可根据温度配置的充电电压和电流
  - 可选健康状态 (**SoH**) 和基于多级别的充电配置
- 无主机自主电池管理系统
  - 精简的软件开销可实现平台间的轻松可移植性以及更短代工生产 (**OEM**) 设计周期
  - 更高的可靠性和安全性
- 运行时间提升
  - 阻抗跟踪 (**Impedance Track**) 技术带来了更长的运行时间
  - 针对充电器终止的更加严密的精度控制
  - 经改进的再充电阈值
- 智能充电-定制的和自适应充电配置
  - 基于 **SoH** 的充电器控制
  - 温度水平充电 (**TLC**)
- 针对 **bq2416x** 单节开关模式电池充电器的电池充电器控制
  - 独立充电解决方案
- **400kHz I<sup>2</sup>C™** 用于与系统微处理器端口相连接的接口
- 采用 **15** 引脚 **NanoFree™ (CSP)** 封装内

## 应用范围

- 智能手机、功能型手机和平板电脑
- 数码相机与数码摄像机
- 手持终端设备
- **MP3** 或多媒体播放器

## 说明

德州仪器 (TI) 的 bq27530-G1 系统侧锂离子电池管理单元是一款微控制器外设，此外提供针对单节锂离子电池组的 **Impedance Track™** 电量检测和充电控制。此器件只需很少的系统微处理器固件开发。与 bq2416x 单节开关模式充电器一起使用，bq27530-G1 管理一个嵌入式电池（不可拆卸）或一个可拆卸电池组。

bq27530-G1 采用已获专利的 **Impedance Track™** 算法支持电量检测，可提供诸如剩余电池容量 (mAh)，充电状态 (%)，续航时间 (分钟)，电池电压 (mV)，温度 (°C) 以及健康状况 (%) 等信息。

通过 bq27530-G1 进行电池电量监测只需将 PACK+ (P+)，PACK- (P-) 以及热敏电阻 (T) 连接至可拆卸电池组或嵌入式电池电路。CSP 选项采用尺寸为 2.61mm × 1.96mm 的 15 焊球封装，引线间距为 0.5mm。它是空间受限应用的理想选择。



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English Data Sheet: [SLUSAL5](#)

# bq27530-G1

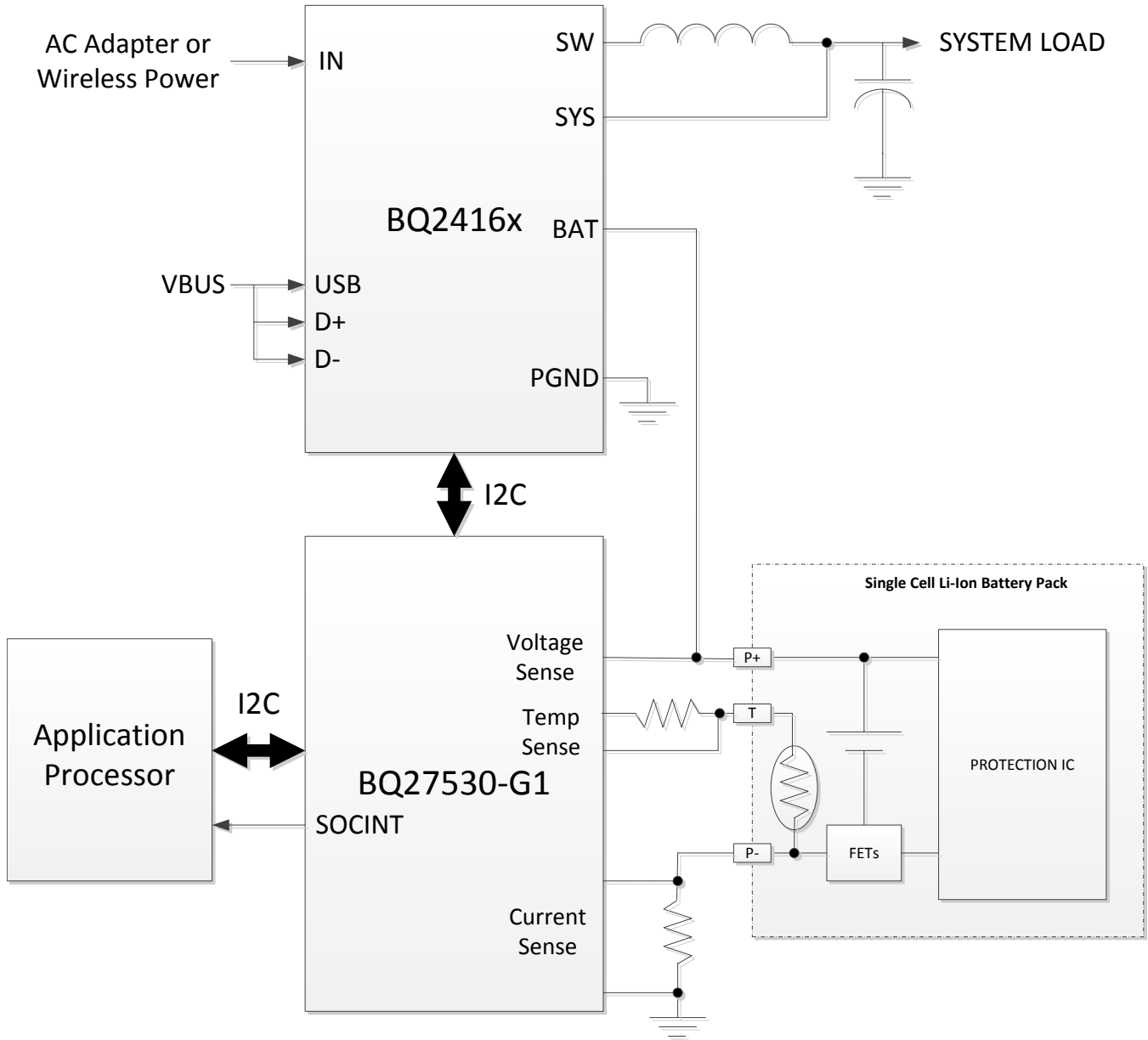
ZHCS240 – DECEMBER 2012

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## TYPICAL APPLICATION



## DEVICE INFORMATION

### AVAILABLE OPTIONS

PART NUMBER	FIRMWARE VERSION <sup>(1)</sup>	PACKAGE <sup>(2)</sup>	T <sub>A</sub>	COMMUNICATION FORMAT	TAPE and REEL QUANTITY
bq27530YZFR-G1	1.04 (0x0104)	CSP-15	–40°C to 85°C	I <sup>2</sup> C	3000
bq27530YZFT-G1					250

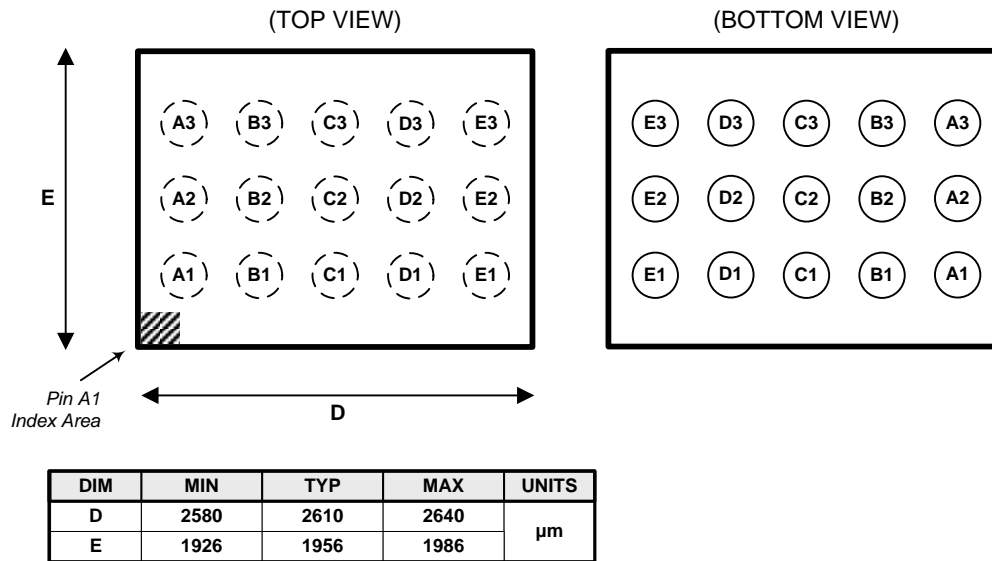
- (1) Refer to the *FW\_VERSION* subcommand to confirm the firmware version.  
 (2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		bq27530-G1	UNITS
		YZF(15 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	70	°C/W
$\theta_{JCTop}$	Junction-to-case (top) thermal resistance	17	
$\theta_{JB}$	Junction-to-board thermal resistance	20	
$\Psi_{JT}$	Junction-to-top characterization parameter	1	
$\Psi_{JB}$	Junction-to-board characterization parameter	18	
$\theta_{JCbott}$	Junction-to-case (bottom) thermal resistance	n/a	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#)

**PIN ASSIGNMENT AND PACKAGE DIMENSIONS**



**Table 1. PIN FUNCTIONS**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
SRP	A1	IA	Analog input pin connected to the internal coulomb counter where SRP is nearest the PACK– connection. Connect to 5-mΩ to 20-mΩ sense resistor.
SRN	B1	IA	Analog input pin connected to the internal coulomb counter where SRN is nearest the Vss connection. Connect to 5-mΩ to 20-mΩ sense resistor.
V <sub>SS</sub>	C1, C2	P	Device ground
V <sub>CC</sub>	D1	P	Regulator output and bq27530-G1 power. Decouple with 1μF ceramic capacitor to Vss.
REGIN	E1	P	Regulator input. Decouple with 0.1μF ceramic capacitor to Vss.
SOC_INT	A2	I/O	SOC state interrupts output. Generates a pulse as described in <i>bq27530-G1 Technical Reference Manual</i> . Open drain output.
BSCCL	B2	O	Battery Charger clock output line for chipset communication. Push-pull output. <b>Note:</b> CE has an internal ESD protection diode connected to REGIN. Recommend maintaining V <sub>CE</sub> ≤ V <sub>REGIN</sub> under all conditions.
CE	D2	I	Chip Enable. Internal LDO is disconnected from REGIN when driven low.
BAT	E2	I	Cell-voltage measurement input. ADC input. Recommend 4.8V maximum for conversion accuracy.
SCL	A3	I	Slave I <sup>2</sup> C serial communications clock input line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical).
SDA	B3	I/O	Slave I <sup>2</sup> C serial communications data line for communication with system (Master). Open-drain I/O. Use with 10kΩ pull-up resistor (typical).
BSDA	C3	I/O	Battery Charger data line for chipset communication. Push-pull output.
TS	D3	IA	Pack thermistor voltage sense (use 103AT-type thermistor). ADC input.
BI/TOUT	E3	I/O	Battery-insertion detection input. Power pin for pack thermistor network. Thermistor-multiplexer control pin. Use with pull-up resistor >1MΩ (1.8 MΩ typical).

(1) I/O = Digital input/output, IA = Analog input, P = Power connection

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

PARAMETER		VALUE	UNIT
V <sub>REGIN</sub>	Regulator input range	-0.3 to 5.5	V
		-0.3 to 6.0 <sup>(2)</sup>	V
V <sub>CE</sub>	CE input pin	-0.3 to V <sub>REGIN</sub> + 0.3	V
V <sub>CC</sub>	Supply voltage range	-0.3 to 2.75	V
V <sub>IOD</sub>	Open-drain I/O pins (SDA, SCL, SOC_INT)	-0.3 to 5.5	V
V <sub>BAT</sub>	BAT input pin	-0.3 to 5.5	V
		-0.3 to 6.0 <sup>(2)</sup>	V
V <sub>I</sub>	Input voltage range to all other pins (BI/TOUT, TS, SRP, SRN, BSDA, BSCL)	-0.3 to V <sub>CC</sub> + 0.3	V
ESD	Human-body model (HBM), BAT pin	1.5	kV
	Human-body model (HBM), all other pins	2	
T <sub>A</sub>	Operating free-air temperature range	-40 to 85	°C
T <sub>stg</sub>	Storage temperature range	-65 to 150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Condition not to exceed 100 hours at 25 °C lifetime.

### RECOMMENDED OPERATING CONDITIONS

T<sub>A</sub> = -40°C to 85°C, V<sub>REGIN</sub> = V<sub>BAT</sub> = 3.6V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>REGIN</sub>	Supply voltage	2.8		4.5	V
	No operating restrictions			2.8	
C <sub>REGIN</sub>	External input capacitor for internal LDO between REGIN and V <sub>SS</sub>	Nominal capacitor values specified. Recommend a 5% ceramic X5R type capacitor located close to the device.		0.1	μF
C <sub>LDO25</sub>	External output capacitor for internal LDO between V <sub>CC</sub> and V <sub>SS</sub>	0.47	1		μF
t <sub>PUCD</sub>	Power-up communication delay		250		ms

### SUPPLY CURRENT

T<sub>A</sub> = 25°C and V<sub>REGIN</sub> = V<sub>BAT</sub> = 3.6V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>CC</sub> <sup>(1)</sup>	Normal operating-mode current Fuel gauge in NORMAL mode. I <sub>LOAD</sub> > <b>Sleep Current</b>		118		μA
I <sub>SLEEP+</sub> <sup>(1)</sup>	Sleep+ operating mode current Fuel gauge in SLEEP+ mode. I <sub>LOAD</sub> < <b>Sleep Current</b>		62		μA
I <sub>SLEEP</sub> <sup>(1)</sup>	Low-power storage-mode current Fuel gauge in SLEEP mode. I <sub>LOAD</sub> < <b>Sleep Current</b>		23		μA
I <sub>HIB</sub> <sup>(1)</sup>	Hibernate operating-mode current Fuel gauge in HIBERNATE mode. I <sub>LOAD</sub> < <b>Hibernate Current</b>		8		μA

- (1) Specified by design. Not production tested.

## DIGITAL INPUT AND OUTPUT DC CHARACTERISTICS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{\text{REGIN}} = 3.6\text{ V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{OL}}$	Output voltage, low (SCL, SDA, SOC_INT, BSDA, BSCL)	$I_{\text{OL}} = 3\text{ mA}$			0.4	V
$V_{\text{OH(PP)}}$	Output voltage, high (BSDA, BSCL)	$I_{\text{OH}} = -1\text{ mA}$	$V_{\text{CC}} - 0.5$			V
$V_{\text{OH(OD)}}$	Output voltage, high (SDA, SCL, SOC_INT)	External pullup resistor connected to $V_{\text{CC}}$	$V_{\text{CC}} - 0.5$			
$V_{\text{IL}}$	Input voltage, low (SDA, SCL)		-0.3		0.6	V
	Input voltage, low (BI/TOUT)	BAT INSERT CHECK MODE active	-0.3		0.6	
$V_{\text{IH}}$	Input voltage, high (SDA, SCL)		1.2			V
	Input voltage, high (BI/TOUT)	BAT INSERT CHECK MODE active	1.2		$V_{\text{CC}} + 0.3$	
$V_{\text{IL(CE)}}$	Input voltage, low (CE)	$V_{\text{REGIN}} = 2.8$ to $4.5\text{ V}$			0.8	V
$V_{\text{IH(CE)}}$	Input voltage, high (CE)				2.65	
$I_{\text{Ikg}}^{(1)}$	Input leakage current (I/O pins)				0.3	$\mu\text{A}$

(1) Specified by design. Not production tested.

## POWER-ON RESET

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ , typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{\text{REGIN}} = 3.6\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{IT+}}$	Positive-going battery voltage input at $V_{\text{CC}}$	2.05	2.15	2.20	V
$V_{\text{HYS}}$	Power-on reset hysteresis	45	115	185	mV

## 2.5V LDO REGULATOR

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $C_{\text{LDO25}} = 1\mu\text{F}$ ,  $V_{\text{REGIN}} = 3.6\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{\text{REG25}}$	$2.8\text{ V} \leq V_{\text{REGIN}} \leq 4.5\text{ V}$ , $I_{\text{OUT}} \leq 16\text{ mA}$	2.3	2.5	2.6	V
	$2.45\text{ V} \leq V_{\text{REGIN}} < 2.8\text{ V}$ (low battery), $I_{\text{OUT}} \leq 3\text{ mA}$	2.3			V

## INTERNAL CLOCK OSCILLATORS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $2.4\text{ V} < V_{\text{CC}} < 2.6\text{ V}$ ; typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{\text{CC}} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{OSC}}$	High Frequency Oscillator		2.097		MHz
$f_{\text{LOSC}}$	Low Frequency Oscillator		32.768		kHz

## ADC (TEMPERATURE AND CELL MEASUREMENT) CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $2.4\text{ V} < V_{CC} < 2.6\text{ V}$ ; typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{ADC1}}$	Input voltage range (TS)	$V_{\text{SS}} - 0.125$		2	V
$V_{\text{ADC2}}$	Input voltage range (BAT)	$V_{\text{SS}} - 0.125$		5	V
$V_{\text{IN(ADC)}}$	Input voltage range	0.05		1	V
$G_{\text{TEMP}}$	Internal temperature sensor voltage gain		-2		mV/ $^{\circ}\text{C}$
$t_{\text{ADC\_CONV}}$	Conversion time			125	ms
	Resolution	14		15	bits
$V_{\text{OS(ADC)}}$	Input offset		1		mV
$Z_{\text{ADC1}}$ <sup>(1)</sup>	Effective input resistance (TS)	8			M $\Omega$
$Z_{\text{ADC2}}$ <sup>(1)</sup>	Effective input resistance (BAT)	bq27530-G1 not measuring cell voltage			M $\Omega$
		bq27530-G1 measuring cell voltage		100	k $\Omega$
$I_{\text{lkq(ADC)}}$ <sup>(1)</sup>	Input leakage current			0.3	$\mu\text{A}$

(1) Specified by design. Not tested in production.

## INTEGRATING ADC (COULOMB COUNTER) CHARACTERISTICS

$T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $2.4\text{ V} < V_{CC} < 2.6\text{ V}$ ; typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{\text{SR}}$	Input voltage range, $V_{\text{(SRP)}}$ and $V_{\text{(SRN)}}$	$V_{\text{SR}} = V_{\text{(SRP)}} - V_{\text{(SRN)}}$		-0.125	0.125	V
$t_{\text{SR\_CONV}}$	Conversion time	Single conversion				
	Resolution	14	1	15	s	
$V_{\text{OS(SR)}}$	Input offset		10		$\mu\text{V}$	
INL	Integral nonlinearity error		$\pm 0.007$	$\pm 0.034$	% FSR	
$Z_{\text{IN(SR)}}$ <sup>(1)</sup>	Effective input resistance	2.5			M $\Omega$	
$I_{\text{lkq(SR)}}$ <sup>(1)</sup>	Input leakage current			0.3	$\mu\text{A}$	

(1) Specified by design. Not tested in production.

## DATA FLASH MEMORY CHARACTERISTICS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $2.4\text{ V} < V_{CC} < 2.6\text{ V}$ ; typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 2.5\text{ V}$  (unless otherwise noted)

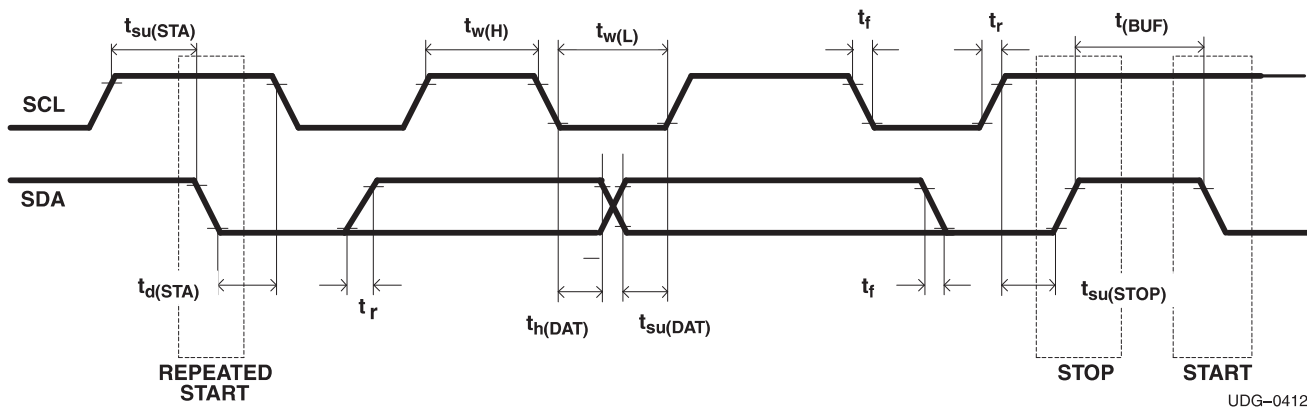
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{DR}^{(1)}$	Data retention	10			Years
	Flash-programming write cycles <sup>(1)</sup>	20,000			Cycles
$t_{WORDPROG}^{(1)}$	Word programming time			2	ms
$I_{CCPROG}^{(1)}$	Flash-write supply current		5	10	mA
$t_{DFERASE}^{(1)}$	Data flash master erase time	200			ms
$t_{IFERASE}^{(1)}$	Instruction flash master erase time	200			ms
$t_{PGERASE}^{(1)}$	Flash page erase time	20			ms

(1) Specified by design. Not production tested

## I<sup>2</sup>C-COMPATIBLE INTERFACE COMMUNICATION TIMING CHARACTERISTICS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $2.4\text{ V} < V_{CC} < 2.6\text{ V}$ ; typical values at  $T_A = 25^{\circ}\text{C}$  and  $V_{CC} = 2.5\text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	SCL/SDA rise time			300	ns
$t_f$	SCL/SDA fall time			300	ns
$t_{w(H)}$	SCL pulse duration (high)	600			ns
$t_{w(L)}$	SCL pulse duration (low)	1.3			$\mu\text{s}$
$t_{su(STA)}$	Setup for repeated start	600			ns
$t_{d(STA)}$	Start to first falling edge of SCL	600			ns
$t_{su(DAT)}$	Data setup time	100			ns
$t_{h(DAT)}$	Data hold time	0			ns
$t_{su(STOP)}$	Setup time for stop	600			ns
$t_{(BUF)}$	Bus free time between stop and start	66			$\mu\text{s}$
$f_{SCL}$	Clock frequency <sup>(1)</sup>			400	kHz

 (1) If the clock frequency ( $f_{SCL}$ ) is  $> 100\text{ kHz}$ , use 1-byte write commands for proper operation. All other transactions types are supported at 400 kHz. (Refer to [I<sup>2</sup>C INTERFACE](#) and [I<sup>2</sup>C Command Waiting Time](#))

**Figure 1. I<sup>2</sup>C-Compatible Interface Timing Diagrams**



## GENERAL DESCRIPTION

The bq27530-G1 accurately predicts the battery capacity and other operational characteristics of a single Li-based rechargeable cell. It can be interrogated by a system processor to provide cell information, such as time-to-empty (TTE), and state-of-charge (SOC) as well as SOC interrupt signal to the host.

The bq27530-G1 can control a bq2416x Charger IC without the intervention from an application system processor. Using the bq27530-G1 and bq2416x chipset, batteries can be charged with the typical constant-current, constant voltage (CCCV) profile or charged using a Multi-Level Charging (MLC) algorithm.

Information is accessed through a series of commands, called *Standard Commands*. Further capabilities are provided by the additional *Extended Commands* set. Both sets of commands, indicated by the general format *Command( )*, are used to read and write information contained within the device control and status registers, as well as its data flash locations. Commands are sent from system to gauge using the bq27530-G1's I<sup>2</sup>C serial communications engine, and can be executed during application development, pack manufacture, or end-equipment operation.

Cell information is stored in the device in non-volatile flash memory. Many of these data flash locations are accessible during application development. They cannot, generally, be accessed directly during end-equipment operation. Access to these locations is achieved by either use of the bq27530-G1's companion evaluation software, through individual commands, or through a sequence of data-flash-access commands. To access a desired data flash location, the correct data flash subclass and offset must be known.

The key to the bq27530-G1 high-accuracy gas gauging prediction is Texas Instrument's proprietary Impedance Track™ algorithm. This algorithm uses cell measurements, characteristics, and properties to create state-of-charge predictions that can achieve less than 1% error across a wide variety of operating conditions and over the lifetime of the battery.

The device measures battery charge/discharge activity by monitoring the voltage across a small-value series sense resistor (5 mΩ to 20 mΩ typ.) located between the system's V<sub>SS</sub> and the battery's PACK- terminal. When a cell is attached to the device, cell impedance is computed, based on cell current, cell open-circuit voltage (OCV), and cell voltage under loading conditions.

The device external temperature sensing is optimized with the use of a high accuracy negative temperature coefficient (NTC) thermistor with R<sub>25</sub> = 10.0kΩ ±1%, B<sub>25/85</sub> = 3435K ± 1% (such as Semitec NTC 103AT). The bq27530-G1 can also be configured to use its internal temperature sensor. When an external thermistor is used, a 18.2k pull up resistor between BI/TOUT and TS pins is also required. The bq27530-G1 uses temperature to monitor the battery-pack environment, which is used for fuel gauging and cell protection functionality.

To minimize power consumption, the device has different power modes: NORMAL, SLEEP, SLEEP+, HIBERNATE, and BAT INSERT CHECK. The bq27530-G1 passes automatically between these modes, depending upon the occurrence of specific events, though a system processor can initiate some of these modes directly.

For complete operational details, refer to [bq27530-G1 Technical Reference Manual](#).

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### NOTE

#### FORMATTING CONVENTIONS IN THIS DOCUMENT:

Commands: *italics* with parentheses and no breaking spaces, e.g., *RemainingCapacity( )*

Data flash: *italics*, **bold**, and *breaking spaces*, e.g., **Design Capacity**

Register bits and flags: brackets and *italics*, e.g., [TDA]

Data flash bits: brackets, *italics* and **bold**, e.g., [LED1]

Modes and states: ALL CAPITALS, e.g., UNSEALED mode.

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## DATA COMMANDS

### STANDARD DATA COMMANDS

The bq27530-G1 uses a series of 2-byte standard commands to enable system reading and writing of battery information. Each standard command has an associated command-code pair, as indicated in [Table 2](#). Because each command consists of two bytes of data, two consecutive I<sup>2</sup>C transmissions must be executed both to initiate the command function, and to read or write the corresponding two bytes of data. Additional details are found in the [bq27530-G1 Technical Reference Manual](#).

**Table 2. Standard Commands**

NAME	COMMAND CODE	UNITS	SEALED ACCESS	UNSEALED ACCESS
<i>Control()</i>	0x00 / 0x01	N/A	R/W	R/W
<i>AtRate()</i>	0x02 / 0x03	mA	R/W	R/W
<i>AtRateTimeToEmpty()</i>	0x04 / 0x05	Minutes	R	R/W
<i>Temperature()</i>	0x06 / 0x07	0.1 K	R/W	R/W
<i>Voltage()</i>	0x08 / 0x09	mV	R	R/W
<i>Flags()</i>	0x0a / 0x0b	N/A	R	R/W
<i>NominalAvailableCapacity()</i>	0x0c / 0x0d	mAh	R	R/W
<i>FullAvailableCapacity()</i>	0x0e / 0x0f	mAh	R	R/W
<i>RemainingCapacity()</i>	0x10 / 0x11	mAh	R	R/W
<i>FullChargeCapacity()</i>	0x12 / 0x13	mAh	R	R/W
<i>AverageCurrent()</i>	0x14 / 0x15	mA	R	R/W
<i>TimeToEmpty()</i>	0x16 / 0x17	Minutes	R	R/W
<i>RemainingCapacityUnfiltered()</i>	0x18 / 0x19	mAh	R	R/W
<i>StandbyCurrent()</i>	0x1a / 0x1b	mA	R	R/W
<i>RemainingCapacityFiltered()</i>	0x1c / 0x1d	mAh	R	R/W
<i>ProgChargingCurrent()</i>	0x1e / 0x1f	mA	R <sup>(1)</sup>	R <sup>(1)</sup>
<i>ProgChargingVoltage()</i>	0x20 / 0x21	mV	R <sup>(1)</sup>	R <sup>(1)</sup>
<i>FullChargeCapacityUnfiltered()</i>	0x22 / 0x23	mAh	R	R/W
<i>AveragePower()</i>	0x24 / 0x25	mW	R	R/W
<i>FullChargeCapacityFiltered()</i>	0x26 / 0x27	mAh	R	R/W
<i>StateOfHealth()</i>	0x28 / 0x29	% / num	R	R/W
<i>CycleCount()</i>	0x2a / 0x2b	Counters	R	R/W
<i>StateOfCharge()</i>	0x2c / 0x2d	%	R	R/W
<i>TrueSOC()</i>	0x2e / 0x2f	%	R	R/W
<i>InstantaneousCurrentReading()</i>	0x30 / 0x31	mA	R	R/W
<i>InternalTemperature()</i>	0x32 / 0x33	0.1 K	R	R/W
<i>ChargingLevel()</i>	0x34 / 0x35	HEX	R	R
<i>LevelTaperCurrent()</i>	0x6e / 0x6f	mA	R	R
<i>CalcChargingCurrent()</i>	0x70 / 0x71	mA	R	R
<i>CalcChargingVoltage()</i>	0x72 / 0x73	V	R	R

(1) Only writeable when **Charger Options [BYPASS]** is set.

**Control( ): 0x00/0x01**

Issuing a *Control()* command requires a subsequent 2-byte subcommand. These additional bytes specify the particular control function desired. The *Control()* command allows the system to control specific features of the bq27530-G1 during normal operation and additional features when the device is in different access modes, as described in [Table 3](#). Additional details are found in the [bq27530-G1 Technical Reference Manual](#).

**Table 3. Control( ) Subcommands**

CNTL FUNCTION	CNTL DATA	SEALED ACCESS	DESCRIPTION
CONTROL_STATUS	0x0000	Yes	Reports the status of hibernate, IT, etc.
DEVICE_TYPE	0x0001	Yes	Reports the device type (eg: bq27530)
FW_VERSION	0x0002	Yes	Reports the firmware version on the device type
HW_VERSION	0x0003	Yes	Reports the hardware version of the device type
PREV_MACWRITE	0x0007	Yes	Returns previous MAC subcommand code
CHEM_ID	0x0008	Yes	Reports the chemical identifier of the Impedance Track™ configuration
BOARD_OFFSET	0x0009	No	Forces the device to measure and store the board offset
CC_OFFSET	0x000a	No	Forces the device to measure the internal CC offset
CC_OFFSET_SAVE	0x000b	No	Forces the device to store the internal CC offset
OCV_CMD	0x000c	Yes	Request the gauge to take a OCV measurement
BAT_INSERT	0x000d	Yes	Forces the BAT_DET bit set when the [BIE] bit is 0
BAT_REMOVE	0x000e	Yes	Forces the BAT_DET bit clear when the [BIE] bit is 0
SET_HIBERNATE	0x0011	Yes	Forces CONTROL_STATUS [HIBERNATE] to 1
CLEAR_HIBERNATE	0x0012	Yes	Forces CONTROL_STATUS [HIBERNATE] to 0
SET_SLEEP+	0x0013	Yes	Forces CONTROL_STATUS [SNOOZE] to 1
CLEAR_SLEEP+	0x0014	Yes	Forces CONTROL_STATUS [SNOOZE] to 0
DIV_CUR_ENABLE	0x0017	Yes	Makes the programmed charge current to be half of what is calculated by the gauge charging algorithm.
CHG_ENABLE	0x001A	Yes	Enable charger. Charge will continue as dictated by gauge charging algorithm.
CHG_DISABLE	0x001B	Yes	Disable charger (Set $\overline{CE}$ bit of bq2416x)
GG_CHGRCTL_ENABLE	0x001C	Yes	Enables the gas gauge to control the charger while continuously resetting the charger watchdog
GG_CHGRCTL_DISABLE	0x001D	Yes	The gas gauge stops resetting the charger watchdog
DIV_CUR_DISABLE	0x001E	Yes	Makes the programmed charge current to be same as what is calculated by the gauge charging algorithm.
DF_VERSION	0x001F	Yes	Returns the Data Flash Version
SEALED	0x0020	No	Places device in SEALED access mode
IT_ENABLE	0x0021	No	Enables the Impedance Track™ algorithm
RESET	0x0041	No	Forces a full reset of the bq27530-G1

## FUNCTIONAL DESCRIPTION

The bq27530-G1 measures the cell voltage, temperature, and current to determine battery SOC. The bq27530-G1 monitors charge and discharge activity by sensing the voltage across a small-value resistor (5 mΩ to 20 mΩ typ.) between the SRP and SRN pins and in series with the cell. By integrating charge passing through the battery, the battery's SOC is adjusted during battery charge or discharge.

The total battery capacity is found by comparing states of charge before and after applying the load with the amount of charge passed. When an application load is applied, the impedance of the cell is measured by comparing the OCV obtained from a predefined function for present SOC with the measured voltage under load. Measurements of OCV and charge integration determine chemical state of charge and chemical capacity (Qmax). The initial Qmax values are taken from a cell manufacturers' data sheet multiplied by the number of parallel cells. It is also used for the value in **Design Capacity**. The bq27530-G1 acquires and updates the battery-impedance profile during normal battery usage. It uses this profile, along with SOC and the Qmax value, to determine *FullChargeCapacity*( ) and *StateOfCharge*( ), specifically for the present load and temperature. *FullChargeCapacity*( ) is reported as capacity available from a fully charged battery under the present load and temperature until *Voltage*( ) reaches the **Terminate Voltage**. *NominalAvailableCapacity*( ) and *FullAvailableCapacity*( ) are the uncompensated (no or light load) versions of *RemainingCapacity*( ) and *FullChargeCapacity*( ) respectively.

The bq27530-G1 has two flags accessed by the *Flags*( ) function that warns when the battery's SOC has fallen to critical levels. When *RemainingCapacity*( ) falls below the first capacity threshold, specified in **SOC1 Set Threshold**, the [SOC1] (*State of Charge Initial*) flag is set. The flag is cleared once *RemainingCapacity*( ) rises above **SOC1 Clear Threshold**.

When *Voltage*( ) falls below the system shut down threshold voltage, **SysDown Set Volt Threshold**, the [SYSDOWN] flag is set, serving as a final warning to shut down the system. The SOC\_INT also signals. When *Voltage*( ) rises above **SysDown Clear Voltage** and the [SYSDOWN] flag has already been set, the [SYSDOWN] flag is cleared. The SOC\_INT also signals such change. All units are in mV.

When the voltage is discharged to **Terminate Voltage**, the SOC will be set as 0.

## COMMUNICATIONS

### I<sup>2</sup>C INTERFACE

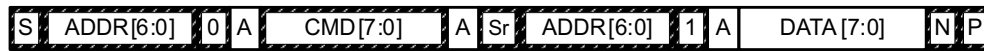
The bq27530-G1 supports the standard I<sup>2</sup>C read, incremental read, quick read, one byte write, and incremental write functions. The 7 bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The first 8-bits of the I<sup>2</sup>C protocol will; therefore, be 0xAA or 0xAB for write or read, respectively.

Host generated     Gauge generated

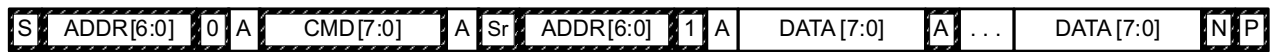


(a) 1-byte write

(b) quick read



(c) 1- byte read



(d) incremental read



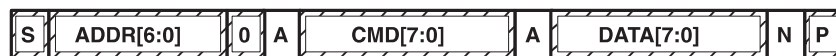
(e) incremental write

(S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop).

The “quick read” returns data at the address indicated by the address pointer. The address pointer, a register internal to the I<sup>2</sup>C communication engine, will increment whenever data is acknowledged by the bq27530-G1 or the I<sup>2</sup>C master. “Quick writes” function in the same manner and are a convenient means of sending multiple bytes to consecutive command locations (such as two-byte commands that require two bytes of data)

The following command sequences are not supported:

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x6B (NACK command):

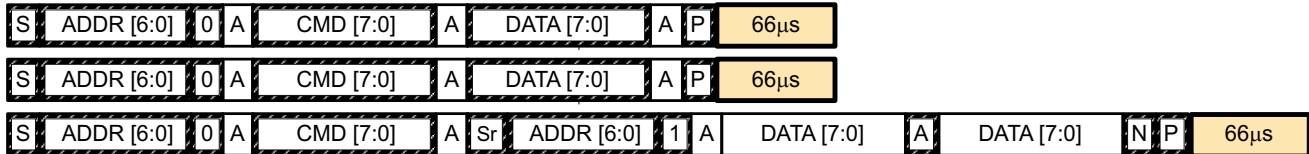


### I<sup>2</sup>C Time Out

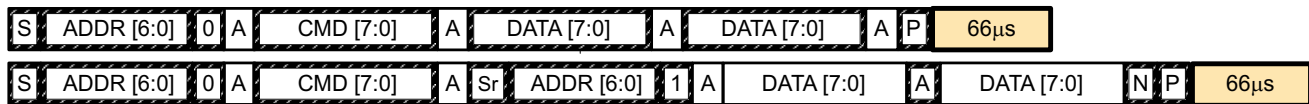
The I<sup>2</sup>C engine will release both SDA and SCL if the I<sup>2</sup>C bus is held low for 2 seconds. If the bq27530-G1 was holding the lines, releasing them will free them for the master to drive the lines. If an external condition is holding either of the lines low, the I<sup>2</sup>C engine will enter the low power sleep mode.

## I<sup>2</sup>C Command Waiting Time

To ensure proper operation at 400 kHz, a  $t_{(BUF)} \geq 66 \mu s$  bus free waiting time should be inserted between all packets addressed to the bq27530-G1. In addition, if the SCL clock frequency ( $f_{SCL}$ ) is  $> 100$  kHz, use individual 1-byte write commands for proper data flow control. The following diagram shows the standard waiting time required between issuing the control subcommand the reading the status result. A DF\_CHECKSUM subcommand requires 100mS minimum prior to reading the result. An OCV\_CMD subcommand requires 1.2 seconds prior to reading the result. For read-write standard command, a minimum of 2 seconds is required to get the result updated. For read-only standard commands, there is no waiting time required, but the host should not issue all standard commands more than two times per second. Otherwise, the gauge could result in a reset issue due to the expiration of the watchdog timer.



Waiting time inserted between two 1-byte write packets for a subcommand and reading results  
(required for  $100 \text{ kHz} < f_{SCL} \leq 400 \text{ kHz}$ )



Waiting time inserted between incremental 2-byte write packet for a subcommand and reading results  
(acceptable for  $f_{SCL} \leq 100 \text{ kHz}$ )



Waiting time inserted after incremental read

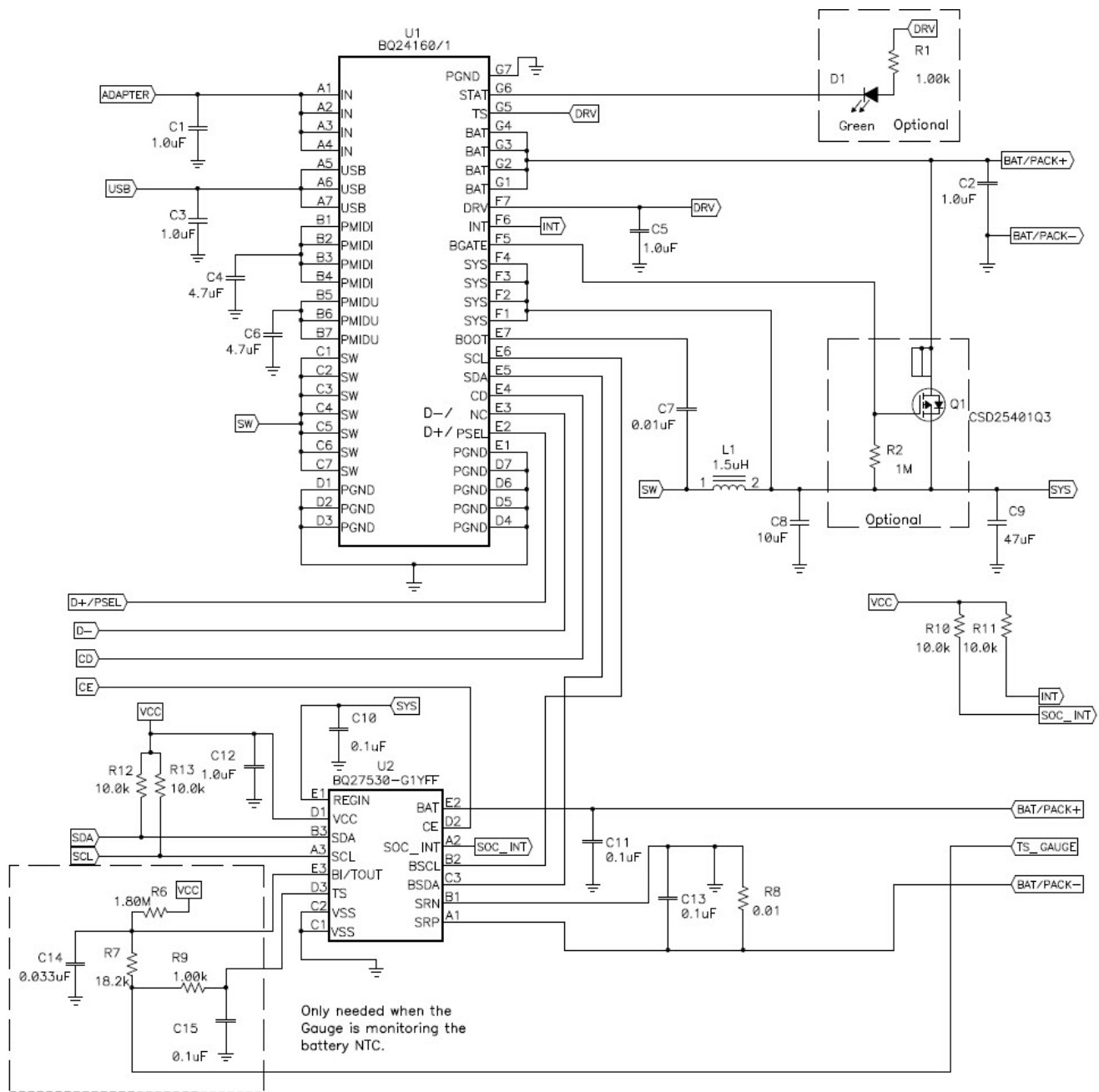
## I<sup>2</sup>C Clock Stretching

A clock stretch can occur during all modes of fuel gauge operation. In 睡眠 and HIBERNATE modes, a short clock stretch will occur on all I<sup>2</sup>C traffic as the device must wake-up to process the packet. In the other modes ( 电池插入检查, NORMAL, 睡眠+ ) clock stretching will only occur for packets addressed for the fuel gauge. The majority of clock stretch periods are small as the I<sup>2</sup>C interface performs normal data flow control. However, less frequent yet more significant clock stretch periods may occur as blocks of 数据闪存 are updated. The following table summarizes the approximate clock stretch duration for various fuel gauge operating conditions.

Gauging Mode	Operating Condition / Comment	Approximate Duration
睡眠 HIBERNATE	Clock stretch occurs at the beginning of all traffic as the device wakes up.	$\leq 4 \text{ ms}$
电池插入检查 NORMAL 睡眠+	Clock stretch occurs within the packet for flow control. (after a start bit, ACK or first data bit)	$\leq 4 \text{ ms}$
	Normal Ra table 数据闪存 updates.	24 ms
	数据闪存 block writes.	72 ms
	Restored 数据闪存 block write after loss of power.	116 ms
	End of discharge Ra table 数据闪存 update.	144 ms

REFERENCE SCHEMATICS

SCHEMATIC



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ27530YZFR-G1	ACTIVE	DSBGA	YZF	15	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27530	<a href="#">Samples</a>
BQ27530YZFT-G1	ACTIVE	DSBGA	YZF	15	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ27530	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

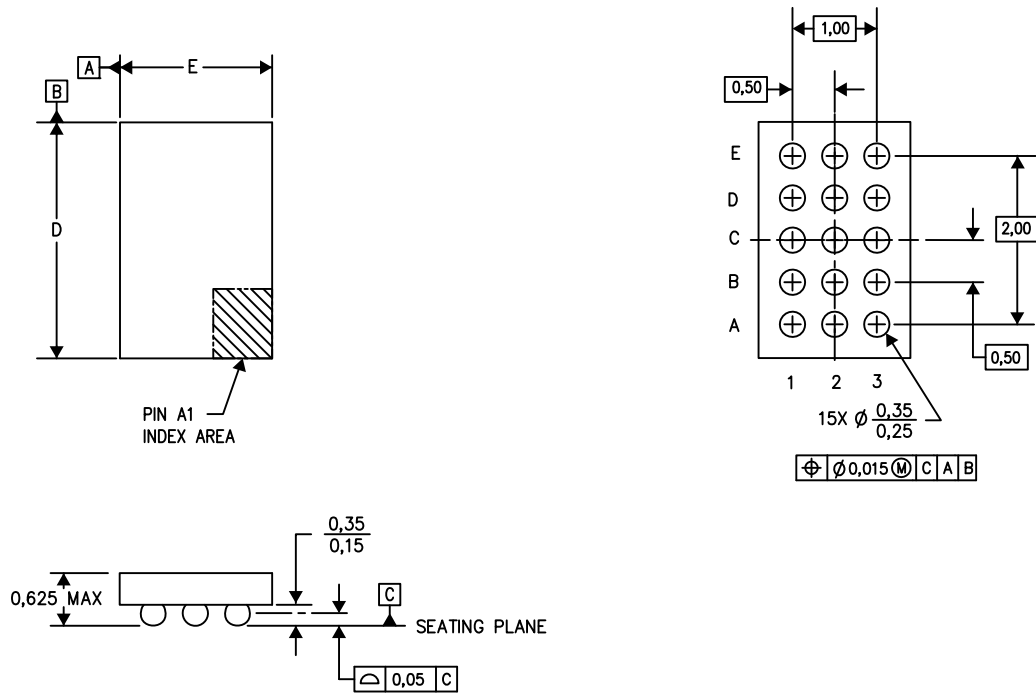
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YZF (R-XBGA-N15)

DIE-SIZE BALL GRID ARRAY



4205058-5/P 07/13

- NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.  
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接口	<a href="http://www.ti.com.cn/interface">www.ti.com.cn/interface</a>	安防应用	<a href="http://www.ti.com.cn/security">www.ti.com.cn/security</a>
逻辑	<a href="http://www.ti.com.cn/logic">www.ti.com.cn/logic</a>	汽车电子	<a href="http://www.ti.com.cn/automotive">www.ti.com.cn/automotive</a>
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RFID 系统	<a href="http://www.ti.com.cn/rfidsys">www.ti.com.cn/rfidsys</a>		
OMAP应用处理器	<a href="http://www.ti.com.cn/omap">www.ti.com.cn/omap</a>		
无线连通性	<a href="http://www.ti.com.cn/wirelessconnectivity">www.ti.com.cn/wirelessconnectivity</a>	德州仪器在线技术支持社区	<a href="http://www.deyisupport.com">www.deyisupport.com</a>

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