



LED Driver with Average-Mode Constant Current Control

General Description

The An9961 is an average current mode control LED driver IC operating in a constant off-time mode. Unlike An9910B, this control IC does not produce a peak-to-average error, and therefore greatly improves accuracy, line and load regulation of the LED current without any need for loop compensation or high-side current sensing. The output LED current accuracy is $\pm 3\%$.

The IC is equipped with a current limit comparator for hiccup mode output short circuit protection.

The An9961 can be powered from an 8.0 - 450V supply. A PWM dimming input is provided that accepts an external control TTL compatible signal. The output current can be programmed by an internal 272mV reference, or controlled externally through a 0 - 1.5V dimming input.

An9961 is pin-to-pin compatible with An9910B and it can be used as a drop-in replacement for many applications to improve the LED current accuracy and regulation.

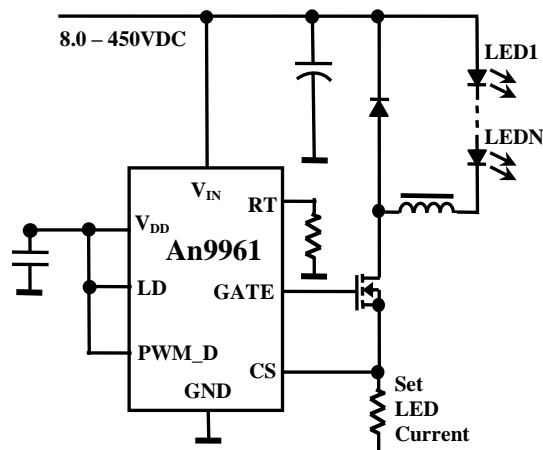
Features

- Fast average current control
- Programmable constant off-time switching
- Linear dimming input
- PWM dimming input
- Output short circuit protection with skip mode
- Ambient operating temperature -40°C to $+125^{\circ}\text{C}$
- Pin-compatible with the An9910B

Applications

- DC/DC or AC/DC LED driver applications
- LED backlight driver for LCD displays
- General purpose constant current source
- LED signage and displays
- Architectural and decorative LED lighting
- LED street lighting

Typical Application Circuit





Absolute Maximum Ratings

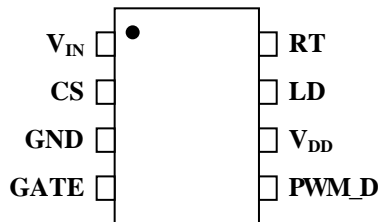
| Parameter | Value |
|---|----------------------------------|
| V _{IN} to GND | -0.5V to +470V |
| V _{DD} to GND | 12V |
| CS, LD, PWM_D, GATE, RT to GND | -0.3V to (V _{DD} +0.3V) |
| Junction temperature range | -40°C to+150°C |
| Storage temperature range | -65°C to+150°C |
| Continuous power dissipation (T _A = +25°C) | |
| 8-Lead SOIC | 650mW |
| 16-LeadSOIC | 1000mW |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

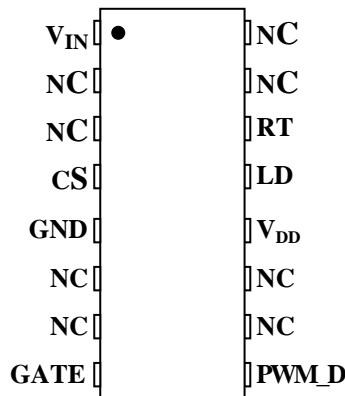
Thermal Resistance

| Package | θ _{JA} |
|-------------|-----------------|
| 8-Lead SOIC | 128°C/W |
| 16-LeadSOIC | 82°C/W |

Pin Configuration



8-Lead SOIC (LG)



16-Lead SOIC (NG)

**Electrical Characteristics**(Specifications are at $T_A = 25^\circ\text{C}$. $V_{IN} = 12\text{V}$, $V_{LD} = V_{DD}$, $PWMD = V_{DD}$ unless otherwise noted)

| Sym | Parameter | Min | Typ | Max | Units | Conditions |
|-----|-----------|-----|-----|-----|-------|------------|
|-----|-----------|-----|-----|-----|-------|------------|

Input

| | | | | | | | |
|------------|--|---|-----|-----|-----|----|-----------------------|
| V_{INDC} | Input DC supply voltage range ¹ | * | 8.0 | - | 450 | V | DC input voltage |
| I_{INSD} | Shut-down mode supply current | * | - | 0.5 | 1.0 | mA | PWMD connected to GND |

Internal Regulator

| | | | | | | | |
|----------------------|--|---|------|------|------|----|--|
| V_{DD} | Internally regulated voltage | - | 7.25 | 7.50 | 7.75 | V | $V_{IN}=8.0$, $I_{DD(EXT)}=0$, 500pF at GATE, $R_T=226\text{k}\Omega$ |
| $\Delta V_{DD,line}$ | Line regulation of V_{DD} | - | 0 | - | 1.0 | V | $V_{IN}=8.0-450\text{V}$, $I_{DD(EXT)}=0$, 500pF at GATE, $F_{RT}=226\text{k}\Omega$, |
| $\Delta V_{DD,load}$ | Load regulation of V_{DD} | - | 0 | - | 100 | mV | $I_{DD(EXT)}=0-1.0\text{mA}$, 500pF at GATE, $F_{RT}=226\text{k}\Omega$, |
| UVLO | V_{DD} under voltage lockout threshold | * | 6.45 | 6.70 | 6.95 | V | V_{IN} rising |
| $\Delta UVLO$ | V_{DD} undervoltage lockout hysteresis | - | - | 500 | - | mV | V_{IN} falling |
| $I_{IN,MAX}$ | Maximum input current (limited by UVLO) | # | 3.5 | - | - | mA | $V_{IN}=8.0\text{V}$, $T_A=25^\circ\text{C}$ |
| | | # | 1.5 | - | - | | $V_{IN}=8.0\text{V}$, $T_A=125^\circ\text{C}$ |

PWM Dimming

| | | | | | | | |
|--------------|---------------------------------------|---|-----|-----|-----|------------|------------------------------|
| $V_{EN(lo)}$ | PWMD input low voltage | * | - | - | 0.8 | V | $V_{IN} = 8.0 - 450\text{V}$ |
| $V_{EN(hi)}$ | PWMD input high voltage | * | 2.0 | - | - | V | $V_{IN} = 8.0 - 450\text{V}$ |
| R_{EN} | Internal pull-down resistance at PWMD | - | 50 | 100 | 150 | k Ω | $R_{PWMD} = 5.0\text{V}$ |

Average Current Sense Logic

| | | | | | | | |
|----------------------|---------------------------------|---|-------|-----|-------|----|--|
| V_{CS} | Current sense reference voltage | - | 238 | 250 | 262 | mV | --- |
| $A_{V(LD)}$ | LD-to-CS voltage ratio | - | 0.176 | - | 0.187 | - | --- |
| $V_{LD(OFF)}$ | LD input voltage, shutdown | - | - | 150 | - | mV | V_{LD} falling |
| $\Delta V_{LD(OFF)}$ | LD input voltage, enable | - | - | 200 | - | mV | V_{LD} rising |
| T_{BLANK} | Current sense blanking interval | * | 150 | - | 280 | ns | --- |
| $T_{ON(min)}$ | Minimum on-time | - | - | - | 1000 | ns | $CS = V_{CS} + 30\text{mV}$ |
| D_{MAX} | Maximum steady-state duty cycle | - | 75 | - | - | % | Reduction in output LED current may occur beyond this duty cycle |

Short Circuit Protection

| | | | | | | | |
|---------------|---------------------------------|---|-----|---|-----|---------------|-----------------------------|
| V_{CS} | Hiccup threshold voltage | - | 410 | - | 470 | mV | --- |
| T_{DELAY} | Current limit delay CS-to-GATE | - | - | - | 150 | ns | $CS = V_{CS} + 30\text{mV}$ |
| T_{HICCUP} | Short circuit hiccup time | - | 330 | - | 460 | μs | --- |
| $T_{ON(min)}$ | Minimum on-time (short circuit) | - | - | - | 430 | ns | $CS = V_{DD}$ |

T_{OFF} Timer

| | | | | | | | |
|-----------|----------|---|-----|----|----|---------------|--------------------------|
| T_{OFF} | Off time | - | 32 | 40 | 48 | μs | $R_T=1.00\text{M}\Omega$ |
| | | - | 8.0 | 10 | 12 | | $R_T=226\text{k}\Omega$ |

GATE Driver

| | | | | | | | |
|--------------|-----------------------|---|-------|----|----|----|--|
| I_{SOURCE} | GATE sourcing current | - | 0.165 | - | - | A | $V_{GATE}=0\text{V}$, $V_{DD}=7.5\text{V}$ |
| I_{SINK} | GATE sinking current | - | 0.165 | - | - | A | $V_{GATE} = V_{DD}$, $V_{DD}=7.5\text{V}$ |
| t_{RISE} | GATE output rise time | - | - | 30 | 50 | ns | $C_{GATE} = 500\text{pF}$, $V_{DD}=7.5\text{V}$ |
| t_{FALL} | GATE output fall time | - | - | 30 | 50 | ns | $C_{GATE} = 500\text{pF}$, $V_{DD}=7.5\text{V}$ |

Notes:

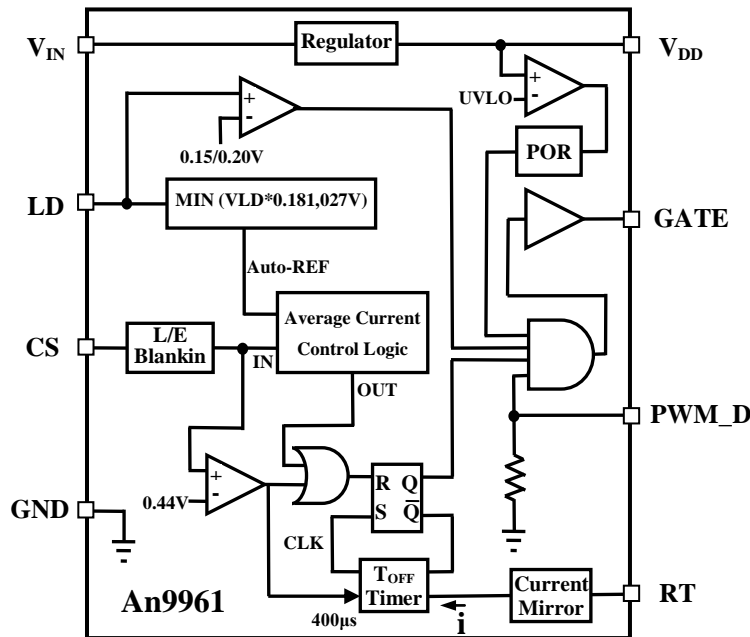
1. Also limited by package power dissipation limit, whichever is lower.

* Denotes the specifications which apply over the full operating ambient temperature range of $-40^\circ\text{C} < T_A < +125^\circ\text{C}$

Guaranteed by design



Functional Block Diagram



Application Information

General Description

Peak-current control (as in An9910B) of a buck converter is the most economical and simple way to regulate its output current. However, it suffers accuracy and regulation problems that arise from the so-called peak-to-average current error, contributed by the current ripple in the output inductor and the propagation delay in the current sense comparator. The full inductor current signal is unavailable for direct sensing at the ground potential in a buck converter when the control switch is referenced to the same ground potential because the control switch is only conducting for small periods. While it is very simple to detect the peak current in the switch, controlling the average inductor current is usually implemented by level translating the sense signal from +V_{IN}. Though this is practical for relatively low input voltage V_{IN}, this type of average-current control may become excessively complex and expensive in the offline AC or other high-voltage DC applications.

The An9961 employs control scheme, achieving fast and very accurate control of average current in the buck inductor through sensing the switch current only. No compensation of the current control loop is required. The LED current response to PWM_D input is similar to that of the An9910B. The inductor current ripple amplitude does not affect this control scheme significantly, and therefore, the LED current is independent of the variation in inductance, switching frequency or output voltage. Constant off-time control of the buck converter is used for stability and to improve the LED current regulation over a wide range of input voltages. (Note that, unlike An9910B, the An9961 does not support the constant-frequency mode of operation.)

OFF Timer

The timing resistor connected to RT determines the off-time of the gate driver, and it must be wired to GND. (Wiring this resistor to GATE as with An9910B is no longer supported.) The equation governing the off-time of the GATE output is given by:

$$T_{OFF} (\mu s) = \frac{R_T (k\Omega)}{25} + 0.3 \quad (1)$$

within the range of $30k\Omega \leq R_T \leq 1.0M\Omega$.

Average Current Control Feedback and Output Short Circuit Protection

The current through the switching MOSFET source is averaged and used to give constant-current feedback. This current is detected using a sense resistor at the CS pin. The feedback operates in a fast open-loop mode. No compensation is required. Output current is programmed simply as:

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$$I_{LED} = \frac{0.272V}{R_{CS}} \quad (2)$$

when the voltage at the LD input $V_{LD} \geq 1.5V$. Otherwise:

$$I_{LED} = \frac{V_{LD} \cdot 0.181}{R_{CS}} \quad (3)$$

The above equations are only valid for continuous conduction of the output inductor. It is a good practice to design the inductor such that the switching ripple current in it is 30~40% of its average peak-to-peak, full load, DC current. Hence, the recommended inductance can be calculated as:

$$L_O = \frac{V_{O(MAX)} \cdot T_{OFF}}{0.4 \cdot I_O} \quad (4)$$

The duty-cycle range of the current control feedback is limited to $D \leq 0.75$. A reduction in the LED current may occur when the LED string voltage V_O is greater than 75% of the input voltage V_{IN} of the An9961 LED driver.

Reducing the output LED voltage V_O below $V_{O(MIN)} = V_{IN} \cdot D_{MIN}$, where $D_{MIN} = 1.0\mu s / (T_{OFF} + 1.0\mu s)$, may also result in the loss of regulation of the LED current. This condition, however, causes an increase in the LED current and can potentially trip the short-circuit protection comparator.

The typical output characteristic of the An9961 LED driver is shown in Fig.1. The corresponding An9910B characteristic is given for the comparison.

Output Characteristics

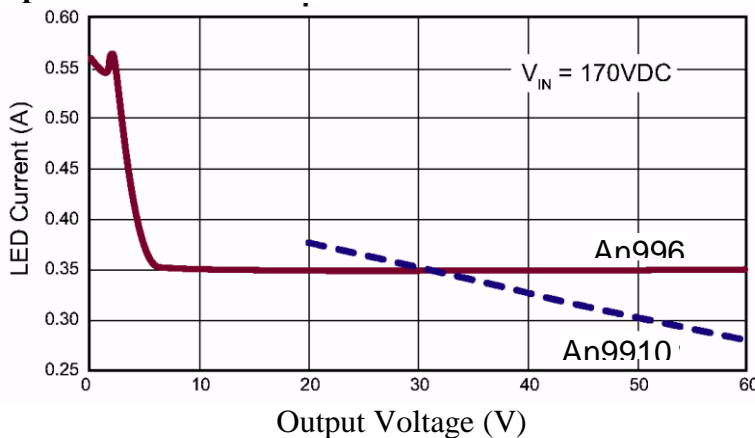


Fig.1. Typical output characteristic of an An9961 LED driver.

The short circuit protection comparator trips when the voltage at CS exceeds $0.44V$. When this occurs, the GATE off-time $T_{HICCUP} = 400\mu s$ is generated to prevent stair-casing of the inductor current and potentially its saturation due to insufficient output voltage. The typical short-circuit current is shown in the waveform of Fig. 2.

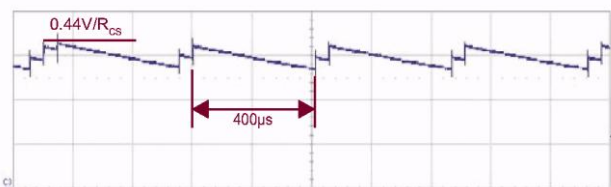


Fig.2. Short-circuit inductor current.

A leading-edge blanking delay is provided at CS to prevent false triggering of the current feedback and the short circuit protection. Both output open and output short circuit conditions require recycling the VDD supply voltage to restore normal operation.



Linear Dimming

When the voltage at LD falls below 1.5V, the internal 272mV reference to the constant-current feedback becomes overridden by $V_{LD} \cdot 0.181$. As long as the current in the inductor remains continuous, the LED current is given by the equation (3) above. However, when V_{LD} falls below 150mV, the GATE output becomes disabled. The GATE signal recovers, when V_{LD} exceeds 200mV. This is required in some applications to be able to shut the LED lamp off with the same signal input that controls the brightness. The typical linear dimming response is shown in Fig.3.

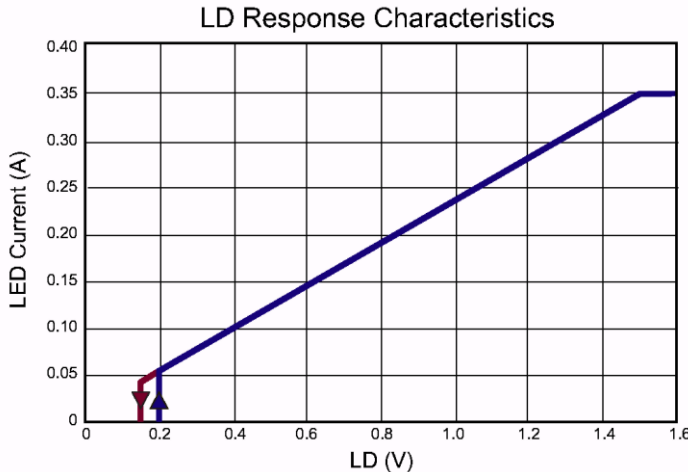


Fig.3. Typical linear dimming response of an An9961 LED driver

The linear dimming input could also be used for "mixed-mode" dimming to expand the dimming ratio. In such case a pulse-width modulated signal of a measured amplitude below 1.5V should be applied at LD.

Input Voltage Regulator

The An9961 can be powered directly from an 8.0 ~ 450VDC supply through its VIN input. When this voltage is applied at the VIN pin, the An9961 maintains a constant 7.5V level at VDD. This voltage can be used to power the IC and external circuitry connected to VDD within the rated maximum current or within the thermal ratings of the package, whichever limit is lower. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the GATE output. The An9961 can also be powered through the VDD pin directly with a voltage greater than the internally regulated 7.5V, but less than 12V.

Despite the instantaneous voltage rating of 450V, continuous voltage at VIN is limited by the power dissipation in the package. For example, when An9961 draws $I_{IN} = 2.0mA$ from the VIN input, and the 8-pin SOIC package is used, the maximum continuous voltage at VIN is limited to:

$$V_{IN(MAX)} = \frac{(T_{J(MAX)} - T_A)}{R_{\theta,JA} \cdot I_{IN}} = 390V \tag{5}$$

where the ambient temperature $T_A = 25OC$, the maximum working junction temperature $T_{J(MAX)} = 125OC$, the junction-to-ambient thermal resistance $R_{\theta,JA} = 128OC/W$.

In such cases, when it is needed to operate the An9961 from a higher voltage, a resistor or a Zener diode can be added in series with the VIN input to divert some of the power loss from the An9961. In the above example, using a 100V Zener diode will allow the circuit to work up to 490V. The input current drawn from the VIN pin is represented by the following equation:

$$I_{IN} \approx 1.0mA + Q_G \cdot f_S \tag{6}$$

In the above equation, f_S is the switching frequency, and Q_G is the GATE charge of the external FET obtained from the manufacturer's datasheet.



GATE Output

The GATE output of the An9961 is used to drive an external MOSFET. It is recommended that the gate charge Q_G of the external MOSFET be less than 25nC for switching frequencies $\leq 100\text{kHz}$ and less than 15nC for switching frequencies $> 100\text{kHz}$.

PWM Dimming

Due to the fast open-loop response of the average-current control loop of the An9961, its PWM dimming performance nearly matches that of the An9910B. The inductor current waveform comparison is shown in Fig. 4.

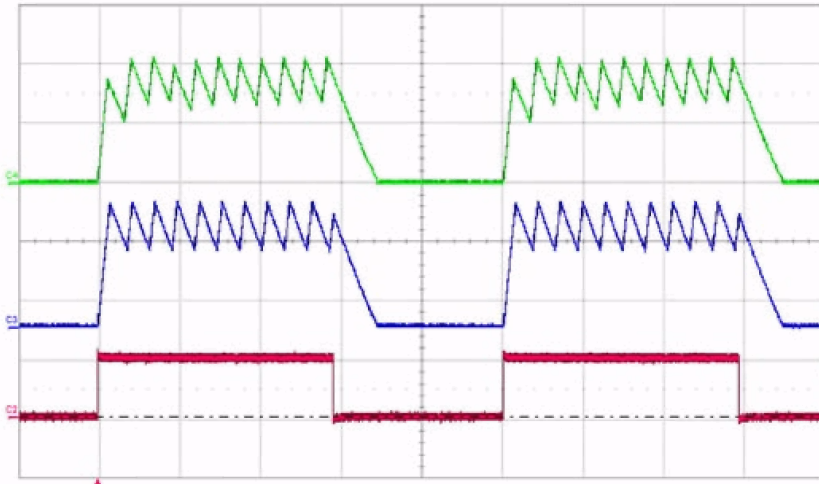


Fig.4. Typical PWM dimming response of an An9961 LED driver.

[CH2 (red): PWMD; CH4 (green): Inductor Current; CH3 (blue): Same as An9910B for comparison]

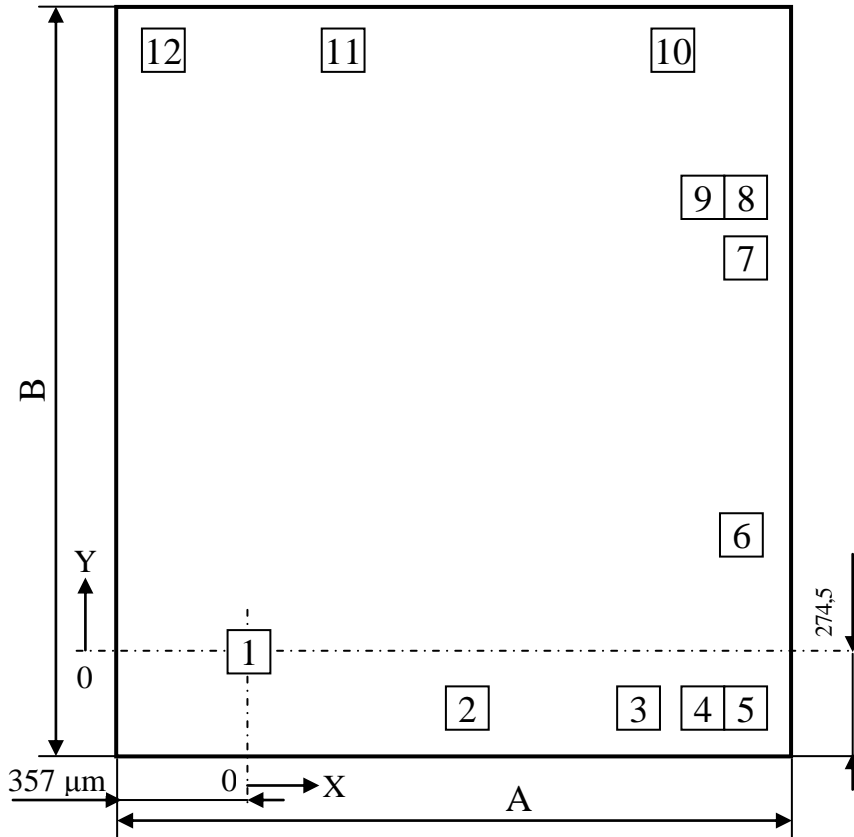
The rising and falling edges are limited by the current slew rate in the inductor. The first switching cycle is terminated upon reaching the 272mV ($V_{LD} \cdot 0.181$) level at CS. The circuit is further reaching its steady-state within 3~4 switching cycles regardless of the switching frequency.

Pin Description

| Pin # | | Pin Name | Description |
|-------------|----------------------------|----------|---|
| 8-Lead SOIC | 16-Lead SOIC | | |
| 1 | 1 | V_{IN} | This pin is the input of an 8.0 - 450V linear regulator. |
| 2 | 4 | CS | This pin is the current sense pin used to sense the FET current by means of an external sense resistor. |
| 3 | 5 | GND | Ground return for all internal circuitry. This pin must be electrically connected to the ground of the power train. |
| 4 | 8 | GATE | This pin is the output GATE driver for an external N-channel power MOSFET. |
| 5 | 9 | PWM_D | This is the PWM dimming input of the IC. When this pin is pulled to GND, the gate driver is turned off. When the pin is pulled high, the gate driver operates normally. |
| 6 | 12 | V_{DD} | This is the power supply pin for all internal circuits. It must be bypassed with a low ESR capacitor to GND (at least 0.1 μF). |
| 7 | 13 | LD | This pin is the linear dimming input, and it sets the current sense threshold as long as the voltage at this pin is less than 1.5V. If voltage at LD falls below 150mV, the GATE output is disabled. The GATE signal recovers at 200mV at LD. |
| 8 | 14 | RT | A resistor connected between this pin and GND programs the GATE off-time. |
| - | 2, 3, 6, 7, 10, 11, 15, 16 | NC | No connection |



PAD DIAGRAM



1. Chip size: A=1.80 mm, B=1.97 mm (without scribe line width).
2. Scribe line width: X=80 μm, Y=80 μm
3. Pad size: 100μm x 100 μm
4. Substrate to GND.
5. Wafer thickness: 460 μm

PAD LOCATION

| Pad number | Pad name | X (μm) | Y (μm) |
|------------|-----------------|--------|---------|
| 1 | V _{IN} | 0 | 0 |
| 2 | CS | 578 | - 144,5 |
| 3 | GND | 1029 | - 144,5 |
| 4 | GND | 1189 | - 144,5 |
| 5 | GND | 1313 | - 144,5 |
| 6 | GATE | 1300 | 303 |
| 7 | PWM_D | 1313 | 1033 |
| 8 | V _{DD} | 1313 | 1193 |
| 9 | V _{DD} | 1189 | 1193 |
| 10 | V _{DD} | 1122 | 1565,5 |
| 11 | LD | 250 | 1565,5 |
| 12 | RT | -227 | 1565,5 |



Photo An9961

