

MG36203

Data Sheet

Version: 1.02

Features:

- | Wide input range: 8V to 200V, without external protection devices
- | Enhanced peak current control, typical $\pm 3\%$ current accuracy
- | Fast switching frequency supported: lower ILED ripple and smaller inductor size
- | Single pin on/off and brightness control using DC voltage or PWM
- | Soft-start built in
- | Under Voltage Protection
- | On board, continuous thermal compensation of ILED current
- | Output short circuit protection with skip mode
- | CS loop open circuit protection with skip mode
- | Inherent LED open protection
- | Operating temperature, -40°C to $+85^{\circ}\text{C}$
- | SOP8 package

Content

Features:.....	2
1. General Description.....	4
2. Order Information.....	4
3. Applications.....	4
4. Pin Configurations (TBD).....	5
5. Pin Descriptions.....	5
6. Block Diagram.....	6
7. Typical Application Circuit.....	7
8. Absolute Maximum Rating.....	8
9. Electrical Characteristics.....	8
10. Package Information:.....	11
11. Revision History.....	12

1. General Description

The MG36203 is a 'peak current control' LED driver IC operating in constant off-time mode. With enhanced circuit structure, the current accuracy is improved to +/-3% for wide input VIN application. The MG36203 can be powered from a 8V - 200V supply without external protection devices (current limiting resistor, zener etc..). The 'wide VIN range application' is easily to be achieved.

The dimming control can be either 'digital' or 'analog' type through one input pin 'DIM'. If the DIM pin voltage is greater than 6.0V, the gate driver operates normally; the output current is programmed by an internal 500mV reference. When the pin voltage is in between 6.0V and 1.5V, the analog dimming function is activated. The output current is proportional to the 'DIM*ratio'. The 'ratio' is a pre-set factor and equal to '1/9.23'. When the pin voltage is less than 1.5V, the gate driver is turned off. If the DIM pin is switched ON and OFF at a rate larger than 100HZ, the pin is acting like a digital dimming function. MG36203 is pin-to-pin compatible with MG20U202 and it can be used as a drop-in replacement for existing applications to improve the LED current accuracy and regulation.

The IC provides various protect schemes: soft start, UVLO, short circuit, open CS-loop and on-board over temperature compensation.

The chip is available in 8 lead SOP package.

2. Order Information

Part No.	MG36203AS1
Package	SOP8

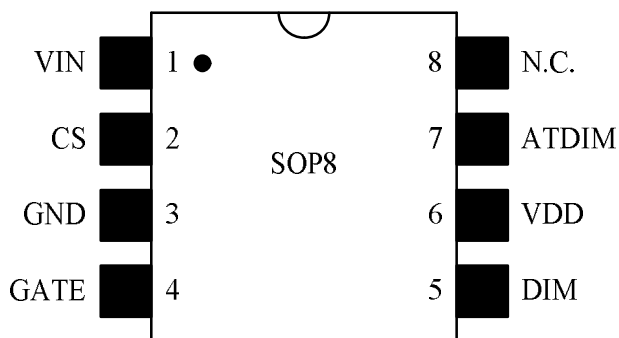
3. Applications

Automotive lighting

LCD backlighting

Replacement of general low voltage DC-DC lighting

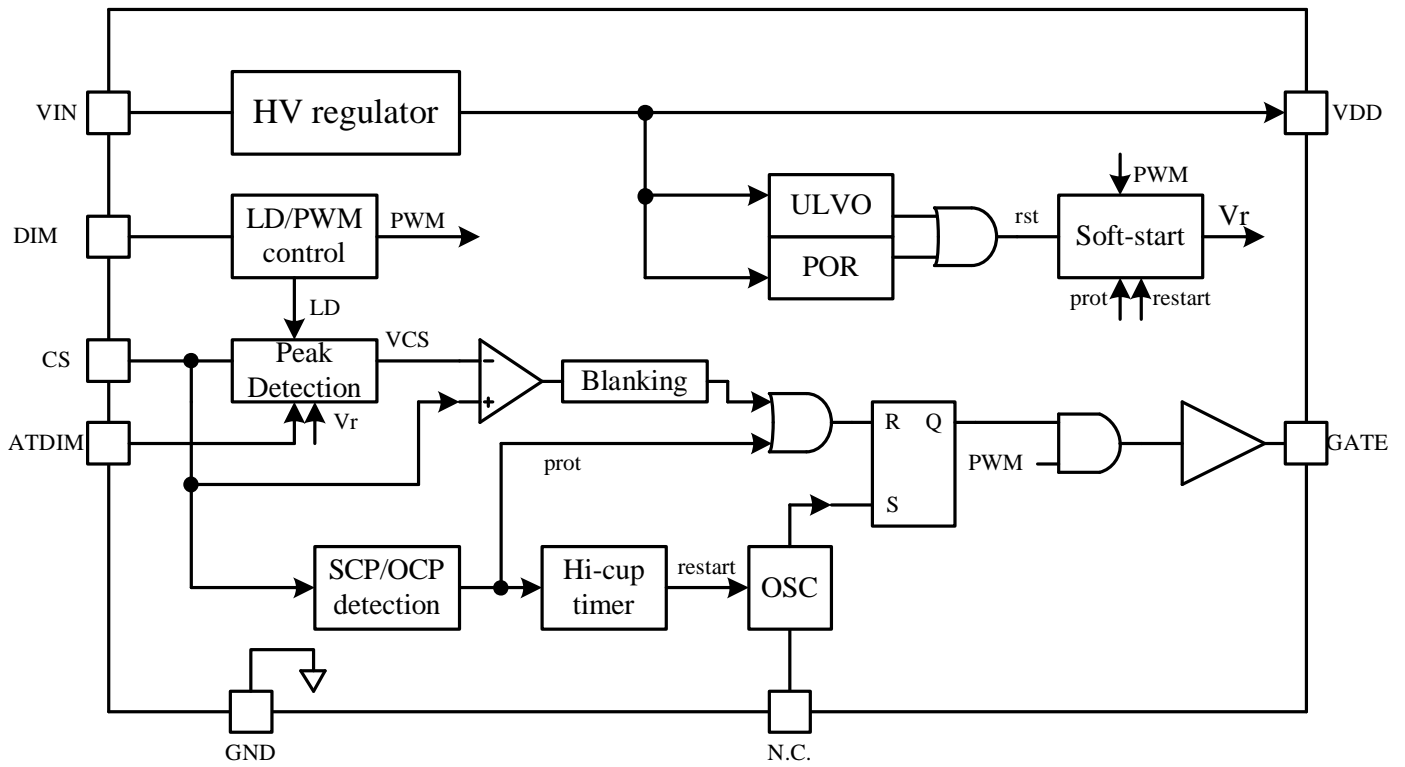
4. Pin Configurations (TBD)



5. Pin Descriptions

Pin No.	Name	I/O	Description
1	VIN	P_hv	Positive power input: 8V ~ 200V
2	CS	I	Current sense pin, used to sense the FET current by means of an external sense resistor.
3	GND	G	IC ground pad
4	GATE	O	PWM signal's output, for driving the external N-channel power MOSFET.
5	DIM	I	Dimming Control If > 6V, gate driver is normally on If < 1.5V, gate driver is forced off If it is between 1.5V and 6V, The CS compare level is $V_{DIM}/9.23$. If the pin is switching at a frequency >100Hz, it becomes a digital dimming control input.
6	VDD	P_lv	7.0V output
7	ATDIM	I	Temperature compensation of LED output current. If $ATDIM \geq 0.5V$, CS compare level is 0.5. If $ATDIM < 0.5$, CS compare level is V_{TCOMP}
8	N.C.		No Connection.

6. Block Diagram



7. Typical Application Circuit

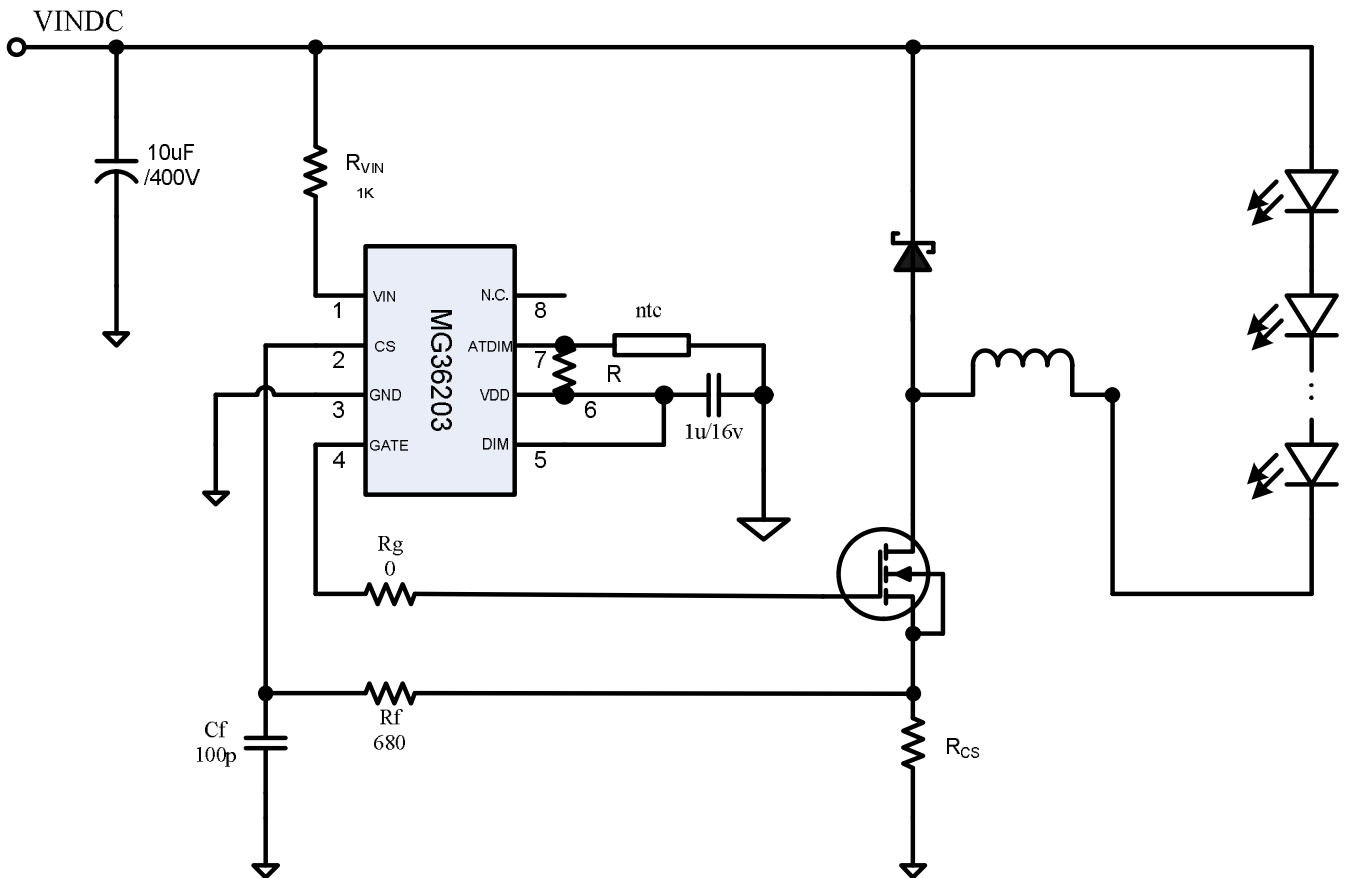


Fig. Typical application circuit with external temperature compensation

8. Absolute Maximum Rating

Parameter	Value
Vin Supply Voltage	-0.5v ~ 225v
Operating temperature	-40 ~ 125 degree
Storage temperature	-55 ~ 155 degree

PS: Operating temperature is strong related to the power consumption of IC.

9. Electrical Characteristics

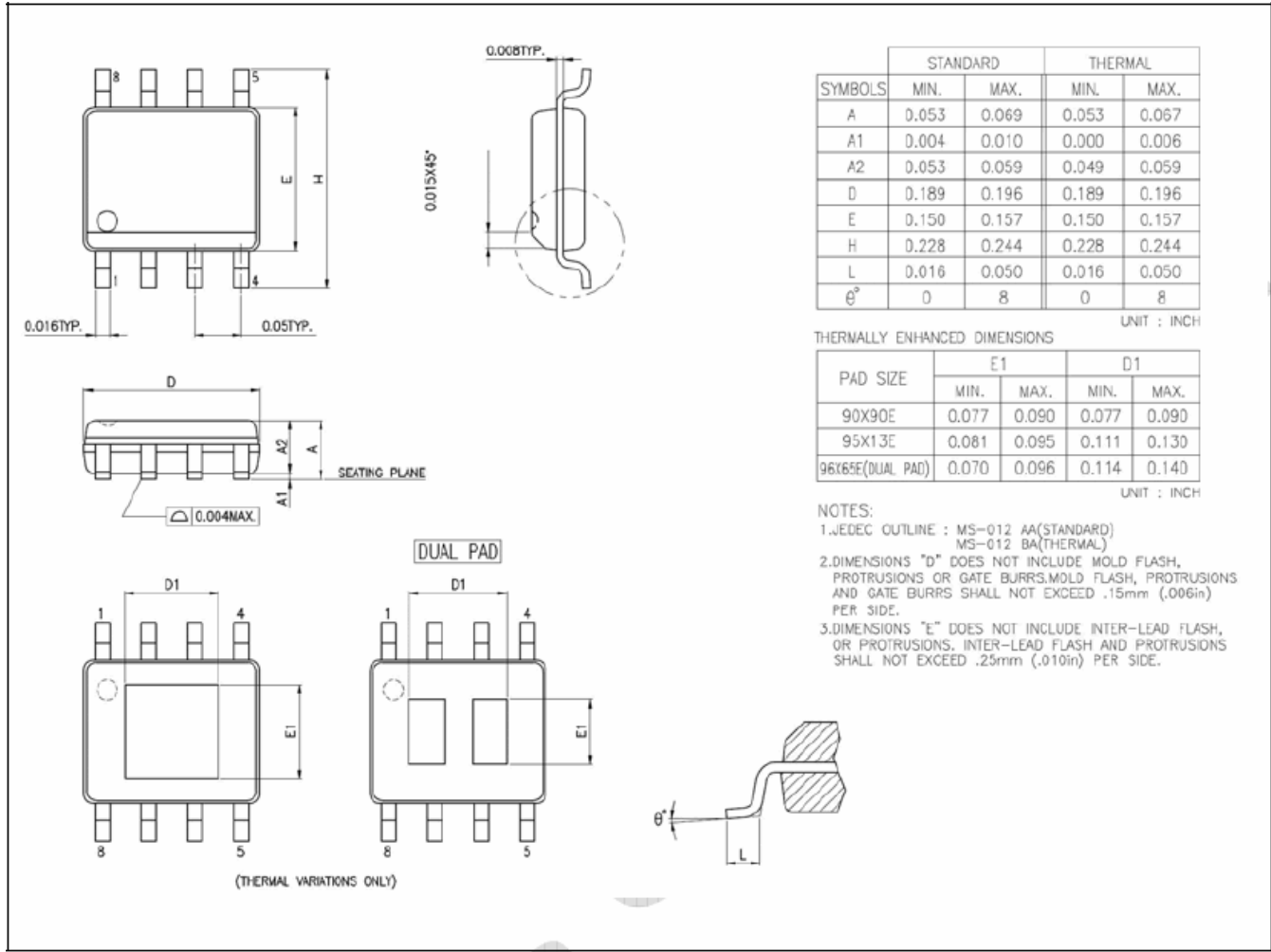
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input DC supply voltage range	VINDC	DC input voltage	8		200	V
Input supply current	IINSD	Pin CS=VDD7, PWM control is not switching		0.4	1.0	mA
Internal Regulator						
Internally regulated voltage	VDD	VIN = 9V, IDD(ext)= 0.5mA (typical case)	6.75	7.0	7.25	V
Line regulation of VDD	Δ VDD, line	VIN = 9V ~ 250V, IDD(ext) = 0.5mA,	0	0.1	0.3	V
Load regulation of VDD	Δ VDD, load	IDD(ext) = 0 ~ 1.7mA, VIN= 9V ~ 250V	0		100	mV
Maximum input current (limited by UVLO)	IIN,MAX	VIN = 9V, TA = 25°C	2.5	3.5		mA
VDD under-voltage lockout threshold	UVLO	VDD rising	5	5.25	5.5	V
VDD under-voltage lockout hysteresis	Δ UVLO	VDD falling		500		mV

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
DIM dimming						
DIM input voltage High	VDIM_H			6.0		V
DIM input voltage Low	VDIM_L			1.5		V
Linear dimming ratio	DIM_ratio			1/9.23		VDI M
ATDIM diming						
VATDIM input range	VATDIM	@TA = -40°C to +85°C	0		VCStH2	V
Current Sense Input						
Current sense pull-in threshold voltage	VCStH1	@TA = 25°C	490	500	510	mV
Current sense pull-in threshold voltage	VCStH2	@TA = -40°C to +85°C	480	500	520	mV
Current sense blanking interval	TBLANK		150	215	320	ns
Minimum on-time	TON(min)	CS = VCS +30mV			1000	ns
Maximum steady-state duty cycle	DMAX	Reduction in output LED current may occur beyond this duty cycle			75	%
Short Circuit Protection						
Hiccup threshold voltage	VHIC			2		V
Current limit delay CS-to-GATE	TDELAY	CS = VCStH +30mV		150		ns
Short circuit hiccup time	TSCP			8		ms
Short circuit detection time	TSHORT	CS > 2.0V		215		ns
Soft-start time	TSS	FSS=FOSC/512		1/FSS		ms
Open Circuit Protection						
Open circuit detection time	TOPEN			2		ms
Open circuit hiccup time	TOCP			8		ms
Gate Driver						
GATE output rise time	TRISE	CGATE = 500pF, VDD = 7.0V		150		ns
GATE output fall time	TFALL	CGATE = 500pF, VDD = 7.0V		150		ns
GATE sourcing current	Isource	VGATE = VDD – 0.4V, VDD = 7.0V		10		mA
GATE sinking current	Isink	VGATE = 0.4V, VDD = 7.0V		10		mA
GATE pull-low resistor	RPULL_LO			200		KΩ

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10. Package Information:

SOP8 Package Dimension



11. Revision History

Rev	Descriptions	Date
V1.00	Initial release	2013/12/23
V1.01	Rename model name	2014/02/11
V1.02	Modify input current spec	2015/5/26
V1.03	Modify input voltage spec	2015/6/11