Data Sheet | August 21, 2006 | FN6328.0

Four-Phase Buck PWM Controller with Integrated MOSFET Drivers and I²C Interface for Intel VR10, VR11, and AMD Applications

The ISL6322 four-phase PWM control IC provides a precision voltage regulation system for advanced microprocessors. The integration of power MOSFET drivers into the controller IC marks a departure from the separate PWM controller and driver configuration of previous multiphase product families. By reducing the number of external parts, this integration is optimized for a cost and space saving power management solution.

One outstanding feature of this controller IC is its multi-processor compatibility, allowing it to work with both Intel and AMD microprocessors. Included are programmable VID codes for Intel VR10, VR11, as well as AMD DAC tables. A unity gain, differential amplifier is provided for remote voltage sensing, compensating for any potential difference between remote and local grounds. The output voltage can also be positively or negatively offset through the use of a single external resistor.

The ISL6322 includes an I^2C interface, allowing the controller to communicate with other devices over an I^2C bus. Signals sent over this bus can command the ISL6322 to adjust voltage margining offset, converter switching frequency, and overvoltage protection levels, and can select the integrated driver adaptive dead time scheme.

The ISL6322 also includes advanced control loop features for optimal transient response to load apply and removal. One of these features is highly accurate, fully differential, continuous DCR current sensing for load line programming and channel current balance. Active Pulse Positioning (APP) modulation is another unique feature, allowing for quicker initial response to high di/dt load transients.

This controller also allows the user the flexibility to choose between PHASE detect or LGATE detect adaptive dead time schemes. This ability allows the ISL6322 to be used in a multitude of applications where either scheme is required.

Protection features of this controller IC include a set of sophisticated overvoltage, undervoltage, and overcurrent protection. Furthermore, the ISL6322 includes protection against an open circuit on the remote sensing inputs. Combined, these features provide advanced protection for the microprocessor and power system.

Features

- Integrated Multiphase Power Conversion
  - 2 or 3-Phase Operation with Internal Drivers
  - 4-Phase Operation with External PWM Driver Signal
- Precision Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Temperature
  - Adjustable Reference-Voltage Offset
- Optimal Transient Response
  - Active Pulse Positioning (APP) Modulation
  - Adaptive Phase Alignment (APA)
- Fully Differential, Continuous DCR Current Sensing
  - Accurate Load Line Programming
  - Precision Channel Current Balancing
- I^2C Interface
  - Voltage Margining Offset
  - Switching Frequency Adjustment
  - Overvoltage Protection Level Adjustment
  - Selects Adaptive Dead Time Scheme
- User Selectable I^2C “Slave Only” Device Address: 1000_110x or 1000_111x
- User Selectable Adaptive Dead Time Scheme
  - PHASE Detect or LGATE Detect for Application Flexibility
- Variable Gate Drive Bias: 5V to 12V
- Multi-Processor Compatible
  - Intel VR10 and VR11 Modes of Operation
  - AMD Mode of Operation
- Microprocessor Voltage Identification Inputs
  - 8-Bit DAC
  - Selectable between Intel’s Extended VR10, VR11, AMD 5-bit, and AMD 6-bit DAC Tables
  - Dynamic VID Technology
- Overcurrent Protection
- Multi-Tiered Overvoltage Protection
- Digital Soft-Start
- Selectable Operation Frequency up to 1.5MHz Per Phase
- Pb-Free Plus Anneal Available (RoHS Compliant)

Ordering Information

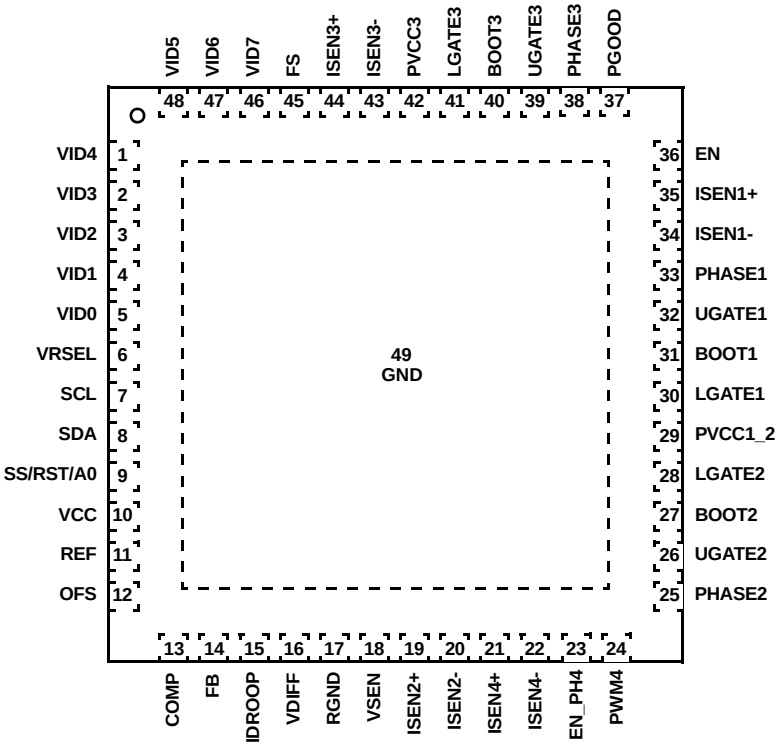
PART NUMBER* (Note)	PART MARKING	TEMP. (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6322CRZ	ISL6322CRZ	0 to 70	48 Ld 7x7 QFN	L48.7x7
ISL6322IRZ	ISL6322IRZ	-40 to 85	48 Ld 7x7 QFN	L48.7x7

*Add “-T” suffix for tape and reel.

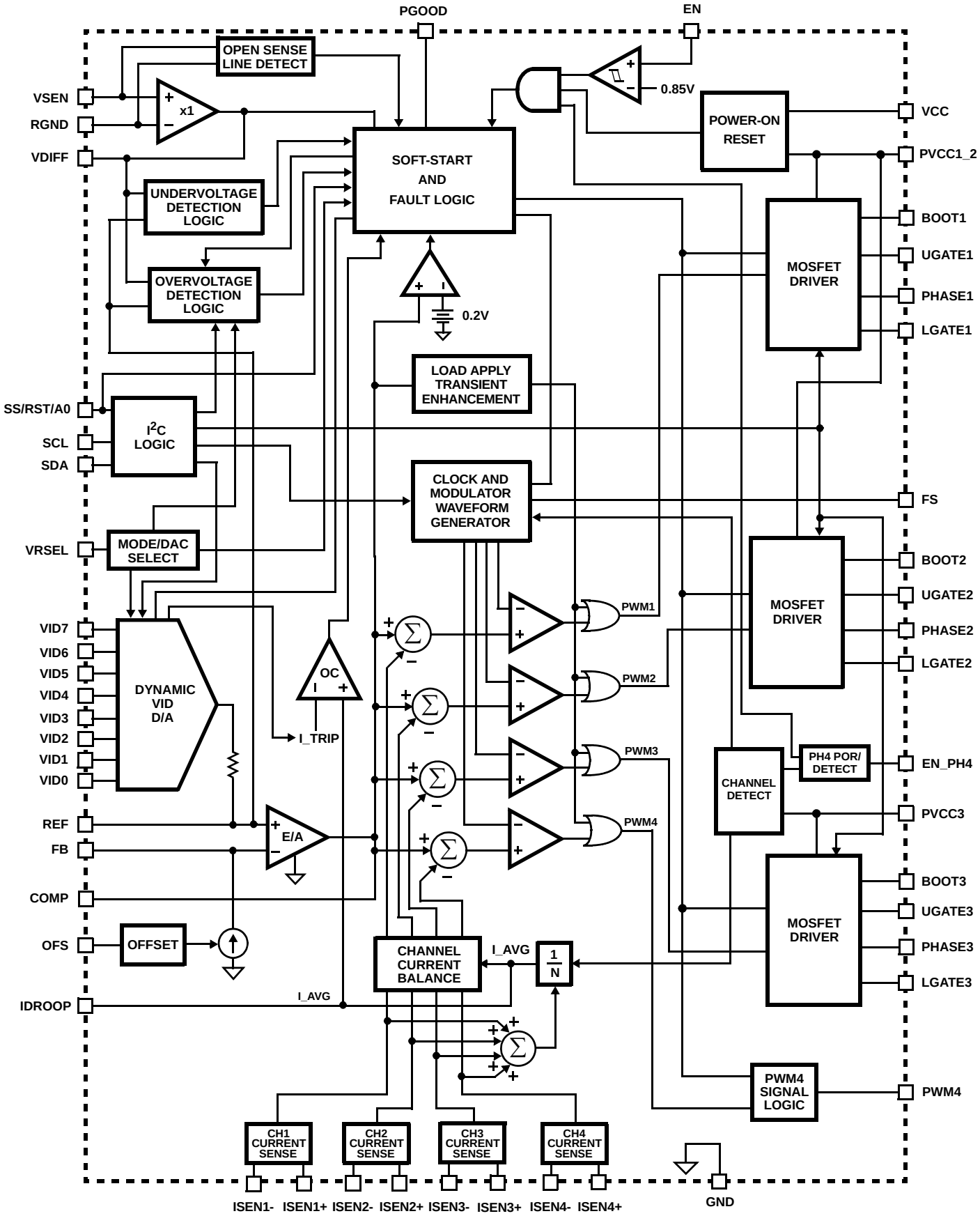
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinout

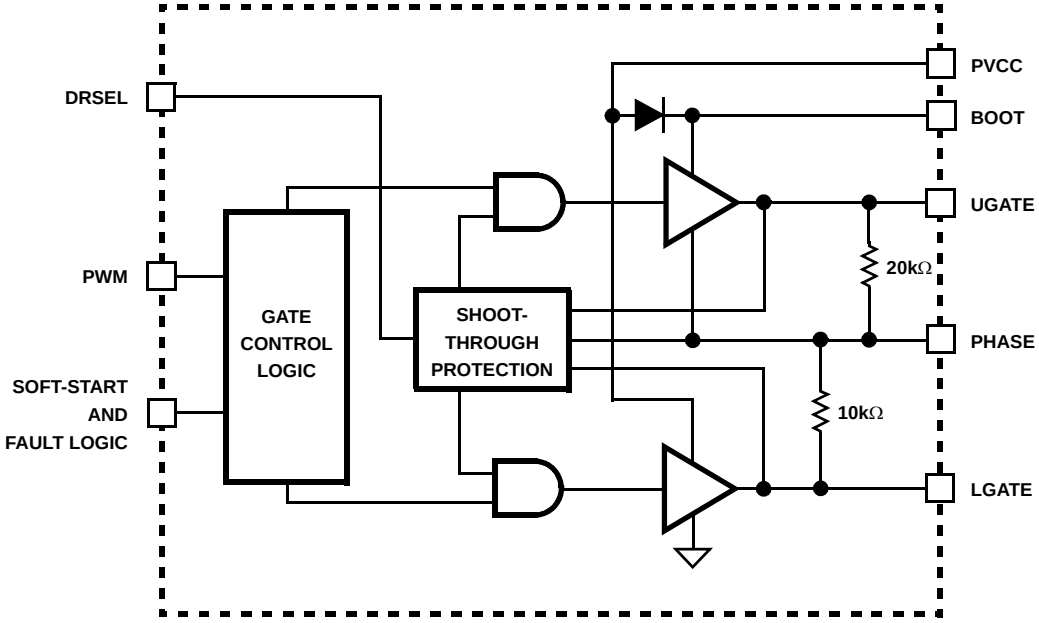
ISL6322 (48 LD QFN)
TOP VIEW



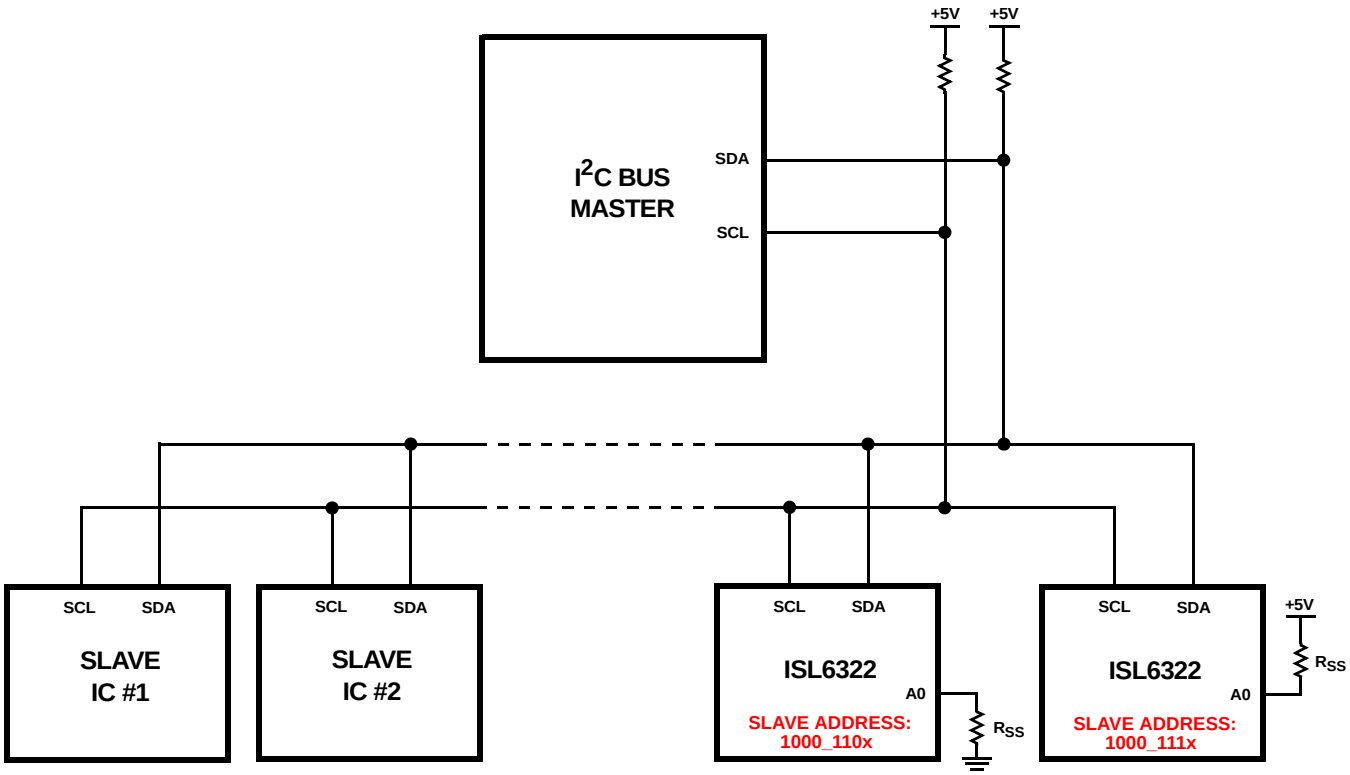
Block Diagram



ISL6322 Integrated Driver Block Diagram

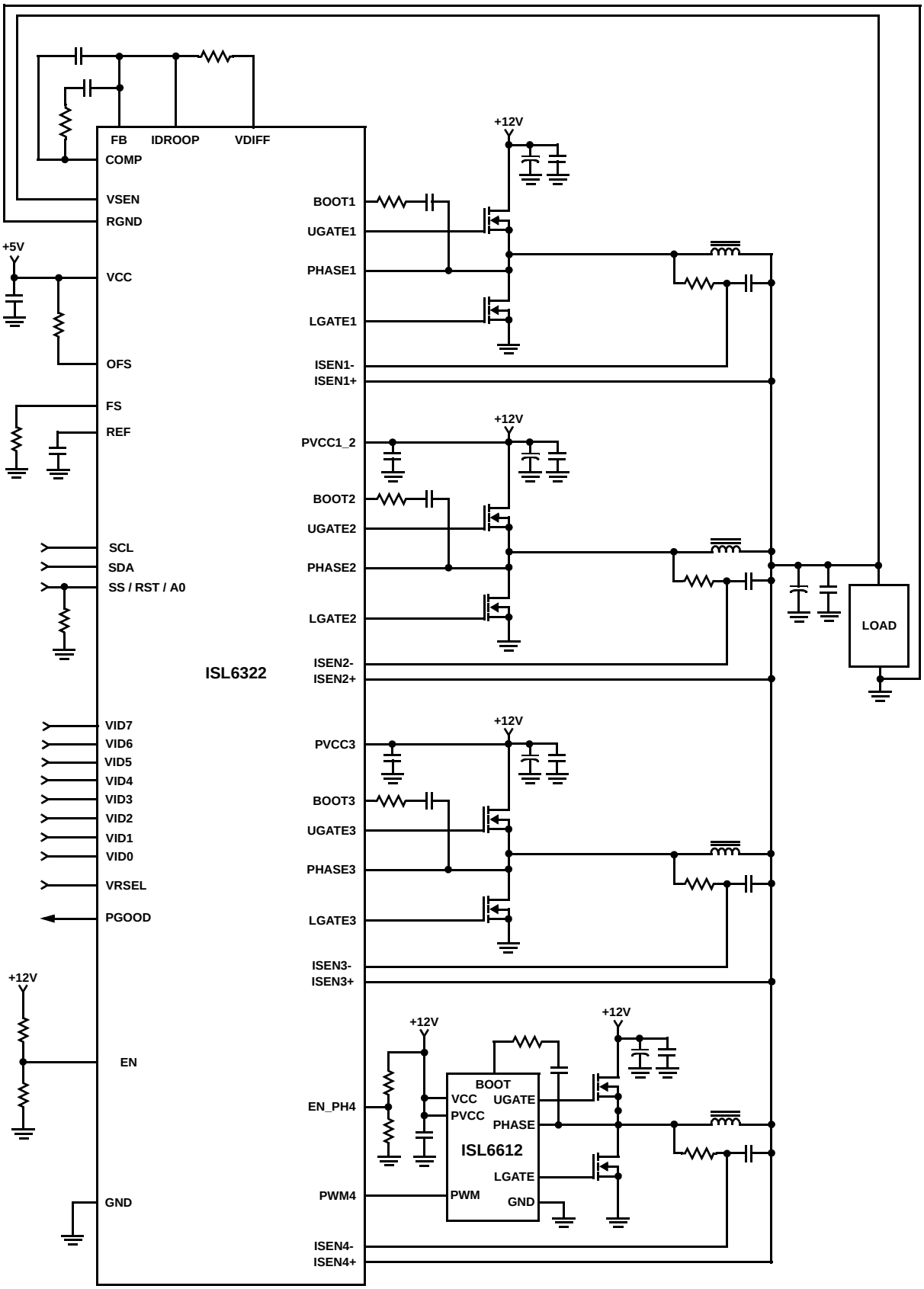


Simplified I²C Bus Architecture

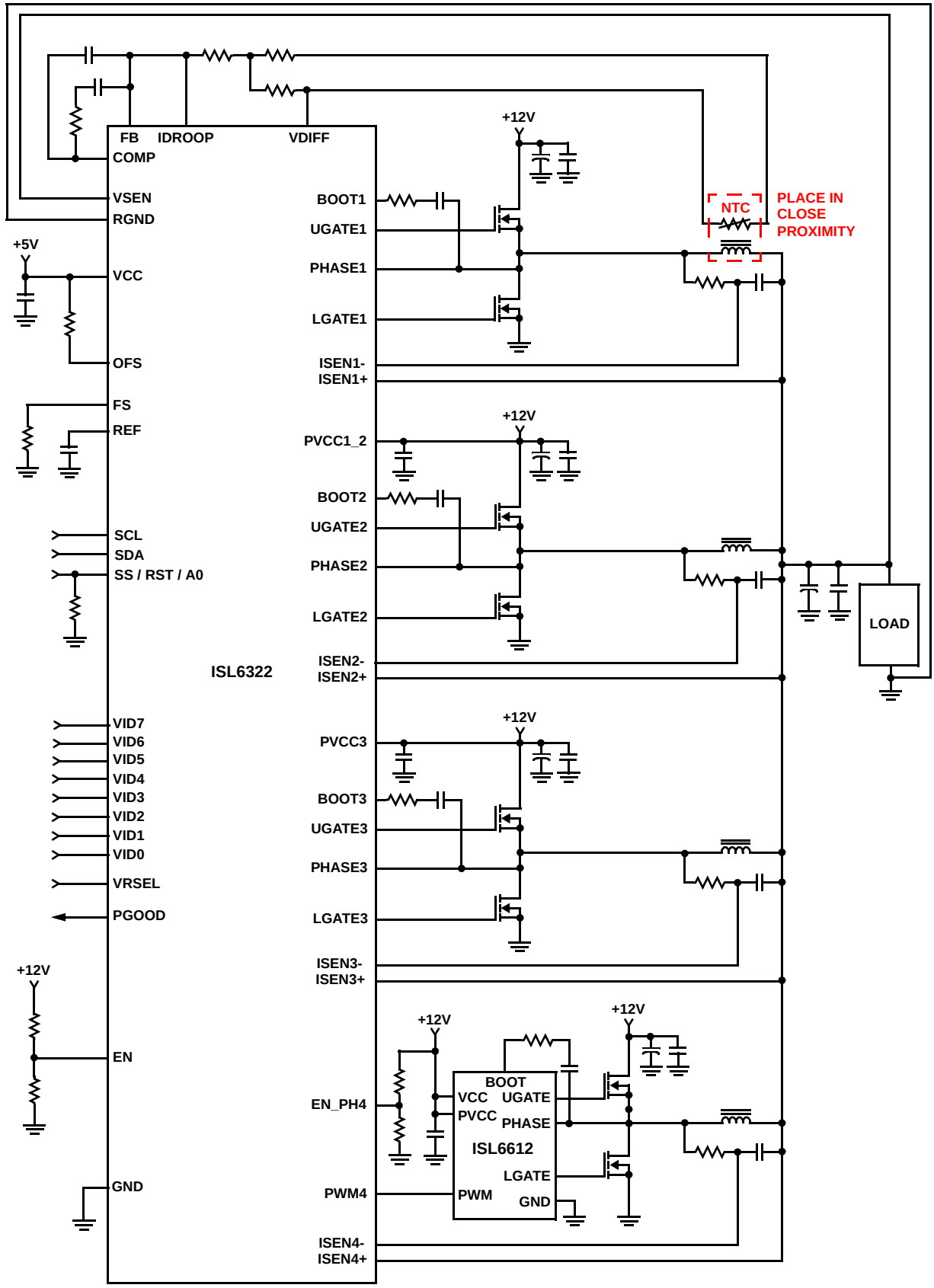


NOTE: PIN A0 SELECTS THE SLAVE ADDRESS FOR THE ISL6322

Typical Application - ISL6322 (4-Phase)



Typical Application - ISL6322 with NTC Thermal Compensation (4-Phase)



Absolute Maximum Ratings

Supply Voltage, VCC . . . . . -0.3V to +6V
Supply Voltage, PVCC . . . . . -0.3V to +15V
Absolute Boot Voltage, V_{BOOT} . . . . . GND - 0.3V to GND + 36V
Phase Voltage, V_{PHASE} . . . . . GND - 0.3V to 15V (PVCC = 12)
GND - 8V (<400ns, 20µJ) to 24V (<200ns, $V_{BOOT-PHASE}$ = 12V)
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
V_{PHASE} - 3.5V (<100ns Pulse Width, 2µJ) to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE}. . . . . GND - 0.3V to PVCC + 0.3V
GND - 5V (<100ns Pulse Width, 2µJ) to PVCC+ 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to VCC + 0.3V
ESD Classification . . . . . Class I JEDEC STD

Recommended Operating Conditions

VCC Supply Voltage . . . . . +5V ±5%
PVCC Supply Voltage . . . . . +5V to 12V ±5%
Ambient Temperature (ISL6322CRZ) . . . . . 0°C to +70°C
Ambient Temperature (ISL6322IRZ) . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	27	2.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Maximum Lead Temperature (Soldering 10s) . . . . . +300°C

CAUTION: Stress above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
3. Parameter magnitude guaranteed by design. Not 100% tested.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLIES					
Input Bias Supply Current	I_{VCC}; ENLL = high	15	20	25	mA
Gate Drive Bias Current - PVCC1_2 Pin	I_{PVCC1_2}; ENLL = high	2	4.3	6	mA
Gate Drive Bias Current - PVCC3 Pin	I_{PVCC3}; ENLL = high	1	2.1	3	mA
VCC POR (Power-On Reset) Threshold	VCC rising	4.25	4.38	4.50	V
	VCC falling	3.75	3.88	4.00	V
PVCC POR (Power-On Reset) Threshold	PVCC rising	4.25	4.38	4.50	V
	PVCC falling	3.60	3.88	4.00	V
PWM MODULATOR					
Oscillator Frequency Accuracy, F_{SW}	R_T = 100kΩ (± 0.1%)	225	250	275	kHz
Adjustment Range of Switching Frequency	(Note 3)	0.08		1.0	MHz
Oscillator Ramp Amplitude, V_{PP}	(Note 3)		1.50		V
Maximum Duty Cycle (Note 3)	(Note 3)		99.5		%
CONTROL THRESHOLDS					
ENLL Rising Threshold			0.85		V
ENLL Hysteresis			110		mV
EN_PH4 Rising Threshold		1.160	1.210	1.250	V
EN_PH4 Falling Threshold		1.00	1.06	1.10	V
COMP Shutdown Threshold	COMP falling	0.1	0.2	0.3	V

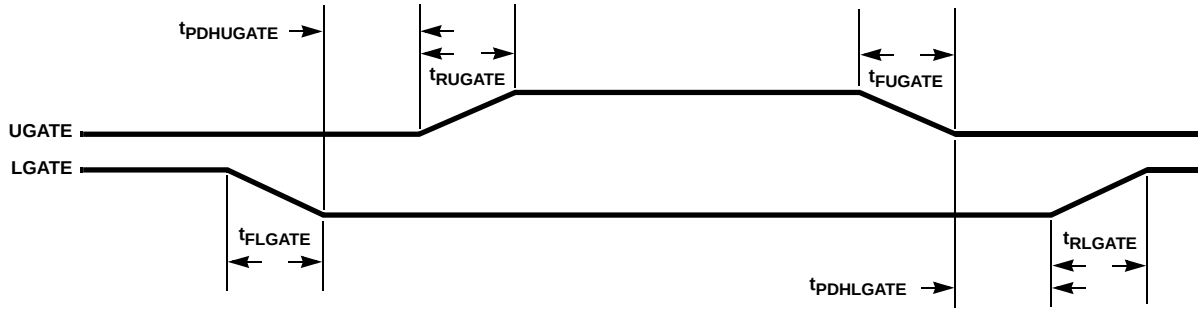
Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE AND DAC					
System Accuracy (1.000V - 1.600V)		-0.5		0.5	%
System Accuracy (0.600V - 1.000V)		-1.0		1.0	%
System Accuracy (0.375V - 0.600V)		-2.0		2.0	%
DAC Input Low Voltage (VR10, VR11)				0.4	V
DAC Input High Voltage (VR10, VR11)		0.8			V
DAC Input Low Voltage (AMD)				0.6	V
DAC Input High Voltage (AMD)		1.0			V
PIN-ADJUSTABLE OFFSET					
OFS Sink Current Accuracy (Negative Offset)	R_{OFS} = 10kΩ from OFS to GND	37.0	40.0	43.0	µA
OFS Source Current Accuracy (Positive Offset)	R_{OFS} = 30kΩ from OFS to VCC	50.5	53.5	56.5	µA
ERROR AMPLIFIER					
DC Gain	R_L = 10k to ground, (Note 3)		96		dB
Gain-Bandwidth Product	C_L = 100pF, R_L = 10k to ground, (Note 3)		20		MHz
Slew Rate	C_L = 100pF, Load = ±400µA, (Note 3)		8		V/µs
Maximum Output Voltage	Load = 1mA	3.90	4.20		V
Minimum Output Voltage	Load = -1mA		1.30	1.5	V
SOFT-START RAMP					
Soft-Start Ramp Rate	VR10/VR11, R_S = 100kΩ		1.563		mV/µs
	AMD		2.063		mV/µs
Adjustment Range of Soft-Start Ramp Rate (Note 3)		0.625		6.25	mV/µs
PWM OUTPUT					
PWM Output Voltage LOW Threshold	Iload = ±500µA			0.5	V
PWM Output Voltage HIGH Threshold	Iload = ±500µA	4.5			V
CURRENT SENSING					
Current Sense Resistance, R_{ISEN}	T = 25°C	297	300	303	Ω
Sensed Current Tolerance	ISEN1+ = ISEN2+ = ISEN3+ = ISEN4+ = 80µA	76	80	84	µA
OVERCURRENT PROTECTION					
Overcurrent Trip Level - Average Channel	Normal operation	110	125	140	µA
	Dynamic VID change	143	163	183	µA
Overcurrent Trip Level - Individual Channel	Normal operation	150	177	204	µA
	Dynamic VID change (Note 3)	209.4	238	266.6	µA
PROTECTION					
Undervoltage Threshold	VSEN falling	55	60	65	%VID
Undervoltage Hysteresis	VSEN rising		10		%VID
Overvoltage Threshold During Soft-Start	VR10/VR11	1.24	1.28	1.32	V
	AMD	2.13	2.20	2.27	V
Overvoltage Threshold (Default)	VSEN rising	VDAC + 225mV	VDAC + 250mV	VDAC + 275mV	V
Overvoltage Threshold (Alternate)	VSEN rising	VDAC + 150mV	VDAC + 175mV	VDAC + 200mV	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Hysteresis	VSEN falling		100		mV
SWITCHING TIME (Note 3)					
UGATE Rise Time	t_{RUGATE}; V_{PVCC} = 12V, 3nF load, 10% to 90%		26		ns
LGATE Rise Time	t_{RLGATE}; V_{PVCC} = 12V, 3nF load, 10% to 90%		18		ns
UGATE Fall Time	t_{FUGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%		18		ns
LGATE Fall Time	t_{FLGATE}; V_{PVCC} = 12V, 3nF load, 90% to 10%		12		ns
UGATE Turn-On Non-Overlap	$t_{PDHUGATE}$; V_{PVCC} = 12V, 3nF load, adaptive		10		ns
LGATE Turn-On Non-Overlap	$t_{PDHLGATE}$; V_{PVCC} = 12V, 3nF load, adaptive		10		ns
GATE DRIVE RESISTANCE (Note 3)					
Upper Drive Source Resistance	V_{PVCC} = 12V, 15mA source current	1.25	2.0	3.0	Ω
Upper Drive Sink Resistance	V_{PVCC} = 12V, 15mA sink current	0.9	1.65	3.0	Ω
Lower Drive Source Resistance	V_{PVCC} = 12V, 15mA source current	0.85	1.25	2.2	Ω
Lower Drive Sink Resistance	V_{PVCC} = 12V, 15mA sink current	0.60	0.80	1.35	Ω

Timing Diagram



Functional Pin Description

VCC

VCC is the bias supply for the ICs small-signal circuitry. Connect this pin to a +5V supply and decouple using a quality 0.1μF ceramic capacitor.

PVCC1_2 and PVCC3

These pins are the power supply pins for the corresponding channel MOSFET drive, and can be connected to any voltage from +5V to +12V depending on the desired MOSFET gate-drive level. Decouple these pins with a quality 1.0μF ceramic capacitor.

Leaving PVCC3 unconnected or grounded programs the controller for 2-phase operation.

GND

GND is the bias and reference ground for the IC.

EN

This pin is a threshold-sensitive (approximately 0.85V) enable input for the controller. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

FS

A resistor, placed from FS to ground, sets the switching frequency of the controller.

VID0, VID1, VID2, VID3, VID4, VID5, VID6, and VID7

These are the inputs for the internal DAC that provides the reference voltage for output regulation. These pins respond to TTL logic thresholds. These pins are internally pulled high, to approximately 1.2V, by 40μA internal current sources for Intel modes of operation, and pulled low by 20μA internal current sources for AMD modes of operation. The internal pull-up current decreases to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage (VCC).

VRSEL

The state of this pin selects which of the available DAC tables will be used to decode the VID inputs and puts the controller into the corresponding mode of operation. For VR10 mode of operation VRSEL should be less then 0.6V. The VR11 mode of operation can be selected by setting VRSEL between 0.6V and 3.0V, and AMD compliance is selected if this pin is between 3.0V and VCC.

VSEN and RGND

VSEN and RGND are inputs to the precision differential remote-sense amplifier and should be connected to the sense pins of the remote load.

VDIFF

VDIFF is the output of the differential remote-sense amplifier. The voltage on this pin is equal to the difference between VSEN and RGND.

FB and COMP

These pins are the internal error amplifier inverting input and output respectively. FB, VDIFF, and COMP are tied together through external R-C networks to compensate the regulator.

IDROOP

The IDROOP pin is the average channel-current sense output. Connecting this pin through a tuned parallel R-C network to FB allows the converter to incorporate output voltage droop proportional to the output current. If voltage droop is not desired leave this pin unconnected.

REF

The REF input pin is the positive input of the error amplifier. It is internally connected to the DAC output through a 1kΩ resistor. A capacitor is used between the REF pin and ground to smooth the voltage transition during Dynamic VID operations.

OFS

The OFS pin provides a means to program a DC current for generating an offset voltage across the resistor between FB and VDIFF. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFS pin should be left unconnected.

ISEN1-, ISEN1+, ISEN2-, ISEN2+, ISEN3-, ISEN3+, ISEN4-, and ISEN4+

These pins are used for differentially sensing the corresponding channel output currents. The sensed currents are used for channel balancing, protection, and load line regulation.

Connect ISEN1-, ISEN2-, ISEN3-, and ISEN4- to the node between the RC sense elements surrounding the inductor of their respective channel. Tie the ISEN+ pins to the VCORE side of their corresponding channel's sense capacitor.

UGATE1, UGATE2, and UGATE3

Connect these pins to the corresponding upper MOSFET gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes.

BOOT1, BOOT2, and BOOT3

These pins provide the bias voltage for the corresponding upper MOSFET drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

PHASE1, PHASE2, and PHASE3

Connect these pins to the sources of the corresponding upper MOSFETs. These pins are the return path for the upper MOSFET drives.

LGATE1, LGATE2, and LGATE3

These pins are used to control the lower MOSFETs. Connect these pins to the corresponding lower MOSFETs' gates.

PWM4

Pulse-width modulation output. Connect this pin to the PWM input pin of an Intersil driver IC if 4-phase operation is desired.

EN_PH4

This pin has two functions. First, a resistor divider connected to this pin will provide a POR power-up synch between the on-chip and external driver. The resistor divider should be designed so that when the POR-trip point of the external driver is reached the voltage on this pin should be 1.21V.

The second function of this pin is disabling PWM4 for 3-phase operation. This can be accomplished by connecting this pin to a +5V supply.

SS/RST/A0

This pin has three different functions associated with it. The first is that a resistor (R_{SS}), placed from this pin to ground, or VCC, will set the soft-start ramp slope for the Intel DAC modes of operation. Refer to Equations 18 and 19 for proper resistor calculation.

The second function of this pin is that it selects which of the two 8-bit Slave I^2C addresses the controller will use. Connecting the R_{SS} resistor on this pin to ground will choose slave address one(1000_110x), while connecting this resistor to VCC will select slave address two(1000_111x).

The third function of this pin is a reset to the I^2C registers. During normal operation of the part, if this pin is ever grounded, all of the I^2C registers are reset to 0000_0000. An open drain device is recommended as the means of grounding this pin for resetting the I^2C registers.

SCL

Connect this pin to the clock signal for the I^2C bus, which is a logic level input signal. The clock signal tells the controller when data is available on the I^2C bus.

SDA

Connect this pin to the bidirectional data line of the I^2C bus, which is a logic level input/output signal. All I^2C data is sent over this line, including the address of the device the bus is trying to communicate with, and what functions the device should perform.

PGOOD

During normal operation PGOOD indicates whether the output voltage is within specified overvoltage and undervoltage limits. If the output voltage exceeds these limits or a reset event occurs (such as an overcurrent event), PGOOD is pulled low. PGOOD is always low prior to the end of soft-start.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that using single-phase regulators is no longer a viable solution. Designing a regulator that is cost-effective, thermally sound, and efficient has become a challenge that only multiphase converters can accomplish. The ISL6322 controller helps simplify implementation by integrating vital functions and requiring minimal external components. The block diagram on page 3 provides a top level view of multiphase power conversion using the ISL6322 controller.

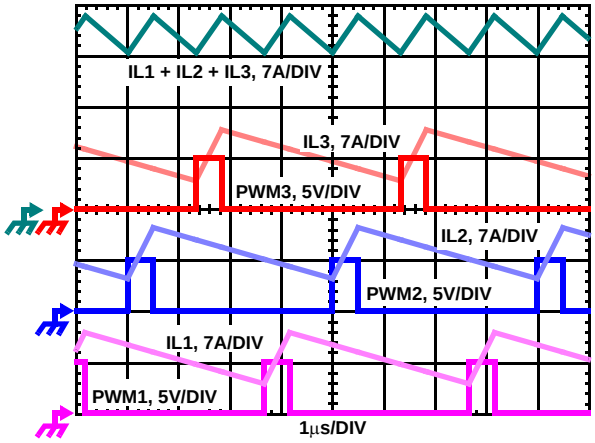


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the three-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM

pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine the equation representing an individual channel peak-to-peak inductor current.

$$I_{PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,PP} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 2)}$$

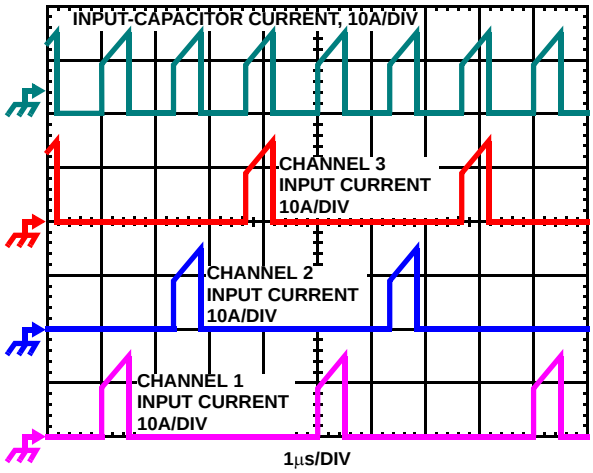


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a three-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 1.5V to a 36A load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent three-phase converter.

Active Pulse Positioning (APP) Modulated PWM Operation

The ISL6322 uses a proprietary Active Pulse Positioning (APP) modulation scheme to control the internal PWM signals that command each channel's driver to turn their upper and lower MOSFETs on and off. The time interval in which a PWM signal can occur is generated by an internal clock, whose cycle time is the inverse of the switching frequency set by the resistor between the FS pin and ground. The advantage of Intersil's proprietary Active Pulse Positioning (APP) modulator is that the PWM signal has the ability to turn on at any point during this PWM time interval, and turn off immediately after the PWM signal has transitioned high. This is important because is allows the controller to quickly respond to output voltage drops associated with current load spikes, while avoiding the ring back affects associated with other modulation schemes.

The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction signal relative to the proprietary modulator ramp waveform as illustrated in Figure 3. At the beginning of each PWM time interval, this modified V_{COMP} signal is compared to the internal modulator waveform. As long as the modified V_{COMP} voltage is lower then the modulator waveform voltage, the PWM signal is commanded low. The internal MOSFET driver detects the low state of the PWM signal and turns off the upper MOSFET and turns on the lower synchronous MOSFET. When the modified V_{COMP} voltage crosses the modulator ramp, the PWM output transitions high, turning off the synchronous MOSFET and turning on the upper MOSFET. The PWM signal will remain high until the modified V_{COMP} voltage crosses the modulator ramp again. When this occurs the PWM signal will transition low again.

During each PWM time interval the PWM signal can only transition high once. Once PWM transitions high it can not transition high again until the beginning of the next PWM time interval. This prevents the occurrence of double PWM pulses occurring during a single period.

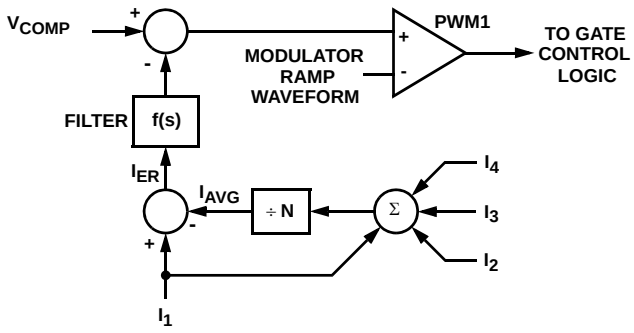
To further improve the transient response, ISL6322 also implements Intersil's proprietary Adaptive Phase Alignment (APA) technique, which turns on all phases together under transient events with large step current. With both APP and APA control, ISL6322 can achieve excellent transient performance and reduce the demand on the output capacitors.

Channel-Current Balance

One important benefit of multiphase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this the designer avoids the complexity of driving parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to realize the thermal advantage, it is important that each channel in a multiphase converter be controlled to carry equal amounts of current at any load level. To achieve this, the currents through each channel must be sampled every switching cycle. The sampled currents, I_n, from each active channel are summed together and divided by the number of active channels. The resulting cycle average current, I_{AVG}, provides a measure of the total load-current demand on the converter during each switching cycle. Channel-current balance is achieved by comparing the sampled current of each channel to the cycle average current, and making the proper adjustment to each channel pulse width based on the error. Intersil's patented current-balance method is illustrated in Figure 3, with error correction for channel 1 represented. In the figure, the cycle average current, I_{AVG}, is compared with the channel 1 sample, I_1, to create an error signal I_{ER}.

The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: CHANNEL 3 AND 4 ARE OPTIONAL.

FIGURE 3. CHANNEL-1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Continuous Current Sampling

In order to realize proper current-balance, the currents in each channel are sensed continuously every switching cycle. During this time the current-sense amplifier uses the ISEN inputs to reproduce a signal proportional to the inductor current, I_L. This sensed current, I_{SEN}, is simply a scaled version of the inductor current.

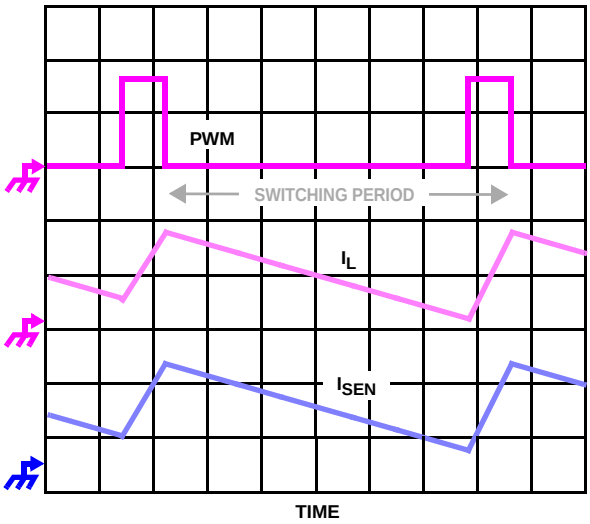


FIGURE 4. CONTINUOUS CURRENT SAMPLING

The ISL6322 supports inductor DCR current sensing to continuously sense each channel's current for channel-current balance. The internal circuitry, shown in Figure 5 represents channel n of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on how many channels are operating.

Inductor windings have a characteristic distributed resistance or DCR (Direct Current Resistance). For simplicity, the inductor DCR is considered as a separate lumped quantity, as shown in Figure 5. The channel current I_L, flowing through the inductor, passes through the DCR. Equation 3 shows the s-domain equivalent voltage, V_L, across the inductor.

$$V_L(s) = I_L \cdot (s \cdot L + DCR) \quad \text{(EQ. 3)}$$

A simple R-C network across the inductor (R_1 and C) extracts the DCR voltage, as shown in Figure 5. The voltage across the sense capacitor, V_C, can be shown to be proportional to the channel current I_L, shown in Equation 4.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{(s \cdot R_1 \cdot C + 1)} \cdot DCR \cdot I_L \quad \text{(EQ. 4)}$$

In some cases it may be necessary to use a resistor divider R-C network to sense the current through the inductor. This can be accomplished by placing a second resistor, R_2, across the sense capacitor. In these cases the voltage

across the sense capacitor, V_C, becomes proportional to the channel current I_L, and the resistor divider ratio, K.

$$V_C(s) = \frac{\left(\frac{s \cdot L}{DCR} + 1\right)}{\left(s \cdot \frac{(R_1 \cdot R_2)}{R_1 + R_2} \cdot C + 1\right)} \cdot K \cdot DCR \cdot I_L \quad \text{(EQ. 5)}$$

$$K = \frac{R_2}{R_2 + R_1} \quad \text{(EQ. 6)}$$

If the R-C network components are selected such that the RC time constant matches the inductor L/DCR time constant, then V_C is equal to the voltage drop across the DCR multiplied by the ratio of the resistor divider, K. **If a resistor divider is not being used, the value for K is 1**.

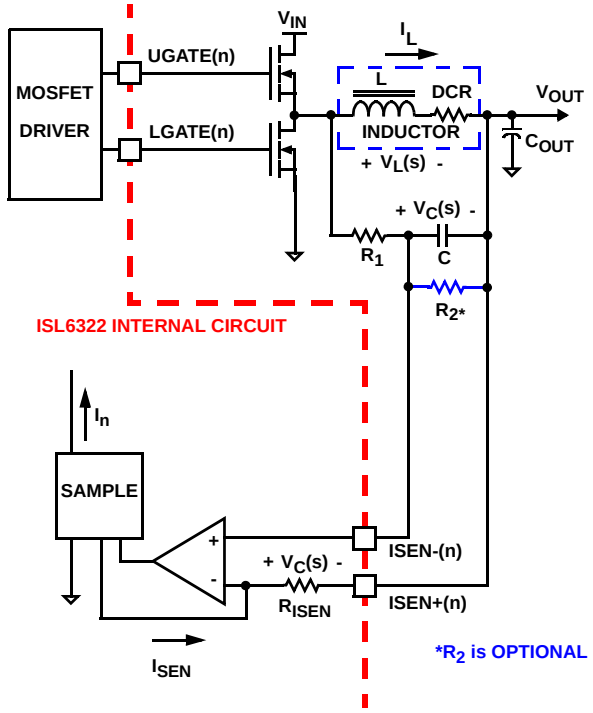


FIGURE 5. INDUCTOR DCR CURRENT SENSING CONFIGURATION

The capacitor voltage V_C, is then replicated across the sense resistor R_{ISEN}. The current through R_{ISEN} is proportional to the inductor current. Equation 7 shows that the proportion between the channel current and the sensed current (I_{SEN}) is driven by the value of the sense resistor, the resistor divider ratio, and the DCR of the inductor.

$$I_n = K \cdot I_L \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 7)}$$

Output Voltage Setting

The ISL6322 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the logic signals into one of the discrete voltages shown in Tables 2, 3, 4 and 5. In Intel modes of operation, each VID pin is pulled up to an internal 1.2V voltage by a weak current source (40µA), which decreases to 0A as the voltage at the VID pin varies from 0 to the internal 1.2V pull-up voltage. In AMD modes of operation the VID pins are pulled low by a weak 20µA current source. External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL6322 accommodates four different DAC ranges: Intel VR10 (Extended), Intel VR11, AMD K8/K9 5-bit, and AMD 6-bit. The state of the VRSEL and VID7 pins decide which DAC version is active. Refer to Table 1 for a description of how to select the desired DAC version.

TABLE 1. ISL6322 DAC SELECT TABLE

DAC VERSION	VRSEL PIN	VID7 PIN
VR10(Extended)	VRSEL < 0.6V	-
VR11	0.8V < VRSEL < 3.0V	-
AMD 5-Bit	3.0V < VRSEL < VCC	low
AMD 6-Bit	3.0V < VRSEL < VCC	high

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125

TABLE 2. VR10 (EXTENDED) VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VID6	VDAC
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875

TABLE 3. VR11 VOLTAGE IDENTIFICATION CODES (Continued)

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625
1	0	1	1	0	0	1	0	0.50000
1	1	1	1	1	1	1	0	OFF
1	1	1	1	1	1	1	1	OFF

TABLE 4. AMD 5-BIT VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075
1	0	0	1	0	1.100
1	0	0	0	1	1.125

TABLE 4. AMD 5-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 5. AMD 6-BIT VOLTAGE IDENTIFICATION CODES

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	0	0	0	0	1.5500
0	0	0	0	0	1	1.5250
0	0	0	0	1	0	1.5000
0	0	0	0	1	1	1.4750
0	0	0	1	0	0	1.4500
0	0	0	1	0	1	1.4250
0	0	0	1	1	0	1.4000
0	0	0	1	1	1	1.3750
0	0	1	0	0	0	1.3500
0	0	1	0	0	1	1.3250
0	0	1	0	1	0	1.3000
0	0	1	0	1	1	1.2750
0	0	1	1	0	0	1.2500
0	0	1	1	0	1	1.2250
0	0	1	1	1	0	1.2000
0	0	1	1	1	1	1.1750
0	1	0	0	0	0	1.1500
0	1	0	0	0	1	1.1250
0	1	0	0	1	0	1.1000

TABLE 5. AMD 6-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	1	0	0	1	1	1.0750
0	1	0	1	0	0	1.0500
0	1	0	1	0	1	1.0250
0	1	0	1	1	0	1.0000
0	1	0	1	1	1	0.9750
0	1	1	0	0	0	0.9500
0	1	1	0	0	1	0.9250
0	1	1	0	1	0	0.9000
0	1	1	0	1	1	0.8750
0	1	1	1	0	0	0.8500
0	1	1	1	0	1	0.8250
0	1	1	1	1	0	0.8000
0	1	1	1	1	1	0.7750
1	0	0	0	0	0	0.7625
1	0	0	0	0	1	0.7500
1	0	0	0	1	0	0.7375
1	0	0	0	1	1	0.7250
1	0	0	1	0	0	0.7125
1	0	0	1	0	1	0.7000
1	0	0	1	1	0	0.6875
1	0	0	1	1	1	0.6750
1	0	1	0	0	0	0.6625
1	0	1	0	0	1	0.6500
1	0	1	0	1	0	0.6375
1	0	1	0	1	1	0.6250
1	0	1	1	0	0	0.6125
1	0	1	1	0	1	0.6000
1	0	1	1	1	0	0.5875
1	0	1	1	1	1	0.5750
1	1	0	0	0	0	0.5625
1	1	0	0	0	1	0.5500
1	1	0	0	1	0	0.5375
1	1	0	0	1	1	0.5250
1	1	0	1	0	0	0.5125
1	1	0	1	0	1	0.5000
1	1	0	1	1	0	0.4875
1	1	0	1	1	1	0.4750
1	1	1	0	0	0	0.4625
1	1	1	0	0	1	0.4500

TABLE 5. AMD 6-BIT VOLTAGE IDENTIFICATION CODES (Continued)

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	0	1	0	0.4375
1	1	1	0	1	1	0.4250
1	1	1	1	0	0	0.4125
1	1	1	1	0	1	0.4000
1	1	1	1	1	0	0.3875
1	1	1	1	1	1	0.3750

Voltage Regulation

The integrating compensation network shown in Figure 6 insures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFS current source, remote-sense and error amplifiers. Intersil specifies the guaranteed tolerance of the ISL6322 to include the combined tolerances of each of these elements.

The output of the error amplifier, V_{COMP}, is compared to the triangle waveform to generate the PWM signals. The PWM signals control the timing of the Internal MOSFET drivers and regulate the converter output so that the voltage at FB is equal to the voltage at REF. This will regulate the output voltage to be equal to Equation 8. The internal and external circuitry that controls voltage regulation is illustrated in Figure 6.

$$V_{OUT} = V_{REF} - V_{OFS} - V_{DROOP} \quad \text{(EQ. 8)}$$

The ISL6322 incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, VSEN, and inverting input, RGND, of the remote-sense amplifier. The remote-sense output, V_{DIFF}, is connected to the inverting input of the error amplifier through an external resistor.

Load-Line (Droop) Regulation

Some microprocessor manufacturers require a precisely controlled output resistance. This dependence of output voltage on load current is often termed “droop” or “load line” regulation. By adding a well controlled output impedance, the output voltage can effectively be level shifted in a direction which works to achieve the load-line regulation required by these manufacturers.

In other cases, the designer may determine that a more cost-effective solution can be achieved by adding droop. Droop can help to reduce the output-voltage spike that results from fast load-current demand changes.

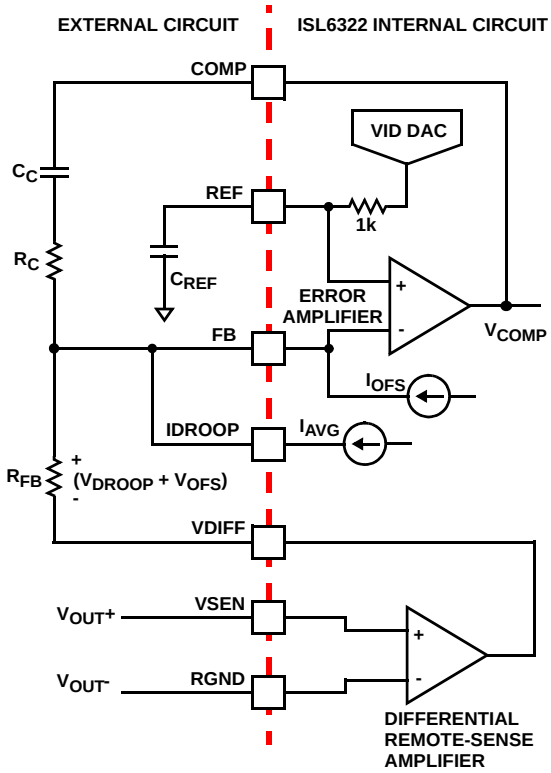


FIGURE 6. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

The magnitude of the spike is dictated by the ESR and ESL of the output capacitors selected. By positioning the no-load voltage level near the upper specification limit, a larger negative spike can be sustained without crossing the lower limit. By adding a well controlled output impedance, the output voltage under load can effectively be level shifted down so that a larger positive spike can be sustained without crossing the upper specification limit.

As shown in Figure 6, a current proportional to the average current of all active channels, I_{AVG}, flows from FB through a load-line regulation resistor R_{FB}. The resulting voltage drop across R_{FB} is proportional to the output current, effectively creating an output voltage droop with a steady-state value defined as

$$V_{DROOP} = I_{AVG} \cdot R_{FB} \quad \text{(EQ. 9)}$$

The regulated output voltage is reduced by the droop voltage V_{DROOP}. The output voltage as a function of load current is derived by combining Equation 9 with Equation 10.

$$V_{OUT} = V_{REF} - V_{OFS} - \left(\frac{I_{OUT}}{N} \cdot \frac{DCR}{R_{ISEN}} \cdot R_{FB}\right) \quad \text{(EQ. 10)}$$

In Equation 10, V_{REF} is the reference voltage, V_{OFS} is the programmed offset voltage, I_{OUT} is the total output current of the converter, R_{ISEN} is the internal sense resistor connected to the ISEN+ pin, and R_{FB} is the feedback

resistor, N is the active channel number, and DCR is the Inductor DCR value.

Therefore the equivalent load-line impedance, i.e. droop impedance, is equal to:

$$R_{LL} = \frac{R_{FB}}{N} \cdot \frac{DCR}{R_{ISEN}} \quad \text{(EQ. 11)}$$

Output-Voltage Offset Programming

The ISL6322 allows the designer to accurately adjust the offset voltage by connecting a resistor, R_{OFS}, from the OFS pin to VCC or GND. When R_{OFS} is connected between OFS and VCC, the voltage across it is regulated to 1.6V. This causes a proportional current (I_{OFS}) to flow into the FB pin and out of the OFS pin. If R_{OFS} is connected to ground, the voltage across it is regulated to 0.4V, and I_{OFS} flows into the OFS pin and out of the FB pin. The offset current flowing through the resistor between VDIFF and FB will generate the desired offset voltage which is equal to the product (I_{OFS} x R_{FB}). These functions are shown in Figures 7 and 8.

Once the desired output offset voltage has been determined, use the following formulas to set R_{OFS}:

For Negative Offset (connect R_{OFS} to GND):

$$R_{OFS} = \frac{0.4 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 12)}$$

For Positive Offset (connect R_{OFS} to VCC):

$$R_{OFS} = \frac{1.6 \cdot R_{FB}}{V_{OFFSET}} \quad \text{(EQ. 13)}$$

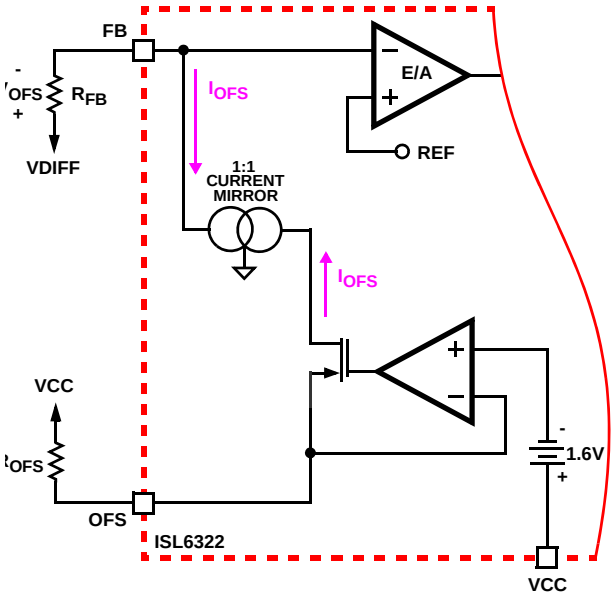


FIGURE 7. POSITIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

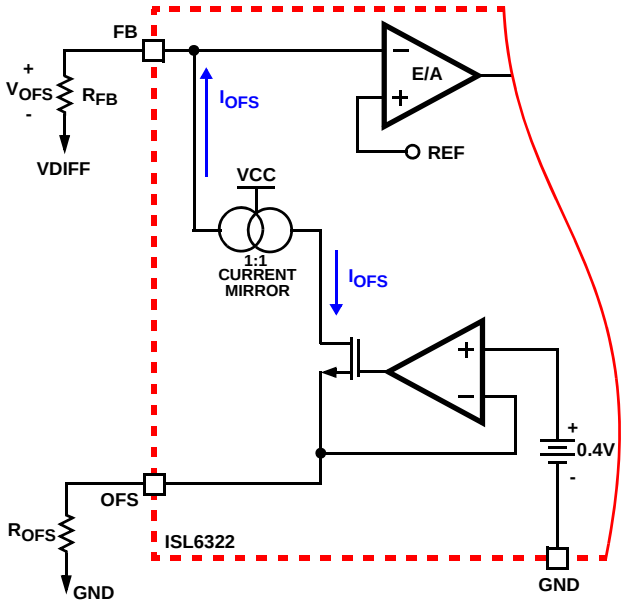


FIGURE 8. NEGATIVE OFFSET OUTPUT VOLTAGE PROGRAMMING

Dynamic VID

Modern microprocessors need to make changes to their core voltage as part of normal operation. They direct the ISL6322 to do this by making changes to the VID inputs. The ISL6322 is required to monitor the DAC inputs and respond to on-the-fly VID changes in a controlled manner, supervising a safe output voltage transition without discontinuity or disruption. The DAC mode the ISL6322 is operating in determines how the controller responds to a dynamic VID change.

Intel Dynamic VID Transitions

When in Intel VR10 or VR11 mode, the ISL6322 checks the VID inputs on the positive edge of an internal 3MHz clock. If a new code is established and it remains stable for 3 consecutive readings (1µs to 1.33µs), the ISL6322 recognizes the new code and changes the internal DAC reference directly to the new level. The Intel processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VR10 and VR11 settings, the ISL6322 will immediately change the internal DAC reference to the new requested value as soon as the request is validated, which means the fastest recommended rate at which a bit change can occur is once every 2µs. In cases where the reference step is too large, the sudden change can trigger overcurrent or overvoltage events.

In order to ensure the smooth transition of output voltage during a VR10 or VR11 VID change, a VID step change smoothing network is required. This network is composed of an internal 1kΩ resistor between the DAC and the REF pin, and the external capacitor C_{REF}, between the REF pin and

ground. The selection of C_{REF} is based on the time duration for 1 bit VID change and the allowable delay time.

Assuming the microprocessor controls the VID change at 1 bit every T_{VID}, the relationship between C_{REF} and T_{VID} is given by Equation 14.

$$C_{REF} = 0.001(S) \cdot T_{VID} \quad \text{(EQ. 14)}$$

As an example, for a VID step change rate of 5µs per bit, the value of C_{REF} is 5600pF based on Equation 14.

AMD Dynamic VID Transitions

When running in AMD 5-bit or 6-bit modes of operation, the ISL6322 responds differently to a dynamic VID change than when in Intel VR10 or VR11 mode. In the AMD modes, the ISL6322 still checks the VID inputs on the positive edge of an internal 3MHz clock. In these modes the VID code can be changed by more than a 1-bit step at a time. If a new code is established and it remains stable for 3 consecutive readings (1µs to 1.33µs), the ISL6322 recognizes the change and begins slewing the DAC in 6.25mV steps at a stepping frequency of 330kHz until the VID and DAC are equal. Thus, the total time required for a VID change, t_{DVID}, is dependent only on the size of the VID change (ΔV_{VID}).

The time required for a ISL6322-based converter in AMD 5-bit DAC configuration to make a 1.1V to 1.5V reference voltage change is about 194µs, as calculated using the following equation.

$$t_{DVID} = \frac{1}{330 \times 10^3} \cdot \left(\frac{\Delta V_{VID}}{0.00625}\right) \quad \text{(EQ. 15)}$$

In order to ensure the smooth transition of output voltage during an AMD VID change, a VID step change smoothing network is required. This network is composed of an internal 1kΩ resistor between the DAC and the REF pin, and the external capacitor C_{REF}, between the REF pin and ground. For AMD VID transitions C_{REF} should be a 1000pF capacitor.

User Selectable Adaptive Deadtime Control Techniques

The ISL6322 integrated drivers incorporate two different adaptive deadtime control techniques, which the user can choose between. Both of these control techniques help to minimize deadtime, resulting in high efficiency from the reduced freewheeling time of the lower MOSFET body-diode conduction, and both help to prevent the upper and lower MOSFETs from conducting simultaneously. This is accomplished by ensuring either rising gate turns on its MOSFET with minimum and sufficient delay after the other has turned off.

The difference between the two adaptive deadtime control techniques is the method in which they detect that the lower MOSFET has transitioned off in order to turn on the upper MOSFET. The state of the internal I^2C registers determines which of the two control techniques is active (see pages 27 through 31 for details of controlling deadtime control with I^2C). The default setting is PHASE Detect. If the PHASE Detect Scheme is chosen, the voltage on the PHASE pin is monitored to determine if the lower MOSFET has transitioned off or not. Choosing the LGATE Detect Scheme instructs the controller to monitor the voltage on the LGATE pin to determine if the lower MOSFET has turned off or not. For both schemes, the method for determining whether the upper MOSFET has transitioned off in order to signal to turn on the lower MOSFET is the same.

PHASE Detect

For the PHASE detect scheme, during turn-off of the lower MOSFET, the PHASE voltage is monitored until it reaches a -0.3V/+0.8V (forward/reverse inductor current). At this time the UGATE is released to rise. An auto-zero comparator is used to correct the $r_{DS(ON)}$ drop in the phase voltage preventing false detection of the -0.3V phase level during $r_{DS(ON)}$ conduction period. In the case of zero current, the UGATE is released after 35ns delay of the LGATE dropping below 0.5V. When LGATE first begins to transition low, this quick transition can disturb the PHASE node and cause a false trip, so there is 20ns of blanking time once LGATE falls until PHASE is monitored.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

LGATE Detect

For the LGATE detect scheme, during turn-off of the lower MOSFET, the LGATE voltage is monitored until it reaches 1.75V. At this time the UGATE is released to rise.

Once the PHASE is high, the advanced adaptive shoot-through circuitry monitors the PHASE and UGATE voltages during a PWM falling edge and the subsequent UGATE turn-off. If either the UGATE falls to less than 1.75V above the PHASE or the PHASE falls to less than +0.8V, the LGATE is released to turn-on.

Internal Bootstrap Device

All three integrated drivers feature an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the PHASE node. This reduces voltage stress on the boot to phase pins.

The bootstrap capacitor must have a maximum voltage rating above PVCC + 4V and its capacitance value can be chosen from the following equation:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 16)}$$

$$Q_{GATE} = \frac{Q_{G1} \cdot PVCC}{V_{GS1}} \cdot N_{Q1}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive.

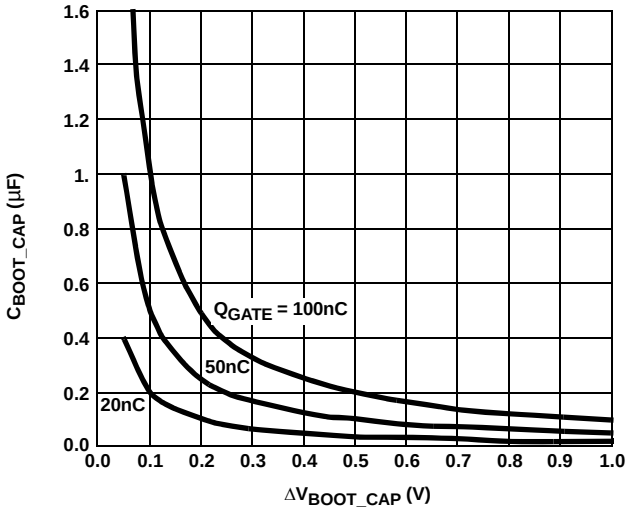


FIGURE 9. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Gate Drive Voltage Versatility

The ISL6322 provides the user flexibility in choosing the gate drive voltage for efficiency optimization. The controller ties the upper and lower drive rails together. Simply applying a voltage from 5V up to 12V on PVCC sets both gate drive rail voltages simultaneously.

Initialization

Prior to initialization, proper conditions must exist on the EN, VCC, PVCC and the VID pins. When the conditions are met, the controller begins soft-start. Once the output voltage is within the proper window of operation, the controller asserts PGOOD.

Enable and Disable

While in shutdown mode, the PWM outputs are held in a high-impedance state to assure the drivers remain off. The following input conditions must be met, for both Intel and AMD modes of operation, before the ISL6322 is released from shutdown mode to begin the soft-start startup sequence:

1. The bias voltage applied at VCC must reach the internal power-on reset (POR) rising threshold. Once this threshold is reached, proper operation of all aspects of the ISL6322 is guaranteed. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6322 will not inadvertently turn off unless the bias voltage drops substantially (see *Electrical Specifications on page* 7).

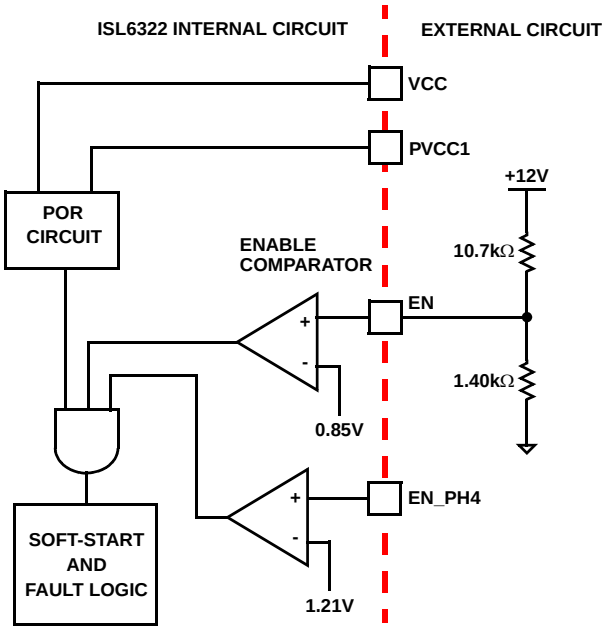


FIGURE 10. POWER SEQUENCING USING THRESHOLD-SENSITIVE ENABLE (EN) FUNCTION

2. The voltage on EN must be above 0.85V. The EN input allows for power sequencing between the controller bias voltage and another voltage rail. The enable comparator holds the ISL6322 in shutdown until the voltage at EN rises above 0.85V. The enable comparator has 110mV of hysteresis to prevent bounce.
3. The voltage on the EN_PH4 pin must be above 1.21V. The EN_PH4 input allows for power sequencing between the controller and the external driver.
4. The driver bias voltage applied at the PVCC pins must reach the internal power-on reset (POR) rising threshold. In order for the ISL6322 to begin operation, PVCC1 is the only pin that is required to have a voltage applied that exceeds POR. However, for 2 or 3-phase operation PVCC2 and PVCC3 must also exceed the POR threshold. Hysteresis between the rising and falling thresholds assure that once enabled, the ISL6322 will not inadvertently turn off unless the PVCC bias voltage drops substantially (see *Electrical Specifications on page* 7).

For Intel VR10, VR11 and AMD 6-bit modes of operation these are the only conditions that must be met for the controller to immediately begin the soft-start sequence. If running in AMD 5-bit mode of operation there is one more condition that must be met:

5. The VID code must not be 11111 in AMD 5-bit mode. This code signals the controller that no load is present. The controller will not allow soft-start to begin if this VID code is present on the VID pins.

Once all of these conditions are met the controller will begin the soft-start sequence and will ramp the output voltage up to the user designated level.

Intel Soft-Start

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. The soft-start sequence for the Intel modes of operation is slightly different then the AMD soft-start sequence.

For the Intel VR10 and VR11 modes of operation, the soft-start sequence is composed of four periods, as shown in Figure 11. Once the ISL6322 is released from shutdown and soft-start begins (as described in the *Enable and Disable* section), the controller will have fixed delay period TD1. After this delay period, the VR will begin first soft-start ramp until the output voltage reaches 1.1V VBOOT voltage. Then, the controller will regulate the VR voltage at 1.1V for another fixed period TD3. At the end of TD3 period, ISL6322 will read the VID signals. If the VID code is valid, ISL6322 will initiate the second soft-start ramp until the output voltage reaches the VID voltage plus/minus any offset or droop voltage.

The soft-start time is the sum of the four periods as shown in Equation 17.

$$T_{SS} = TD1 + TD2 + TD3 + TD4 \quad \text{(EQ. 17)}$$

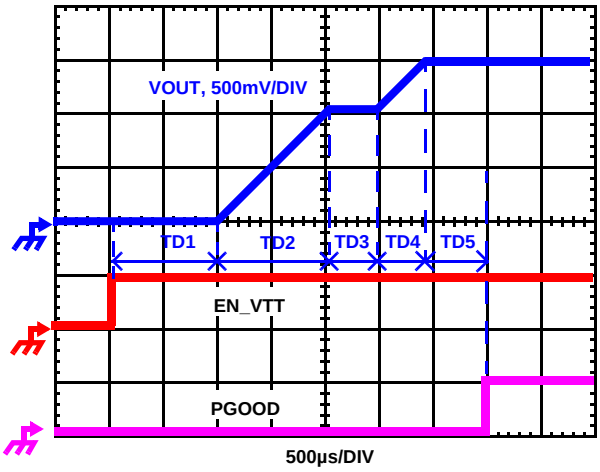


FIGURE 11. INTEL SOFT-START WAVEFORMS

TD1 is a fixed delay with the typical value as 1.40ms. TD3 is determined by the fixed 85µs plus the time to obtain valid VID voltage. If the VID is valid before the output reaches the 1.1V, the minimum time to validate the VID input is 500ns. Therefore the minimum TD3 is about 86µs.

During TD2 and TD4, ISL6322 digitally controls the DAC voltage change at 6.25mV per step. The time for each step is determined by the frequency of the soft-start oscillator which is defined by the resistor R_{SS} from SS pin to GND. The second soft-start ramp time TD2 and TD4 can be calculated based on the following equations:

$$TD2 = \frac{1.1 \cdot R_{SS}}{6.25 \cdot 25}(\mu s) \quad \text{(EQ. 18)}$$

$$TD4 = \frac{\left|(V_{VID} - 1.1)\right| \cdot R_{SS}}{6.25 \cdot 25}(\mu s) \quad \text{(EQ. 19)}$$

For example, when VID is set to 1.5V and the R_{SS} is set at 100kΩ, the first soft-start ramp time TD2 will be 704µs and the second soft-start ramp time TD4 will be 256µs.

NOTE: If the SS pin is grounded, the soft-start ramp in TD2 and TD4 will be defaulted to a 6.25mV step frequency of 330kHz.

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay TD5. The typical value for TD5 is 440µs.

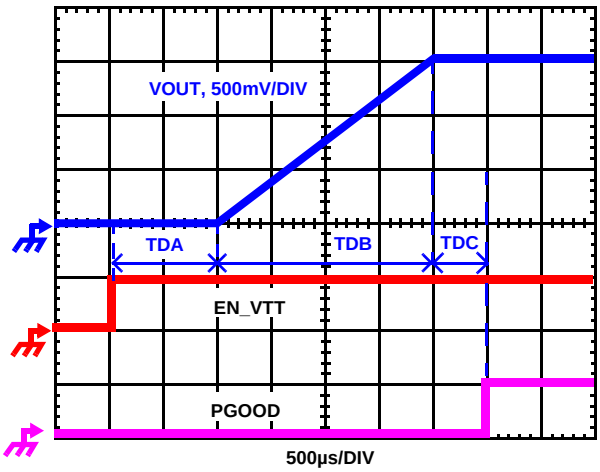


FIGURE 12. AMD SOFT-START WAVEFORMS

AMD Soft-Start

For the AMD 5-bit and 6-bit modes of operation, the soft-start sequence is composed of three periods, as shown in Figure 12. At the beginning of soft-start, the VID code is immediately obtained from the VID pins, followed by a fixed delay period TDA. After this delay period the ISL6322 will begin ramping the output voltage to the desired DAC level at a fixed rate of 6.25mV per step, with a stepping frequency of 330kHz. The amount of time required to ramp the output voltage to the final DAC voltage is referred to as TDB, and can be calculated as shown in Equation 20.

$$TDB = \frac{1}{330 \times 10^3} \cdot \left(\frac{V_{VID}}{0.00625}\right) \quad \text{(EQ. 20)}$$

After the DAC voltage reaches the final VID setting, PGOOD will be set to high with the fixed delay TDC. The typical value for TDC can range between 1.5ms and 3.0ms.

Pre-Biased Soft-Start

The ISL6322 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

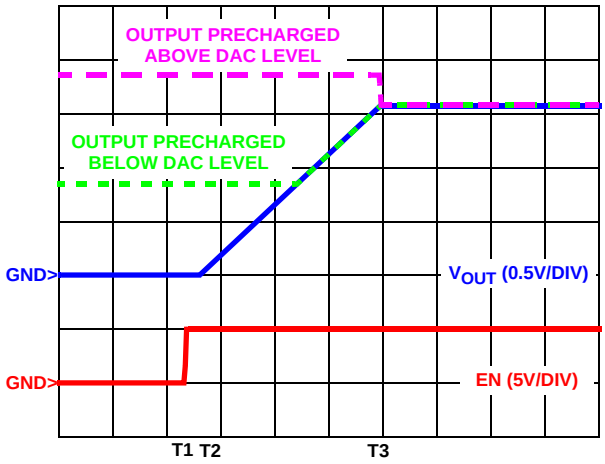


FIGURE 13. SOFT-START WAVEFORMS FOR ISL6322-BASED MULTIPHASE CONVERTER

Fault Monitoring and Protection

The ISL6322 actively monitors output voltage and current to detect fault conditions. Fault monitors trigger protective measures to prevent damage to a microprocessor load. One common power good indicator is provided for linking to external system monitors. The schematic in Figure 14 outlines the interaction between the fault monitors and the power good signal.

Power Good Signal

The power good pin (PGOOD) is an open-drain logic output that signals whether or not the ISL6322 is regulating the output voltage within the proper levels, and whether any fault conditions exist. This pin should be tied to a +5V source through a resistor.

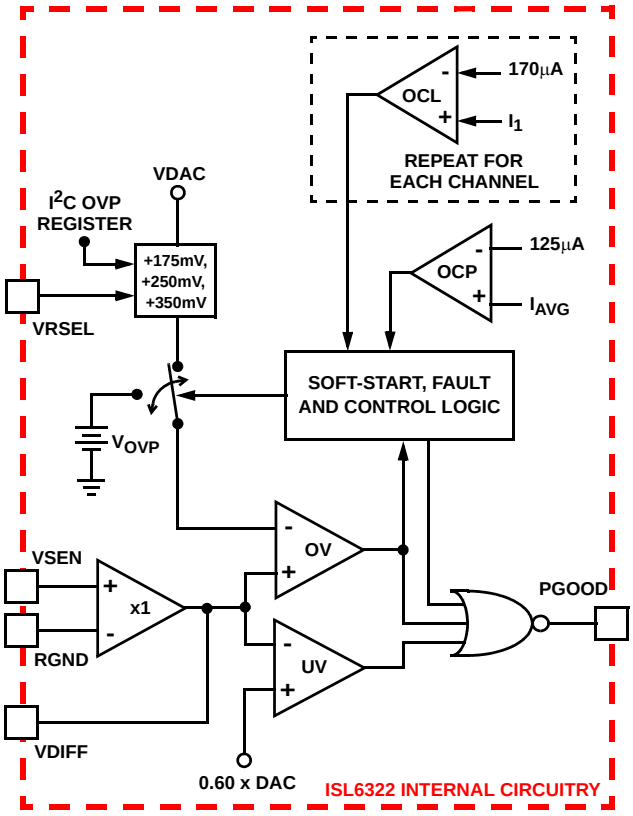


FIGURE 14. POWER GOOD AND PROTECTION CIRCUITRY

During shutdown and soft-start PGOOD pulls low and releases high after a successful soft-start and the output voltage is operating between the undervoltage and overvoltage limits. PGOOD transitions low when an undervoltage, overvoltage, or overcurrent condition is detected or when the controller is disabled by a reset from EN, EN_PH4, POR, or one of the no-CPU VID codes. In the event of an overvoltage or overcurrent condition, the controller latches off and PGOOD will not return high until after a successful soft-start. In the case of an undervoltage event, PGOOD will return high when the output voltage returns to within the undervoltage.

Undervoltage Detection

The undervoltage threshold is set at 60% of the VID code. When the output voltage (VSEN-RGND) is below the undervoltage threshold, PGOOD gets pulled low. No other action is taken by the controller. PGOOD will return high if the output voltage rises above 70% of the VID code.

Overvoltage Protection

The ISL6322 constantly monitors the sensed output voltage on the VDIFF pin to detect if an overvoltage event occurs. When the output voltage rises above the OVP trip level actions are taken by the ISL6322 to protect the microprocessor load. The overvoltage protection trip level changes depending on what mode of operation the controller is in and what state the I^2C registers and the VRSEL pin are

in. Table 6 and 7 below list what the OVP trip levels are under all conditions (see pages 27 through 31 for details of controlling OVP thresholds with I^2C).

At the inception of an overvoltage event, LGATE1, LGATE2 and LGATE3 are commanded high, PWM4 is commanded low, and the PGOOD signal is driven low. This turns on the all of the lower MOSFETs and pulls the output voltage below a level that might cause damage to the load. The LGATE outputs remain high and PWM4 remains low until VDIFF falls 100mV below the OVP threshold that tripped the overvoltage protection circuitry. The ISL6322 will continue to protect the load in this fashion as long as the overvoltage condition recurs.

Once an overvoltage condition ends, the ISL6322 latches off and must be reset by toggling EN, or through POR, before a soft-start can be re-initiated.

TABLE 6. INTEL VR10 AND VR11 OVP THRESHOLDS

MODE OF OPERATION	DEFAULT	ALTERNATE
Soft-Start (TD1 and TD2)	1.280V and VDAC+250mV (higher of the two)	1.280V and VDAC+175mV (higher of the two)
Soft-Start (TD3 and TD4)	VDAC+250mV	VDAC+175mV
Normal Operation	VDAC+250mV	VDAC+175mV

TABLE 7. AMD OVP THRESHOLDS

MODE OF OPERATION	DEFAULT	ALTERNATE
Soft-Start	2.200V and VDAC+250mV (higher of the two)	2.200V and VDAC+175mV (higher of the two)
Normal Operation	VDAC+250mV	VDAC+175mV

One exception that overrides the overvoltage protection circuitry is a dynamic VID transition in AMD modes of operation. If a new VID code is detected during normal operation, the OVP protection circuitry is disabled from the beginning of the dynamic VID transition, until 50µs after the internal DAC reaches the final VID setting. This is the only time during operation of the ISL6322 that the OVP circuitry is not active.

Pre-POR Overvoltage Protection

Prior to PVCC and VCC exceeding their POR levels, the ISL6322 is designed to protect the load from any overvoltage events that may occur. This is accomplished by means of an internal 10kΩ resistor tied from PHASE to LGATE, which turns on the lower MOSFET to control the output voltage until the overvoltage event ceases or the input power supply cuts off. For complete protection, the low side MOSFET should have a gate threshold well below the maximum voltage rating of the load/microprocessor.

In the event that during normal operation the PVCC or VCC voltage falls back below the POR threshold, the pre-POR overvoltage protection circuitry reactivates to protect from any more pre-POR overvoltage events.

Open Sense Line Protection

In the case that either of the remote sense lines, VSEN or GND, become open, the ISL6322 is designed to detect this and shut down the controller. This event is detected by monitoring small currents that are fed out the VDIFF and RGND pins. In the event of an open sense line fault, the controller will continue to remain off until the fault goes away, at which point the controller will re-initiate a soft-start sequence.

Overcurrent Protection

The ISL6322 takes advantage of the proportionality between the load current and the average current, I_{AVG}, to detect an overcurrent condition. See “Continuous Current Sampling” on page 13 for more detail on how the average current is measured. The average current is continually compared with a constant 125µA OCP reference current as shown in Figure 14. Once the average current exceeds the OCP reference current, a comparator triggers the converter to begin overcurrent protection procedures.

This method for detecting overcurrent events limits the minimum overcurrent trip threshold because of the fact the ISL6322 uses set internal R_{ISEN} current sense resistors. The minimum overcurrent trip threshold is dictated by the DCR of the inductors and the number of active channels. To calculate the minimum overcurrent trip level, $I_{OCP,min}$, use Equation 21, where N is the number of active channels, DCR is the individual inductor’s DCR, and R_{ISEN} is the 300Ω internal current sense resistor. If the desired overcurrent trip

$$I_{OCP,\,min} = \frac{125 \cdot 10^{-6} \cdot R_{ISEN} \cdot N}{DCR} \quad \text{(EQ. 21)}$$

level is greater then the minimum overcurrent trip level, $I_{OCP,min}$, then the resistor divider R-C circuit around the inductor shown in Figure 5 should be used to set the desired trip level.

$$I_{OCP} = \left(\frac{125 \cdot 10^{-6} \cdot R_{ISEN} \cdot N}{DCR}\right) \cdot \left(\frac{R_1 + R_2}{R_2}\right) \quad \text{(EQ. 22)}$$

$$I_{OCP} > I_{OCP,\,min}$$

The overcurrent trip level of the ISL6322 cannot be set any lower than the $I_{OCP,min}$ level calculated above.

At the beginning of overcurrent shutdown, the controller sets all of the UGATE and LGATE signals low, puts PWM4 in a high-impedance state, and forces PGOOD low. This turns off all of the upper and lower MOSFETs. The system remains in this state for a fixed period of 12ms. If the controller is still enabled at the end of this wait period, it will attempt a soft-start. If the fault remains, the trip-retry cycles will

continue indefinitely until either the controller is disabled or the fault is cleared. Note that the energy delivered during trip-retry cycling is much less than during full-load operation, so there is no thermal hazard.

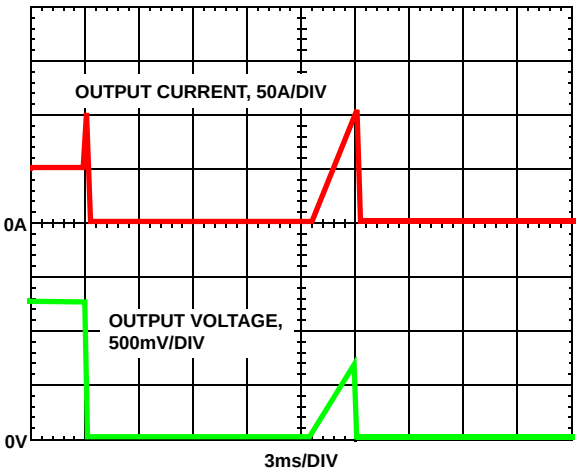


FIGURE 15. OVERCURRENT BEHAVIOR IN HICCUP MODE

Individual Channel Overcurrent Limiting

The ISL6322 has the ability to limit the current in each individual channel without shutting down the entire regulator. This is accomplished by continuously comparing the sensed currents of each channel with a constant 170µA OCL reference current as shown in Figure 14. If a channel's individual sensed current exceeds this OCL limit, the UGATE signal of that channel is immediately forced low, and the LGATE signal is forced high. This turns off the upper MOSFET(s), turns on the lower MOSFET(s), and stops the rise of current in that channel, forcing the current in the channel to decrease. That channel's UGATE signal will not be able to return high until the sensed channel current falls back below the 170µA reference.

I²C Bus Interface

The ISL6322 includes an I²C bus interface which allows for user programmability of four of the controller's operating parameters. The operating parameters that can be adjusted through the I²C are:

1. **Voltage Margining Offset**: The output voltage can be positively offset up to +787.5mV in 12.5mV increments.
2. **Adaptive Deadtime Control**: Selects between LGATE Detect and PHASE Detect deadtime control schemes as described in the *User Selectable Adaptive Deadtime Control Techniques* section.
3. **Overvoltage Trip Level**: Selects the overvoltage protection trip threshold as described in the *Overvoltage Protection* section.
4. **Switching Frequency:** The switching frequency can be increased by a fixed +15% or +30%, or can be decreased by -15% or -30%.

To adjust these four parameters, data transmission from the main microprocessor to the ISL6322 and vice versa must take place through the two wire I²C bus interface. The two wires of the I²C bus consist of the SDA line, over which all data is sent, and the SCL line, which is a clock signal used to synchronize sending/receiving of the data.

Both SDA and SCL are bidirectional lines, externally connected to a positive supply voltage via a pull-up resistor. Pull-up resistor values should be chosen to limit the input current to less then 3mA. When the bus is free, both lines are HIGH. The output stages of ISL6322 have an open drain/open collector in order to perform the wired-AND function. Data on the I²C bus can be transferred up to 100Kbps in the standard-mode or up to 400Kbps in the fast-mode. The level of logic "0" and logic "1" is dependent on associated value of V_{DD} as per electrical specification table. One clock pulse is generated for each data bit transferred. The ISL6322 is a "SLAVE only" device, so the SCL line must always be controlled by an external master.

It is important to note that the I²C interface of the ISL6322 only works once the voltage on the VCC pin has risen above the POR rising threshold. The I²C will continue to remain active until the voltage on the VCC pin falls back below the falling POR threshold level.

Data Validity

The data on the SDA line must be stable during the HIGH period of the SCL, unless generating a START or STOP condition. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. Refer to Figure 16.

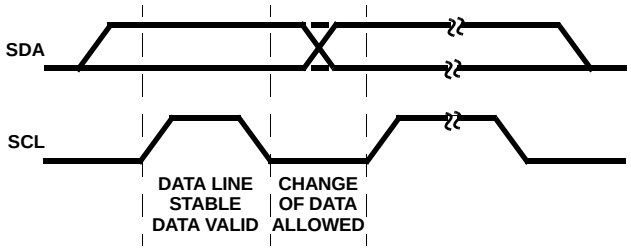


FIGURE 16. DATA VALIDITY

START and STOP Conditions

As shown in Figure 17, a START (S) condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.

The STOP (P) condition is a LOW to HIGH transition on the SDA line while SCL is HIGH. A STOP condition must be sent before each START condition.

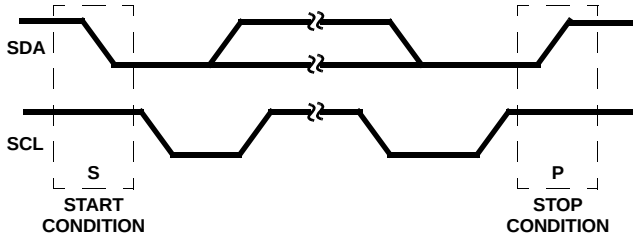


FIGURE 17. START AND STOP WAVEFORMS

Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB) and the least significant bit last (LSB).

Acknowledge

Each address and data transmission uses 9 clock pulses. The ninth pulse is the acknowledge bit (A). After the start condition, the master sends 7 slave address bits and a R/W bit during the next 8 clock pulses. During the ninth clock pulse, the device that recognizes its own address holds the data line low to acknowledge. The acknowledge bit is also used by both the master and the slave to acknowledge receipt of register addresses and data as described below.

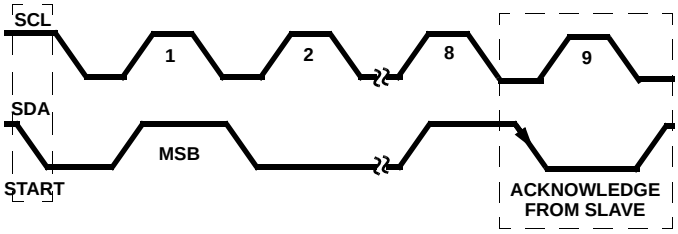


FIGURE 18. ACKNOWLEDGE ON THE I^2C BUS

ISL6322 I^2C Slave Address

All devices on the I^2C bus must have a 7-bit I^2C address in order to be recognized. The ISL6322 has two user selectable addresses to ensure it does not interfere with other devices on the bus. The address is programmed via the R_{SS} resistor on the SS/RST/A0 pin. Placing the R_{SS} resistor from the SS/RST/A0 pin to ground sets the I^2C address to be 1000_110. If the R_{SS} resistor is placed from the SS/RST/A0 pin to VCC the address is 1000_111.

Please note that the I^2C address of the ISL6322 is programmed from the SS/RST/A0 pin as soon as VCC rises above the POR threshold. The ISL6322's I^2C address stays the same and can not be reprogrammed until VCC falls back below the POR falling threshold.

Communicating Over the I^2C Bus

Two transactions are supported on the I^2C interface: 1) Write register, 2) Read register from current address.

All transactions start with a control byte sent from the I^2C master device. The control byte begins with a Start condition, followed by 7-bits of slave address. The last bit sent by the master is the R/W bit and is 0 for a write or 1 for a read. If any slaves on the I^2C bus recognize their address, they will Acknowledge by pulling the serial data line low for the last clock cycle in the control byte. If no slaves exist at that address or are not ready to communicate, the data line will be 1, indicating a Not Acknowledge condition.

Once the control byte is sent, and the ISL6322 acknowledges it, the 2nd byte sent by the master must be a register address byte. This register address byte tells the ISL6322 which one of the two internal registers it wants to write to or read from. The address of the first internal register, RGS1, is 0000_0000. This register sets the Voltage Margining Offset. The address of the second internal register, RGS2, is 0000_0001. This register sets the Adaptive Deadtime Control, Overvoltage Protection, and Switching Frequency parameters. Once the ISL6322 receives a correct register address byte, it responds with an acknowledge.

Writing to the Internal Registers

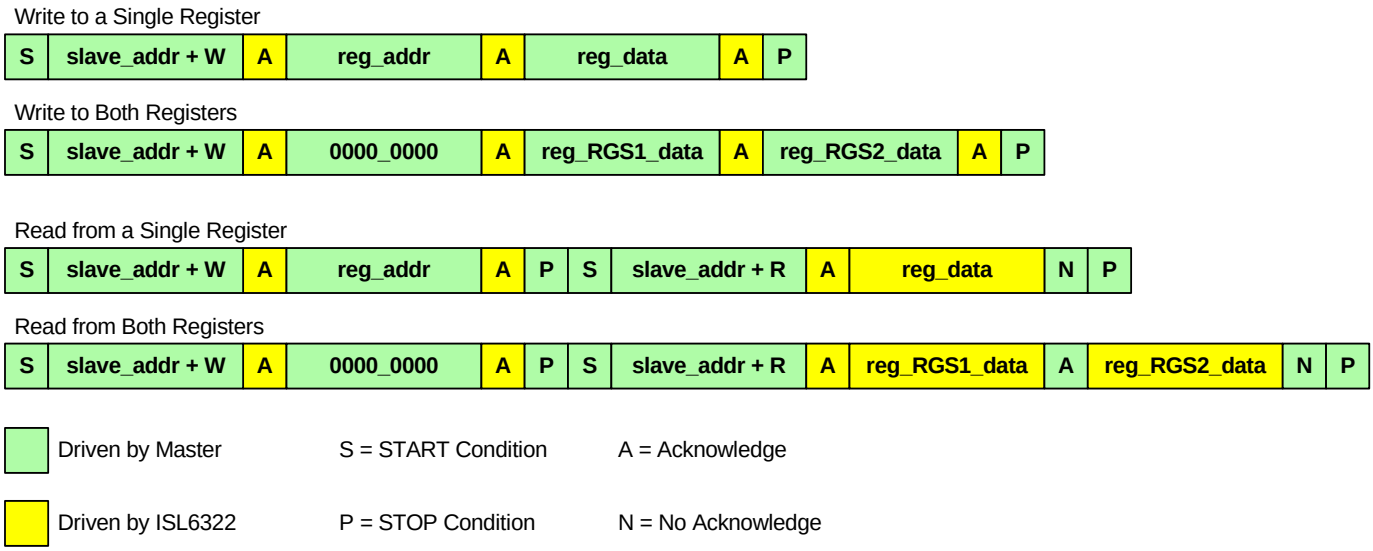
In order to change any of the four operating parameters via the I^2C bus, the internal registers must be written to. The two registers inside the ISL6322 can be written individually with two separate write transactions or sequentially with one write transaction by sending two data bytes as described below.

To write to a single register in the ISL6322, the master sends a control byte with the R/W bit set to 0, indicating a write. If it receives an Acknowledge from the ISL6322, it sends a register address byte representing the internal register it wants to write to (0000_0000 for RGS1 or 0000_0001 for RGS2). The ISL6322 will respond with an Acknowledge. The master then sends a byte representing the data byte to be written into the desired register. The ISL6322 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL6322 that the current transaction is complete. Once this transaction completes, the ISL6322 will immediately update and change the operating parameters on-the-fly.

It is also possible to write to both registers sequentially. To do this the master must write to register RGS1 first. This transaction begins with the master sending a control byte with the R/W bit set to 0. If it receives an Acknowledge from the ISL6322, it sends the register address byte 0000_0000, representing the internal register RGS1. The ISL6322 will respond with an Acknowledge. After sending the data byte to

RGS1 and receiving an Acknowledge from the ISL6322, instead of sending a Stop condition, the master sends the data byte to be stored in register RGS2. The ISL6322 will respond with an Acknowledge. The master then issues a Stop condition, indicating to the ISL6322 that the current transaction is complete. Once this transaction completes the ISL6322 will immediately update and change the operating parameters on-the-fly.

I^2C Read and Write Protocol



Reading from the Internal Registers

The ISL6322 has the ability to read from both registers separately or read from them consecutively. Prior to reading from an internal register, the master must first select the desired register by writing to it and sending the register's address byte. This process begins by the master sending a control byte with the R/W bit set to 0, indicating a write. Once it receives an Acknowledge from the ISL6322, it sends a register address byte representing the internal register it wants to read from (0000_0000 for RGS1 or 0000_0001 for RGS2). The ISL6322 will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition, the master follows with a new Start condition, and then sends a new control byte with the R/W bit set to 1, indicating a read. The ISL6322 will then respond by sending the master an Acknowledge, followed by the data byte stored in that register. The master must then send a Not Acknowledge followed by a Stop command, which will complete the read transaction.

It is also possible for both registers to be read consecutively. To do this the master must read from register RGS1 first. This transaction begins with the master sending a control byte with the R/W bit set to 0. If it receives an Acknowledge from the ISL6322, it sends the register address byte 0000_0000, representing the internal register RGS1. The ISL6322 will respond with an Acknowledge. The master must then respond with a Stop condition. After the Stop condition the master follows with a new Start condition, and then sends a new control byte with the R/W bit set to 1, indicating a read. The ISL6322 will then respond by sending the master an Acknowledge, followed by the data byte stored in register RGS. The master must then send an Acknowledge, and after doing so, the ISL6322 will respond by sending the data byte stored in register RGS2. The master must then send a Not Acknowledge followed by a Stop command, which will complete the read transaction.

Resetting the Internal Registers

The ISL6322's two internal I^2C registers always initialize to 0000_0000 when the controller first receives power. Once the voltage on the VCC pin rises above the POR rising threshold level, these registers can be changed at any time via the I^2C interface. If the voltage on the VCC pin falls below the POR falling threshold, the internal registers are automatically reset to 0000_0000.

It is possible to reset the internal registers without powering down the controller and without requiring the controller to stop regulating and soft-start again. This can be done by one of two methods. The first method is to simply write to the internal registers over the I^2C interface to be 0000_0000. The other method is pull the voltage on the SS/RST/A0 pin down below 0.4V. This will immediately reset the internal registers to 0000_0000 and will not stop the controller from regulating the output voltage or cause soft-start to recycle.

TABLE 8. REGISTER RGS1 (VOLTAGE MARGINING OFFSET)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Voffset (mV)
X	X	VO5	VO4	VO3	VO2	VO1	VO0	
x	x	0	0	0	0	0	0	0.0
x	x	0	0	0	0	0	1	12.5
x	x	0	0	0	0	1	0	25.0
x	x	0	0	0	0	1	1	37.5
x	x	0	0	0	1	0	0	50.00
x	x	0	0	0	1	0	1	62.5
x	x	0	0	0	1	1	0	75.0
x	x	0	0	0	1	1	1	87.5
x	x	0	0	1	0	0	0	100.0
x	x	0	0	1	0	0	1	112.5
x	x	0	0	1	0	1	0	125.0
x	x	0	0	1	0	1	1	137.5
x	x	0	0	1	1	0	0	150.0
x	x	0	0	1	1	0	1	162.5
x	x	0	0	1	1	1	0	175.0
x	x	0	0	1	1	1	1	187.5
x	x	0	1	0	0	0	0	200.00
x	x	0	1	0	0	0	1	212.5
x	x	0	1	0	0	1	0	225.0
x	x	0	1	0	0	1	1	237.5
x	x	0	1	0	1	0	0	250.0
x	x	0	1	0	1	0	1	262.5
x	x	0	1	0	1	1	0	275.0
x	x	0	1	0	1	1	1	287.5
x	x	0	1	1	0	0	0	300.0
x	x	0	1	1	0	0	1	312.5
x	x	0	1	1	0	1	0	325.0
x	x	0	1	1	0	1	1	337.5
x	x	0	1	1	1	0	0	350.0
x	x	0	1	1	1	0	1	362.5
x	x	0	1	1	1	1	0	375.0
x	x	0	1	1	1	1	1	387.5
x	x	1	0	0	0	0	0	400.0
x	x	1	0	0	0	0	1	412.5
x	x	1	0	0	0	1	0	425.0
x	x	1	0	0	0	1	1	437.5
x	x	1	0	0	1	0	0	450.0
x	x	1	0	0	1	0	1	462.5

TABLE 8. REGISTER RGS1 (VOLTAGE MARGINING OFFSET) (Continued)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	Voffset (mV)
X	X	VO5	VO4	VO3	VO2	VO1	VO0	
x	x	1	0	0	1	1	0	475.0
x	x	1	0	0	1	1	1	487.5
x	x	1	0	1	0	0	0	500.0
x	x	1	0	1	0	0	1	512.5
x	x	1	0	1	0	1	0	525.0
x	x	1	0	1	0	1	1	537.5
x	x	1	0	1	1	0	0	550.0
x	x	1	0	1	1	0	1	562.5
x	x	1	0	1	1	1	0	575.0
x	x	1	0	1	1	1	1	587.5
x	x	1	1	0	0	0	0	600.0
x	x	1	1	0	0	0	1	612.5
x	x	1	1	0	0	1	0	625.0
x	x	1	1	0	0	1	1	637.5
x	x	1	1	0	1	0	0	650.0
x	x	1	1	0	1	0	1	662.5
x	x	1	1	0	1	1	0	675.0
x	x	1	1	0	1	1	1	687.5
x	x	1	1	1	0	0	0	700.0
x	x	1	1	1	0	0	1	712.5
x	x	1	1	1	0	1	0	725.0
x	x	1	1	1	0	1	1	737.5
x	x	1	1	1	1	0	0	750.0
x	x	1	1	1	1	0	1	762.5
x	x	1	1	1	1	1	0	775.0
x	x	1	1	1	1	1	1	787.5

TABLE 9. REGISTER RGS2 (ADAPTIVE DEADTIME CONTROL/OVERVOLTAGE PROTECTION/SWITCHING FREQUENCY)

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	ADAPTIVE DEADTIME CONTROL	OVERVOLTAGE PROTECTION LEVEL	SWITCHING FREQUENCY
X	X	DT1	DT0	OVP	FS2	FS1	FS0			
x	x	0	0	0	0	0	0	PHASE DETECT	DEFAULT	NOMINAL
x	x	0	0	0	0	0	1	PHASE DETECT	DEFAULT	-15%
x	x	0	0	0	0	1	0	PHASE DETECT	DEFAULT	-30%
x	x	0	0	0	0	1	1	PHASE DETECT	DEFAULT	+15%
x	x	0	0	0	1	0	0	PHASE DETECT	DEFAULT	+30%
x	x	0	0	1	0	0	0	PHASE DETECT	ALTERNATE	NOMINAL
x	x	0	0	1	0	0	1	PHASE DETECT	ALTERNATE	-15%
x	x	0	0	1	0	1	0	PHASE DETECT	ALTERNATE	-30%
x	x	0	0	1	0	1	1	PHASE DETECT	ALTERNATE	+15%
x	x	0	0	1	1	0	0	PHASE DETECT	ALTERNATE	+30%
x	x	0	1	0	0	0	0	LGATE DETECT	DEFAULT	NOMINAL
x	x	0	1	0	0	0	1	LGATE DETECT	DEFAULT	-15%
x	x	0	1	0	0	1	0	LGATE DETECT	DEFAULT	-30%
x	x	0	1	0	0	1	1	LGATE DETECT	DEFAULT	+15%
x	x	0	1	0	1	0	0	LGATE DETECT	DEFAULT	+30%
x	x	0	1	1	0	0	0	LGATE DETECT	ALTERNATE	NOMINAL
x	x	0	1	1	0	0	1	LGATE DETECT	ALTERNATE	-15%
x	x	0	1	1	0	1	0	LGATE DETECT	ALTERNATE	-30%
x	x	0	1	1	0	1	1	LGATE DETECT	ALTERNATE	+15%
x	x	0	1	1	1	0	0	LGATE DETECT	ALTERNATE	+30%

NOTE: It is recommended that frequency shifts occur in 15% increments only.

General Design Guide

This section is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

Power Stages

The first step in designing a multiphase converter is to determine the number of phases. This determination depends heavily on the cost analysis, which in turn depends on system constraints that differ from one design to the next. Principally, the designer will be concerned with whether components can be mounted on both sides of the circuit board, whether through-hole components are permitted, the total board space available for power-supply circuitry, and the maximum amount of load current. Generally speaking, the most economical solutions are those in which each phase handles between 25A and 30A. All surface-mount designs will tend toward the lower end of this current range. If through-hole MOSFETs and inductors can be used, higher per-phase currents are possible. In cases where board space is the limiting constraint, current can be pushed as high as 40A per phase, but these designs require heat sinks and forced air to cool the MOSFETs, inductors and heat-dissipating surfaces.

MOSFETS

The choice of MOSFETs depends on the current each MOSFET will be required to conduct, the switching frequency, the capability of the MOSFETs to dissipate heat, and the availability and nature of heat sinking and air flow.

LOWER MOSFET POWER CALCULATION

The calculation for power loss in the lower MOSFET is simple, since virtually all of the loss in the lower MOSFET is due to current conducted through the channel resistance ($r_{DS(ON)}$). In Equation 23, I_M is the maximum continuous output current, I_{PP} is the peak-to-peak inductor current (see Equation 1), and d is the duty cycle (V_{OUT}/V_{IN}).

$$P_{LOW,1} = r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N} \right)^2 \cdot (1-d) + \frac{I_{L,PP}^2 \cdot (1-d)}{12} \right] \quad \text{(EQ. 23)}$$

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$, the switching frequency, f_S, and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval respectively.

$$P_{LOW,2} = V_{D(ON)} \cdot f_S \cdot \left[\left(\frac{I_M}{N} + \frac{I_{PP}}{2} \right) \cdot t_{d1} + \left(\frac{I_M}{N} - \frac{I_{PP}}{2} \right) \cdot t_{d2} \right] \quad \text{(EQ. 24)}$$

The total maximum power dissipated in each lower MOSFET is approximated by the summation of $P_{LOW,1}$ and $P_{LOW,2}$.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are due to currents conducted across the input voltage (V_{IN}) during switching. Since a substantially higher portion of the upper-MOSFET losses are dependent on switching frequency, the power calculation is more complex. Upper MOSFET losses can be divided into separate components involving the upper-MOSFET switching times, the lower-MOSFET body-diode reverse-recovery charge, Q_{rr}, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

When the upper MOSFET turns off, the lower MOSFET does not conduct any portion of the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting, the current in the upper MOSFET falls to zero as the current in the lower MOSFET ramps up to assume the full inductor current. In Equation 25, the required time for this commutation is t_1 and the approximated associated power loss is $P_{UP,1}$.

$$P_{UP,1} \approx V_{IN} \cdot \left(\frac{I_M}{N} + \frac{I_{PP}}{2} \right) \cdot \left(\frac{t_1}{2} \right) \cdot f_S \quad \text{(EQ. 25)}$$

At turn on, the upper MOSFET begins to conduct and this transition occurs over a time t_2. In Equation 26, the approximate power loss is $P_{UP,2}$.

$$P_{UP,2} \approx V_{IN} \cdot \left(\frac{I_M}{N} - \frac{I_{PP}}{2} \right) \cdot \left(\frac{t_2}{2} \right) \cdot f_S \quad \text{(EQ. 26)}$$

A third component involves the lower MOSFET reverse-recovery charge, Q_{rr}. Since the inductor current has fully commutated to the upper MOSFET before the lower-MOSFET body diode can recover all of Q_{rr}, it is conducted through the upper MOSFET across VIN. The power dissipated as a result is $P_{UP,3}$.

$$P_{UP,3} = V_{IN} \cdot Q_{rr} \cdot f_S \quad \text{(EQ. 27)}$$

Finally, the resistive part of the upper MOSFET is given in Equation 28 as $P_{UP,4}$.

$$P_{UP,4} \approx r_{DS(ON)} \cdot \left[\left(\frac{I_M}{N} \right)^2 \cdot d + \frac{I_{PP}^2}{12} \right] \quad \text{(EQ. 28)}$$

The total power dissipated by the upper MOSFET at full load can now be approximated as the summation of the results from Equations 25, 26, 27 and 28. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process involving repetitive solutions to the loss equations for different MOSFETs and different switching frequencies.

Package Power Dissipation

When choosing MOSFETs it is important to consider the amount of power being dissipated in the integrated drivers located in the controller. Since there are a total of three drivers in the controller package, the total power dissipated by all three drivers must be less than the maximum allowable power dissipation for the QFN package.

Calculating the power dissipation in the drivers for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of 125°C. The maximum allowable IC power dissipation for the 7x7 QFN package is approximately 3.5W at room temperature. See *Layout Considerations* paragraph for thermal transfer improvement suggestions.

When designing the ISL6322 into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses, P_{Qg_TOT}, due to the gate charge of MOSFETs and the integrated driver's internal circuitry and their corresponding average driver current can be estimated with Equations 29 and 30, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \cdot VCC \quad \text{(EQ. 29)}$$

$$P_{Qg\_Q1} = \frac{3}{2} \cdot Q_{G1} \cdot PVCC \cdot F_{SW} \cdot N_{Q1} \cdot N_{PHASE}$$

$$P_{Qg\_Q2} = Q_{G2} \cdot PVCC \cdot F_{SW} \cdot N_{Q2} \cdot N_{PHASE}$$

$$I_{DR} = \left(\frac{3}{2} \cdot Q_{G1} \cdot N_{Q1} + Q_{G2} \cdot N_{Q2} \right) \cdot N_{PHASE} \cdot F_{SW} + I_Q \quad \text{(EQ. 30)}$$

In Equations 29 and 30, P_{Qg_Q1} is the total upper gate drive power loss and P_{Qg_Q2} is the total lower gate drive power loss; the gate charge (Q_{G1} and Q_{G2}) is defined at the particular gate to source drive voltage PVCC in the corresponding MOSFET data sheet; I_Q is the driver total

quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are the number of upper and lower MOSFETs per phase, respectively; N_{PHASE} is the number of active phases. The I_Q*VCC product is the quiescent power of the controller without capacitive load and is typically 75mW at 300kHz.

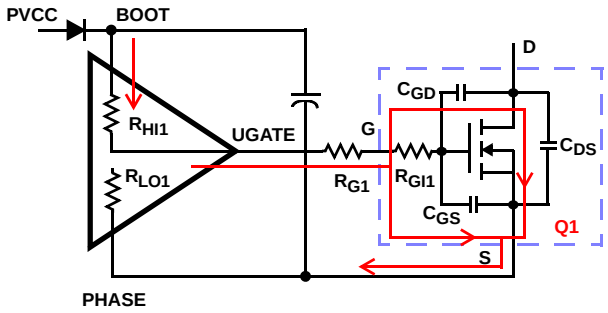


FIGURE 19. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

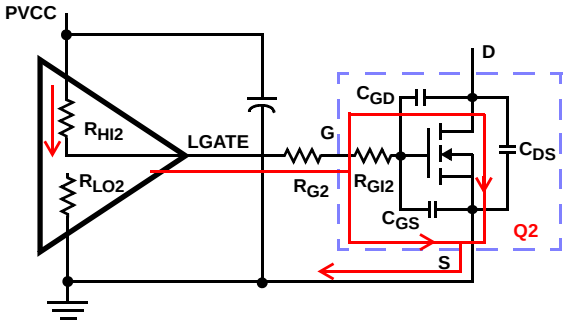


FIGURE 20. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

The total gate drive power losses are dissipated among the resistive components along the transition path and in the bootstrap diode. The portion of the total power dissipated in the controller itself is the power dissipated in the upper drive path resistance, P_{DR_UP}, the lower drive path resistance, P_{DR_UP}, and in the boot strap diode, P_{BOOT}. The rest of the

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + P_{BOOT} + (I_Q \cdot VCC) \quad \text{(EQ. 31)}$$

$$P_{BOOT} = \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \cdot \frac{P_{Qg\_Q1}}{3}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \cdot \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

power will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of the MOSFETs. Figures 19 and 20 show the typical upper and lower gate drives turn-on transition path. The total power dissipation in the controller itself, P_{DR}, can be roughly estimated with Equation 31.

Inductor DCR Current Sensing Component Selection

The ISL6322 senses each individual channel's inductor current by detecting the voltage across the output inductor DCR of that channel (as described in "Continuous Current Sampling" on page 13). As Figure 21 illustrates, an R-C network is required to accurately sense the inductor DCR voltage and convert this information into a current, which is proportional to the total output current. The time constant of this R-C network must match the time constant of the inductor L/DCR.

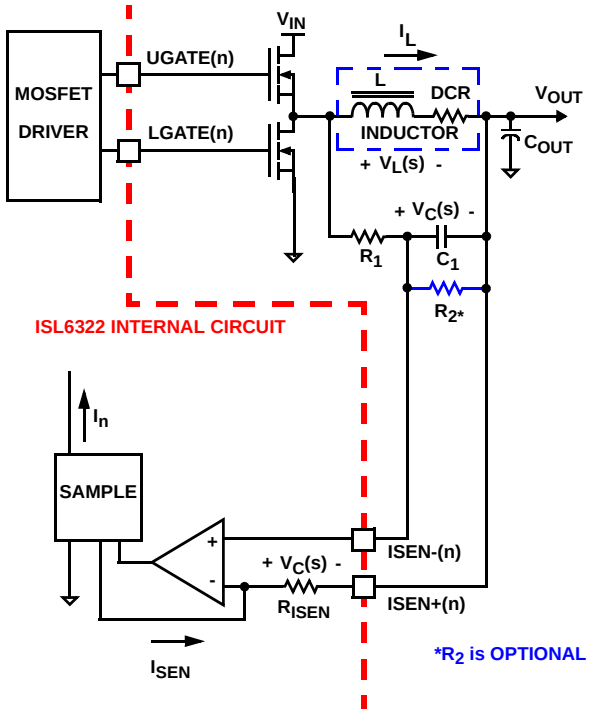


FIGURE 21. DCR SENSING CONFIGURATION

The R-C network across the inductor also sets the overcurrent trip threshold for the regulator. Before the R-C components can be selected, the desired overcurrent protection level should be chosen. The minimum overcurrent trip threshold the controller can support is dictated by the DCR of the inductors and the number of active channels. To calculate the minimum overcurrent trip level, $I_{OCP,min}$, use Equation 32, where N is the number of active channels, and DCR is the individual inductor's DCR.

$$I_{OCP,\,min} = \frac{0.0375 \cdot N}{DCR} \quad \text{(EQ. 32)}$$

The overcurrent trip level of the ISL6322 cannot be set any lower then the $I_{OCP,min}$ level calculated above. **If the minimum overcurrent trip level is desired, do the**

following steps to choose the component values for the R-C current sensing network:

1. Choose an arbitrary value for C_1. The recommended value is 0.1µF.
2. Plug the inductor L and DCR component values, and the value for C_1 chosen in step 1, into Equation 33 to calculate the value for R_1.

$$R_1 = \frac{L}{DCR \cdot C_1} \qquad I_{OCP} = I_{OCP,min} \qquad \text{(EQ. 33)}$$

3. Resistor R_2 should be left unpopulated.

If the desired overcurrent trip level, I_{OCP}, is greater than the minimum overcurrent trip level, $I_{OCP,min}$, then a resistor divider R-C circuit should be used to set the desired trip level. **Do the following steps to choose the component values for the resistor divider R-C current sensing network:**

1. Choose an arbitrary value for C_1. The recommended value is 0.1µF.
2. Plug the inductor L and DCR component values, the value for C_1 chosen in step 1, the number of active channels N, and the desired overcurrent protection level I_{OCP} into Equations 34 and 35 to calculate the values for R_1 and R_2.

$$R_1 = \frac{L \cdot I_{OCP}}{C_1 \cdot 0.0375 \cdot N} \qquad I_{OCP} > I_{OCP,min} \qquad \text{(EQ. 34)}$$

$$R_2 = \frac{L \cdot I_{OCP}}{C_1 \cdot (I_{OCP} \cdot DCR - 0.0375 \cdot N)} \qquad \text{(EQ. 35)}$$

Due to errors in the inductance or DCR, it may be necessary to adjust the value of R_1 and R_2 to match the time constants correctly. The effects of time constant mismatch can be seen in the form of droop overshoot or undershoot during the initial load transient spike, as shown in Figure 22. **Do the following steps to ensure the R-C and inductor L/DCR time constants are matched accurately**.

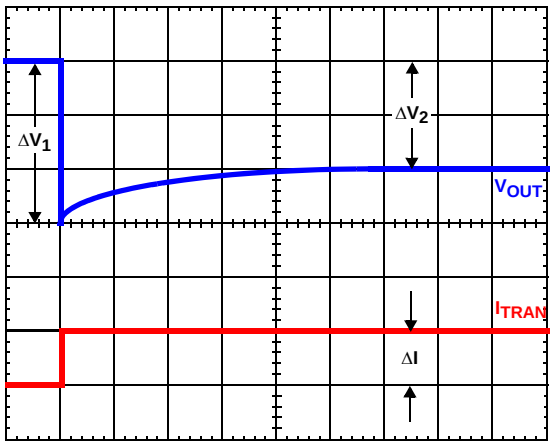


FIGURE 22. TIME CONSTANT MISMATCH BEHAVIOR

1. Capture a transient event with the oscilloscope set to about L/DCR/2 (sec/div). For example, with L = 1µH and DCR = 1mΩ, set the oscilloscope to 500µs/div.
2. Record ΔV1 and ΔV2 as shown in Figure 22.
3. Select new values, $R_{1,NEW}$ and $R_{2,NEW}$, for the time constant resistors based on the original values, $R_{1,OLD}$ and $R_{2,OLD}$, using Equation 36 and Equation 37.

$$R_{1,NEW} = R_{1,OLD} \cdot \frac{\Delta V_1}{\Delta V_2} \qquad \text{(EQ. 36)}$$

$$R_{2,NEW} = R_{2,OLD} \cdot \frac{\Delta V_1}{\Delta V_2} \qquad \text{(EQ. 37)}$$

4. Replace R_1 and R_2 with the new values and check to see that the error is corrected. Repeat the procedure if necessary.

Load-line Regulation Resistor

If load-line regulation is desired, the IDROOP pin should be shorted to the FB pin in order for the internal average sense current to flow out across the load-line regulation resistor, labeled R_{FB} in Figure 6. This resistor's value sets the desired load-line required for the application. The desired load-line, R_{LL}, can be calculated by Equation 38, where V_{DROOP} is the desired droop voltage at the full load current I_{FL}.

$$R_{LL} = \frac{V_{DROOP}}{I_{FL}} \qquad \text{(EQ. 38)}$$

Based on the desired load-line, the load-line regulation resistor, R_{FB}, can be calculated from Equation 39 or Equation 40, depending on the R-C current sense circuitry being employed. If a basic R-C sense circuit consisting of C1 and R1 is being used, use Equation 39. If a resistor divider R-C sense circuit consisting of R1, R2, and C1 is being used, use Equation 40.

$$R_{FB} = \frac{R_{LL} \cdot N \cdot 300}{DCR} \qquad \text{(EQ. 39)}$$

$$R_{FB} = \frac{R_{LL} \cdot N \cdot 300 \cdot (R_1 + R_2)}{DCR \cdot R_2} \qquad \text{(EQ. 40)}$$

In Equations 39 and 40:
R_{LL} is the load-line resistance,
N is the number of active channels,
DCR is the DCR of the individual output inductors, and
R1 and R2 are the current sense R-C resistors.

If no load-line regulation is required, the IDROOP pin should be left open and not connected to anything. To choose the value for R_{FB} in this situation, see "Compensation without Load-line Regulation" on page 35.

Compensation

The two opposing goals of compensating the voltage regulator are stability and speed. Depending on whether the regulator employs the optional load-line regulation as described in “Load-Line (Droop) Regulation” on page 20, there are two distinct methods for achieving these goals: “Compensation with Load-line Regulation” on page 35 and “Compensation without Load-line Regulation” on page 35.

Compensation with Load-line Regulation

The load-line regulated converter behaves in a similar manner to a peak current mode controller because the two poles at the output filter L-C resonant frequency split with the introduction of current information into the control loop. The final location of these poles is determined by the system function, the gain of the current signal, and the value of the compensation components, R_C and C_C.

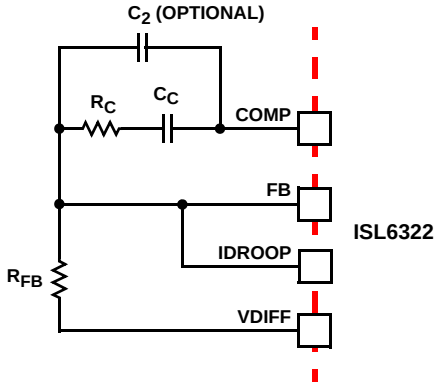


FIGURE 23. COMPENSATION CONFIGURATION FOR LOAD-LINE REGULATED ISL6322 CIRCUIT

Since the system poles and zero are affected by the values of the components that are meant to compensate them, the solution to the system equation becomes fairly complicated. Fortunately, there is a simple approximation that comes very close to an optimal solution. Treating the system as though it were a voltage-mode regulator, by compensating the L-C poles and the ESR zero of the voltage mode approximation, yields a solution that is always stable with very close to ideal transient performance.

Select a target bandwidth for the compensated system, f_0. The target bandwidth must be large enough to assure adequate transient performance, but smaller than 1/3 of the per-channel switching frequency. The values of the compensation components depend on the relationships of f_0 to the L-C pole frequency and the ESR zero frequency. For each of the following three, there is a separate set of equations for the compensation components.

In Equation 41:

- L is the per-channel filter inductance divided by the number of active channels,
- C is the sum total of all output capacitors,
- ESR is the equivalent series resistance of the bulk output filter capacitance, and
- V_{PP} is the peak-to-peak sawtooth signal amplitude as described in the *Electrical Specifications on page* 7.

Once selected, the compensation values in Equation 41 assure a stable converter with reasonable transient performance. In most cases, transient performance can be improved by making adjustments to R_C. Slowly increase the value of R_C while observing the transient performance on an oscilloscope until no further improvement is noted. Normally, C_C will not need adjustment. Keep the value of C_C from the case equations in Equation 41 unless some performance issue is noted.

Case 1: $\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} > f_0$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{pp}\cdot\sqrt{L\cdot C}}{0.66\cdot V_{IN}}$$

$$C_C = \frac{0.66\cdot V_{IN}}{2\cdot\pi\cdot V_{PP}\cdot R_{FB}\cdot f_0}$$

Case 2: $\frac{1}{2\cdot\pi\cdot\sqrt{L\cdot C}} \le f_0 < \frac{1}{2\cdot\pi\cdot C\cdot ESR}$

$$R_C = R_{FB}\cdot\frac{V_{PP}\cdot(2\cdot\pi)^2\cdot f_0^2\cdot L\cdot C}{0.66\cdot V_{IN}} \qquad \text{(EQ. 41)}$$

$$C_C = \frac{0.66\cdot V_{IN}}{(2\cdot\pi)^2\cdot f_0^2\cdot V_{PP}\cdot R_{FB}\cdot\sqrt{L\cdot C}}$$

Case 3: $f_0 > \frac{1}{2\cdot\pi\cdot C\cdot ESR}$

$$R_C = R_{FB}\cdot\frac{2\cdot\pi\cdot f_0\cdot V_{pp}\cdot L}{0.66\cdot V_{IN}\cdot ESR}$$

$$C_C = \frac{0.66\cdot V_{IN}\cdot ESR\cdot\sqrt{C}}{2\cdot\pi\cdot V_{PP}\cdot R_{FB}\cdot f_0\cdot\sqrt{L}}$$

The optional capacitor C_2, is sometimes needed to bypass noise away from the PWM comparator (see Figure 23). Keep a position available for C_2, and be prepared to install a high-frequency capacitor of between 22pF and 150pF in case any leading edge jitter problem is noted.

Compensation without Load-line Regulation

The non load-line regulated converter is accurately modeled as a voltage-mode regulator with two poles at the L-C resonant frequency and a zero at the ESR frequency. A

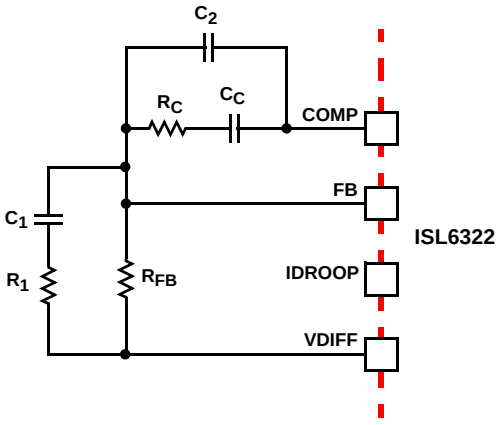


FIGURE 24. COMPENSATION CIRCUIT WITHOUT LOAD-LINE REGULATION

type III controller, as shown in Figure 24, provides the necessary compensation.

The first step is to choose the desired bandwidth, f_0, of the compensated system. Choose a frequency high enough to assure adequate transient performance but not higher than 1/3 of the switching frequency. The type-III compensator has an extra high-frequency pole, f_{HF}. This pole can be used for added noise rejection or to assure adequate attenuation at the error-amplifier high-order pole and zero frequencies. A good general rule is to choose $f_{HF} = 10f_0$, but it can be higher if desired. Choosing f_{HF} to be lower than $10f_0$ can cause problems with too much phase shift below the system bandwidth.

In the solutions to the compensation equations, there is a single degree of freedom. For the solutions presented in Equation 42, R_{FB} is selected arbitrarily. The remaining compensation components are then selected according to Equation 42.

In Equation 42, L is the per-channel filter inductance divided by the number of active channels; C is the sum total of all output capacitors; ESR is the equivalent-series resistance of the bulk output-filter capacitance; and V_{PP} is the peak-to-peak sawtooth signal amplitude as described in *Electrical Specifications on page* 7.

$$R_1 = R_{FB} \cdot \frac{C \cdot ESR}{\sqrt{L \cdot C} - C \cdot ESR}$$

$$C_1 = \frac{\sqrt{L \cdot C} - C \cdot ESR}{R_{FB}}$$

$$C_2 = \frac{0.75 \cdot V_{IN}}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{PP}}$$

$$R_C = \frac{V_{PP} \cdot (2\pi)^2 \cdot f_0 \cdot f_{HF} \cdot L \cdot C \cdot R_{FB}}{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}$$

$$C_C = \frac{0.75 \cdot V_{IN} \cdot (2 \cdot \pi \cdot f_{HF} \cdot \sqrt{L \cdot C} - 1)}{(2 \cdot \pi)^2 \cdot f_0 \cdot f_{HF} \cdot (\sqrt{L \cdot C}) \cdot R_{FB} \cdot V_{PP}} \quad \text{(EQ. 42)}$$

Output Filter Design

The output inductors and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase nodes. The output filter also must provide the transient energy until the regulator can respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response. The output capacitors must supply or sink load current while the current in the output inductors increases or decreases to meet the demand.

In high-speed converters, the output capacitor bank is usually the most costly (and often the largest) part of the circuit. Output filter design begins with minimizing the cost of this part of the circuit. The critical load parameters in choosing the output capacitors are the maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output-voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates by the amount specified in Equation 43.

$$\Delta V \approx ESL \cdot \frac{di}{dt} + ESR \cdot \Delta I \quad \text{(EQ. 43)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors also creates the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current (see *"Interleaving" on page 11* and Equation 2), a voltage develops across the bulk capacitor ESR equal to $I_{C,PP}(ESR)$. Thus, once the output capacitors are selected, the maximum allowable ripple voltage, $V_{PP(MAX)}$, determines the lower limit on the inductance.

$$L \geq ESR \cdot \frac{\left(V_{IN} - N \cdot V_{OUT}\right) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{PP(MAX)}} \quad \text{(EQ. 44)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 45 gives the upper limit on L for the cases when the trailing edge of the current transient causes a greater output-voltage deviation than the leading edge. Equation 46 addresses the leading edge. Normally, the trailing edge dictates the selection of L because duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In each equation:
L is the per-channel inductance,
C is the total output capacitance, and
N is the number of active channels.

$$L \leq \frac{2 \cdot N \cdot C \cdot V_O}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \quad \text{(EQ. 45)}$$

$$L \leq \frac{1.25 \cdot N \cdot C}{(\Delta I)^2} \cdot \left[\Delta V_{MAX} - (\Delta I \cdot ESR)\right] \cdot \left(V_{IN} - V_O\right) \quad \text{(EQ. 46)}$$

Switching Frequency

There are a number of variables to consider when choosing the switching frequency, as there are considerable effects on the upper MOSFET loss calculation. These effects are outlined in *MOSFETs*, and they establish the upper limit for the switching frequency. The lower limit is established by the requirement for fast transient response and small output-voltage ripple as outlined in *"Compensation without Load-line Regulation" on page 35*. Choose the lowest switching frequency that allows the regulator to meet the transient-response requirements.

Switching frequency is determined by the selection of the frequency-setting resistor, R_T. Figure 25 and Equation 47 are provided to assist in selecting the correct value for R_T.

$$R_T = 10^{[10.61 - (1.035 \cdot \log(f_S))]} \quad \text{(EQ. 47)}$$

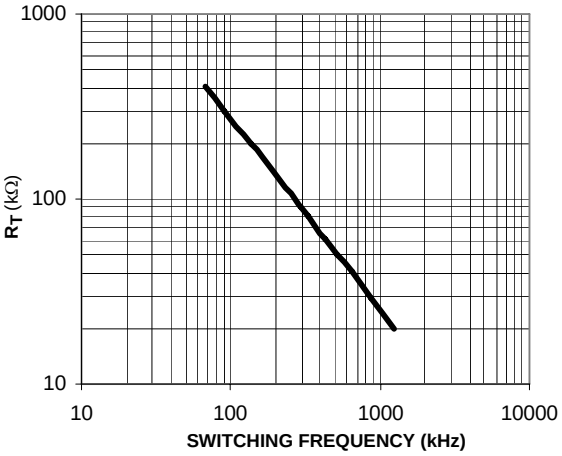


FIGURE 25. R_T vs SWITCHING FREQUENCY

Input Capacitor Selection

The input capacitors are responsible for sourcing the ac component of the input current flowing into the upper MOSFETs. Their RMS current capacity must be sufficient to handle the ac component of the current drawn by the upper MOSFETs which is related to duty cycle and the number of active phases.

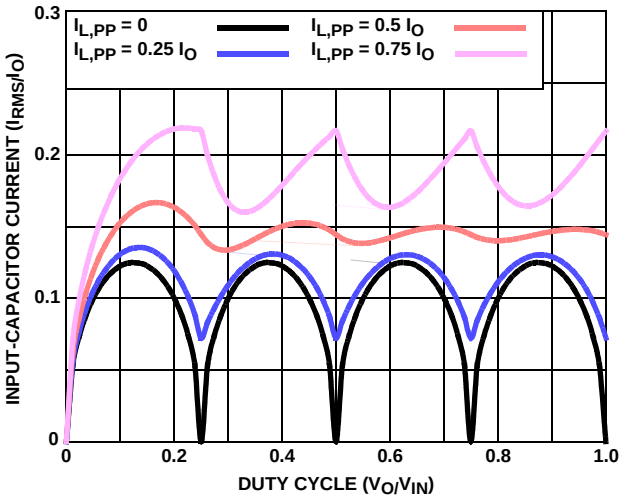


FIGURE 26. NORMALIZED INPUT-CAPACITOR RMS CURRENT vs DUTY CYCLE FOR 4-PHASE CONVERTER

For a four-phase design, use Figure 26 to determine the input-capacitor RMS current requirement set by the duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,PP}$) to I_O. Select a bulk capacitor with a ripple current rating that will minimize the total number of input capacitors required to support the RMS current calculated.

The voltage rating of the capacitors should also be at least 1.25 times greater than the maximum input voltage. Figures 27 and 28 provide the same input RMS current information for three-phase and two-phase designs respectively. Use the same approach for selecting the bulk capacitor type and number.

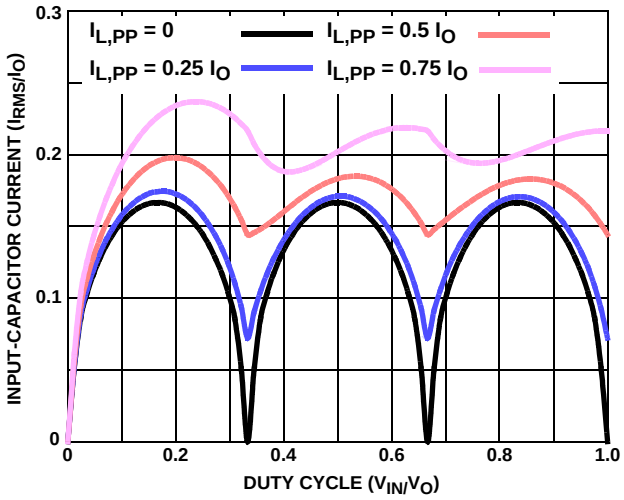


FIGURE 27. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 3-PHASE CONVERTER

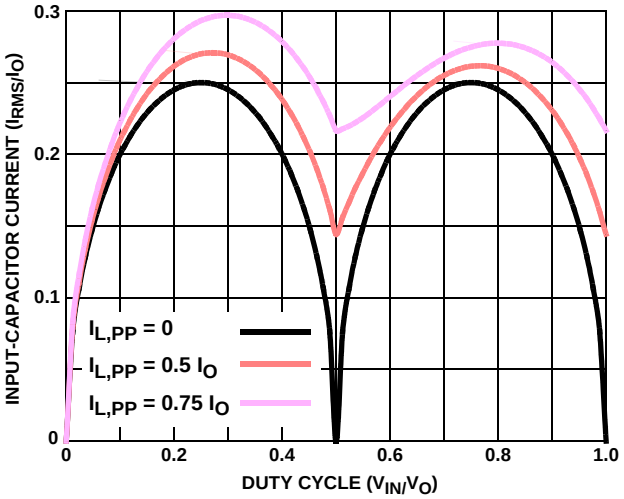


FIGURE 28. NORMALIZED INPUT-CAPACITOR RMS CURRENT FOR 2-PHASE CONVERTER

Low capacitance, high-frequency ceramic capacitors are needed in addition to the input bulk capacitors to suppress leading and falling edge voltage spikes. The spikes result from the high current slew rate produced by the upper MOSFET turn on and off. Select low ESL ceramic capacitors and place one as close as possible to each upper MOSFET drain to minimize board parasitics and maximize suppression.

Layout Considerations

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component selection, layout, and placement minimizes these voltage spikes. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC-DC converter using an ISL6322 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

The power components should be placed first, which include the MOSFETs, input and output capacitors, and the inductors. It is important to have a symmetrical layout for each power train, preferably with the controller located equidistant from each. Symmetrical layout allows heat to be dissipated equally across all power trains. Equidistant placement of the controller to the first three power trains it controls through the integrated drivers helps keep the gate drive traces equally short, resulting in equal trace impedances and similar drive capability of all sets of MOSFETs.

When placing the MOSFETs, try to keep the source of the upper FETs and the drain of the lower FETs as close as thermally possible. Input Bulk capacitors should be placed close to the drain of the upper FETs and the source of the lower FETs. Locate the output inductors and output capacitors between the MOSFETs and the load. The high-frequency input and output decoupling capacitors (ceramic) should be placed as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND next or on the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC, and many of the components surrounding the controller including the feedback network

and current sense components. Locate the VCC/PVCC bypass capacitors as close to the ISL6322 as possible. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up.

A multi-layer printed circuit board is recommended. Figure 29 shows the connections of the critical components for the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to output inductors short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Routing UGATE, LGATE, and PHASE Traces

Great attention should be paid to routing the UGATE, LGATE, and PHASE traces since they drive the power train MOSFETs using short, high current pulses. It is important to size them as large and as short as possible to reduce their overall impedance and inductance. They should be sized to carry at least one ampere of current (0.02” to 0.05”). Going between layers with vias should also be avoided, but if so, use two vias for interconnection when possible.

Extra care should be given to the LGATE traces in particular since keeping their impedance and inductance low helps to significantly reduce the possibility of shoot-through. It is also important to route each channels UGATE and PHASE traces in as close proximity as possible to reduce their inductances.

Current Sense Component Placement and Trace Routing

One of the most critical aspects of the ISL6322 regulator layout is the placement of the inductor DCR current sense components and traces. The R-C current sense components must be placed as close to their respective ISEN+ and ISEN- pins on the ISL6322 as possible.

The sense traces that connect the R-C sense components to each side of the output inductors should be routed on the bottom of the board, away from the noisy switching components located on the top of the board. These traces should be routed side by side, and they should be very thin traces. It’s important to route these traces as far away from any other noisy traces or planes as possible. These traces should pick up as little noise as possible.

Thermal Management

For maximum thermal performance in high current, high switching frequency applications, connecting the thermal GND pad of the ISL6322 to the ground plane with multiple vias is recommended. This heat spreading allows the part to achieve its full thermal potential. It is also recommended that the controller be placed in a direct path of airflow if possible to help thermally manage the part.

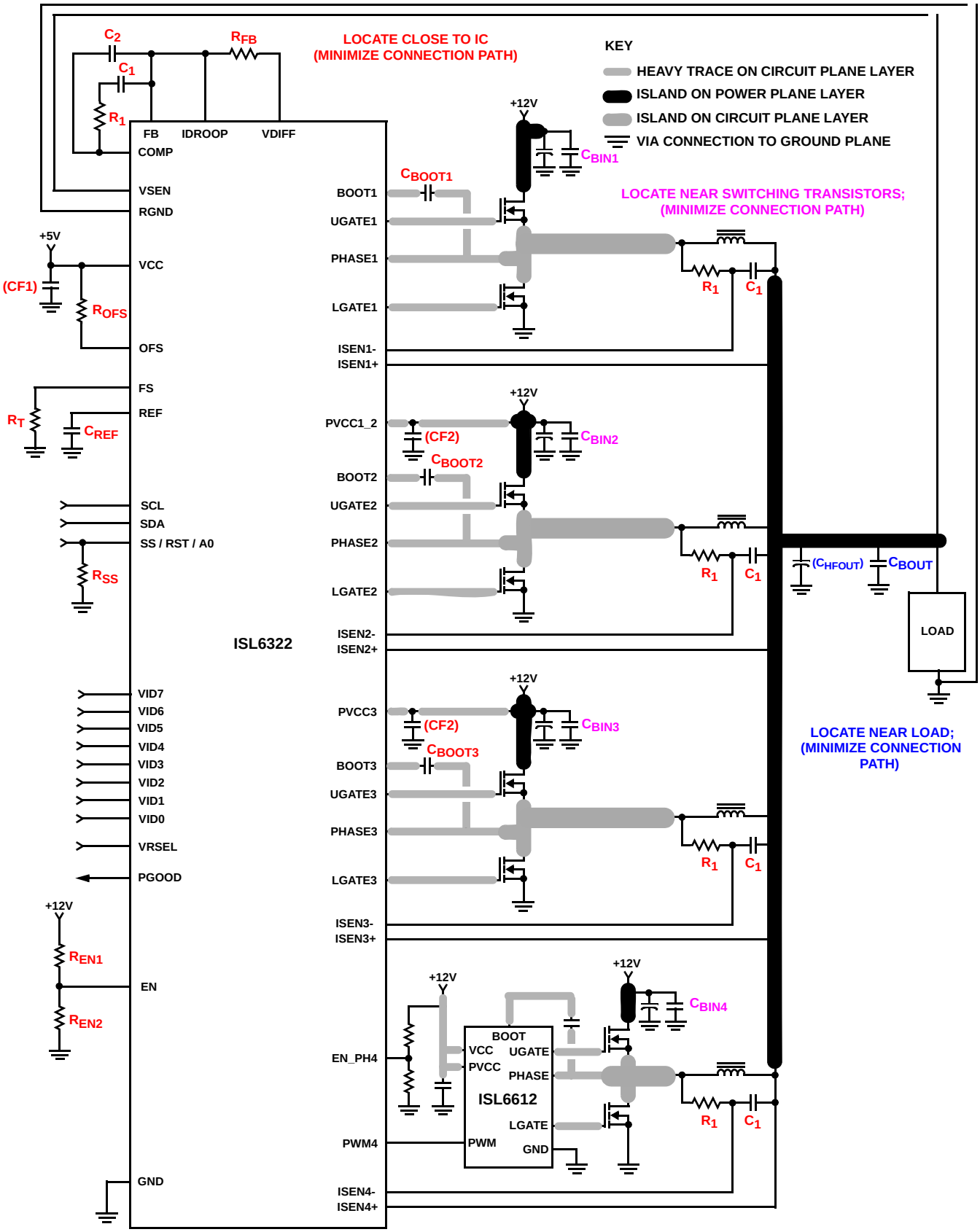
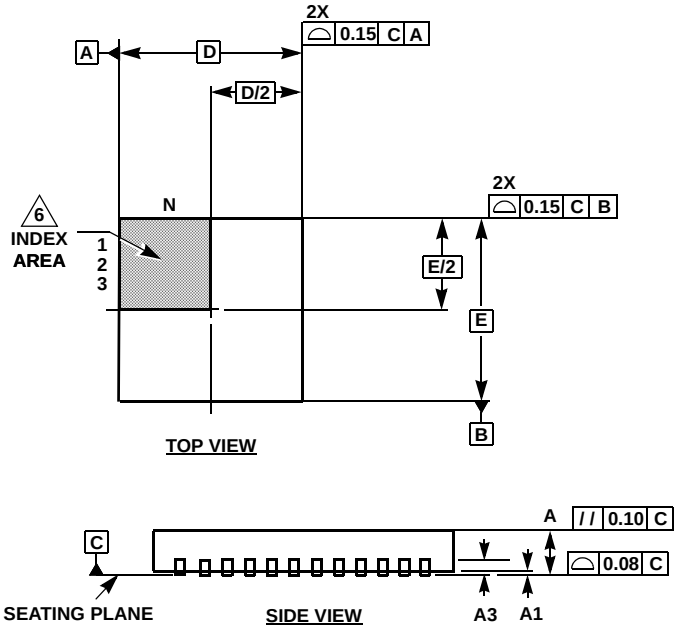
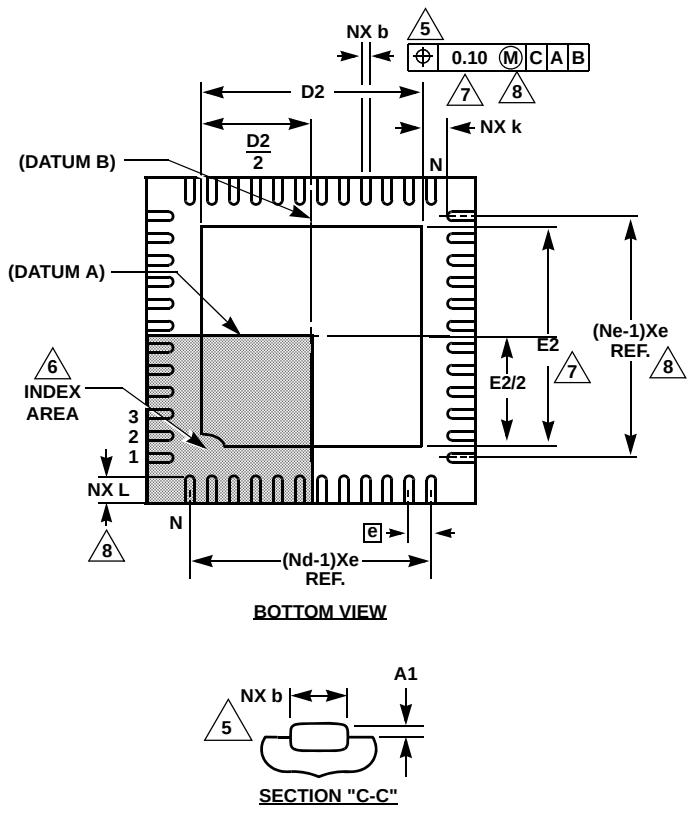


FIGURE 29. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)





L48.7x7

48 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VKKD-2 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5, 8
D		7.00 BSC		-
D2	4.15	4.30	4.45	7, 8
E		7.00 BSC		-
E2	4.15	4.30	4.45	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
N		48		2
Nd		12		3
Ne		12		3

Rev. 2 5/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.