BCM® Bus Converter

BCM384y120x1K5AC0

Unregulated DC-DC Converter

Features

- Up to 1500 W continuous output power
- 2133 W/in^3 power density
- 97.4% peak efficiency
- 4242 Vdc isolation
- Parallel operation for multi-kW arrays
- OV, OC, UV, short circuit and thermal protection
- 2361 through-hole ChiP package
  - 2.485" x 0.990" x 0.286"
    (63.13 mm x 25.14 mm x 7.26 mm)

Typical Applications

- 380 DC Power Distribution
- High End Computing Systems
- Automated Test Equipment
- Industrial Systems
- High Density Power Supplies
- Communications Systems
- Transportation

Product Ratings	
V_{IN} = 384 V (260 – 410 V)	P_{OUT} = up to 1500 W
V_{OUT} = 12.0 V (8.1 – 12.8 V) (NO LOAD)	K = 1/32

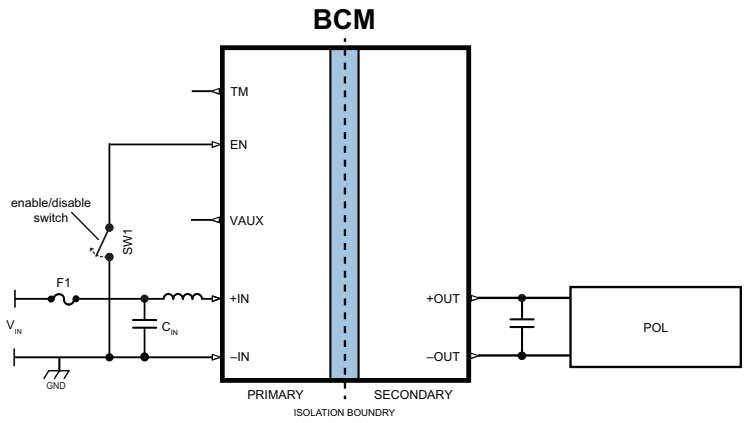
Product Description

The VI Chip® Bus Converter (BCM®) is a high efficiency Sine Amplitude Converter™ (SAC™), operating from a 260 to 410 VDC primary bus to deliver an isolated 8.1 to 12.8 VDC unregulated secondary voltage.

The BCM384y120x1K5AC0 offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the input of the BCM module. With a K factor of 1/32, that capacitance value can be reduced by a factor of 64x, resulting in savings of board area, material and total system cost.

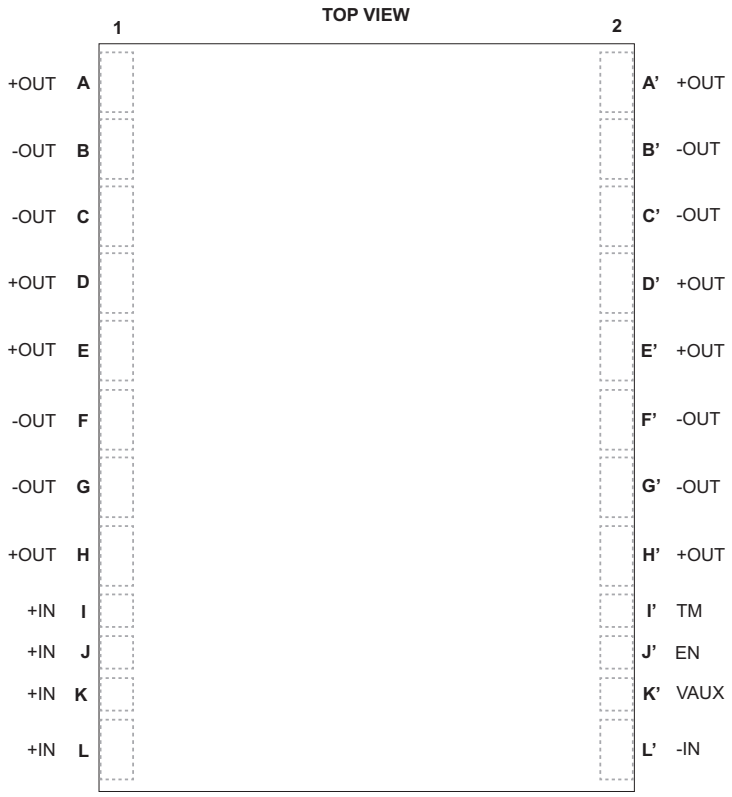
Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

Typical Application



BCM384y120x1K5AC0 + Point of load

Pin Configuration



2361 ChiP Package and Through hole device

Part Ordering Information

Device	Input Voltage Range	Package Type	Output Voltage x 10	Temperature Grade	Output Power	Revision	Package Size	Version
BCM	384	y	120	x	1K5	A	C	0
BCM = BCM	384 = 260 to 410 V	P = ChiP Through Hole	120 = 12.0 V	T = -40 to 125°C M = -55 to 125°C	1K5 = 1,500 W	A	C = 2361	0

All products shipped in JEDEC compliant trays.

Standard Models

Part Number	V_{IN}	Package Type	V_{OUT}	Temperature	Power	Package Size
BCM384**P**120**T**1K5AC0	260 to 410 V	ChiP Through Hole	12.0 V 8.1 to 12.8 V	-40°C to 125°C	1,500 W	2361

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to –IN		-1	480	V
V_{IN} slew rate (operational)		-1	1	V/µs
Isolation voltage, input to output	1 - 2 seconds applied to 100% production units		4242	V
+OUT to –OUT		-1	15	V
TM to –IN		-0.3	4.6	V
EN to –IN		-0.3	5.5	V
VAUX to –IN		-0.3	4.6	V

Electrical Specifications

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Powertrain						
Input voltage range, continuous	V_{IN_DC}		**260**		**410**	V
Input voltage range, transient	V_{IN_TRANS}	Full current or power supported, 50 ms max, 10% duty cycle max	**260**		**410**	V
V_{IN} µController Active	$V_{\mu C\_ACTIVE}$	V_{IN} voltage where µC is initialized, (ie VAUX = Low, powertrain inactive)			130	V
Input Voltage Slew Rate	dV_{IN}/dt	$V_{IN\_UVLO-} \le V_{IN} \le V_{IN\_OVLO+}$	**0.001**		**1000**	V/ms
Quiescent current	I_Q	Disabled, EN Low, V_{IN} = 384		2		mA
		$T_{INTERNAL}$ ≤ 100°C			4	
No load power dissipation	P_{NL}	V_{IN} = 384 V, $T_{INTERNAL}$ = 25°C		9	11.7	W
		V_{IN} = 384 V	**5.9**		**17**	
		V_{IN} = 260 V to 410 V, $T_{INTERNAL}$ = 25°C			13	
		V_{IN} = 260 V to 410 V			**19**	
Inrush current peak	I_{INR_P}	V_{IN} = 410 V, C_{OUT} = 1000 µF, R_{LOAD} = 25% of full load current		10		A
		$T_{INTERNAL}$ ≤ 100°C			15	
DC input current	I_{IN_DC}	At P_{OUT}= 1500 W, $T_{INTERNAL}$ ≤ 100°C			4.1	A
Transformation ratio	K	$K = V_{OUT}/V_{IN}$, at no load		1/32		V/V
Output power (average)	P_{OUT_AVG}	See Figure 1			1500	W
Output power (peak)	P_{OUT_PK}	10 ms max, $P_{OUT} \le P_{OUT\_AVG}$			2000	W
Output current (average)	I_{OUT_AVG}				125	A
Output current (peak)	I_{OUT_PK}	10 ms max, $I_{OUT} \le I_{OUT\_AVG}$			167	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 384 V, I_{OUT} = 125 A	TBD	96.7		%
		V_{IN} = 260 V to 410 V, I_{OUT} = 125 A	TBD			
		V_{IN} = 384 V, I_{OUT} = 62.5 A	TBD	97.4		
Efficiency (hot)	η_{HOT}	V_{IN} = 384 V, I_{OUT} = 125 A; $T_{INTERNAL}$ = 100°C	TBD	96.3		%
Efficiency (over load range)	$\eta_{20\%}$	25 A < I_{OUT} < 125 A, $T_{INTERNAL}$ ≤ 100°C	90			%
Output resistance	R_{OUT_COLD}	V_{IN} = 384 V, I_{OUT} = 125 A, $T_{INTERNAL}$ = -40°C	TBD	1.75	TBD	mΩ
	R_{OUT_AMB}	V_{IN} = 384 V, I_{OUT} = 125 A	TBD	2.25	TBD	
	R_{OUT_HOT}	V_{IN} = 384 V, I_{OUT} = 125 A, $T_{INTERNAL}$ = 100°C	TBD	2.75	TBD	
Switching frequency	F_{SW}	Frequency of the Output Voltage Ripple = 2x F_{SW}	**0.95**	1.00	**1.05**	MHz
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = 125 A, V_{IN} = 384 V, 20 MHz BW		195		mV
		$T_{INTERNAL}$ ≤ 100°C			250	
Input inductance (parasitic)	L_{IN_PAR}	Frequency 2.5 MHz (double switching frequency), Simulated lead model		7		nH
Output inductance (parasitic)	L_{OUT_PAR}	Frequency 2.5 MHz (double switching frequency), Simulated lead model		0.64		nH
Input Series inductance (internal)	L_{IN_INT}	Reduces the need for input decoupling inductance in BCM arrays		0.56		µH
Effective Input capacitance (internal)	C_{IN_INT}	Effective value at 384 V_{IN}		0.37		µF

Electrical Specifications (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
		Powertrain (Cont.)				
Effective Output capacitance (internal)	C_{OUT_INT}	Effective value at 12.0 V_{OUT}		208		µF
Effective Output capacitance (external)	C_{OUT_EXT}	Excessive capacitance may drive module into SC protection	**0**		**1000**	µF
Array Maximum external output capacitance	C_{OUT_AEXT}	C_{OUT_AEXT} Max = N * 0.5*C_{OUT_EXT} Max				
		Protection				
Auto Restart Time	$t_{AUTO\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{IN} > V_{IN_UVLO+}	**292.5**		**357.5**	ms
Input overvoltage lockout threshold	V_{IN_OVLO+}		**420**	434.5	**450**	V
Input overvoltage recovery threshold	V_{IN_OVLO-}		**410**	424	**440**	V
Input overvoltage lockout hysteresis	$V_{IN\_OVLO\_HYST}$			10.5		V
Overvoltage lockout response time	t_{OVLO}			100		µs
Input undervoltage lockout threshold	V_{IN_UVLO-}		**200**	221	**240**	V
Input undervoltage recovery threshold	V_{IN_UVLO+}		**225**	243	**255**	V
Input undervoltage lockout hysteresis	$V_{IN\_UVLO\_HYST}$			15		V
Undervoltage lockout response time	t_{UVLO}			100		µs
Undervoltage startup delay	t_{UVLO+_DELAY}	From V_{IN} = V_{IN_UVLO+} to powertrain active, EN floating (i.e One time Startup delay form application of V_{IN} to V_{OUT})		20		ms
Soft-Start time	$t_{SOFT-START}$	From powertrain active Fast Current limit protection disabled during Soft-Start		1		ms
Output overcurrent trip threshold	I_{OCP}		**TBD**	TBD	**TBD**	A
Output overcurrent response time constant	t_{OCP}	Effective internal RC filter		TBD		ms
Short circuit protection trip threshold	I_{SCP}		**TBD**			A
Short circuit protection response time	t_{SCP}			1		µs
Overtemperature shutdown threshold	t_{OTP}	Temperature sensor located inside controller IC	**125**			°C
Undertemperature shutdown threshold	t_{UTP}	Temperature sensor located inside controller IC			**-45**	°C
Undertemperature Restart time	$t_{UTP\_RESTART}$	Startup into a persistent fault condition. Non-Latching fault detection given V_{IN} > V_{IN_UVLO+}		3		s

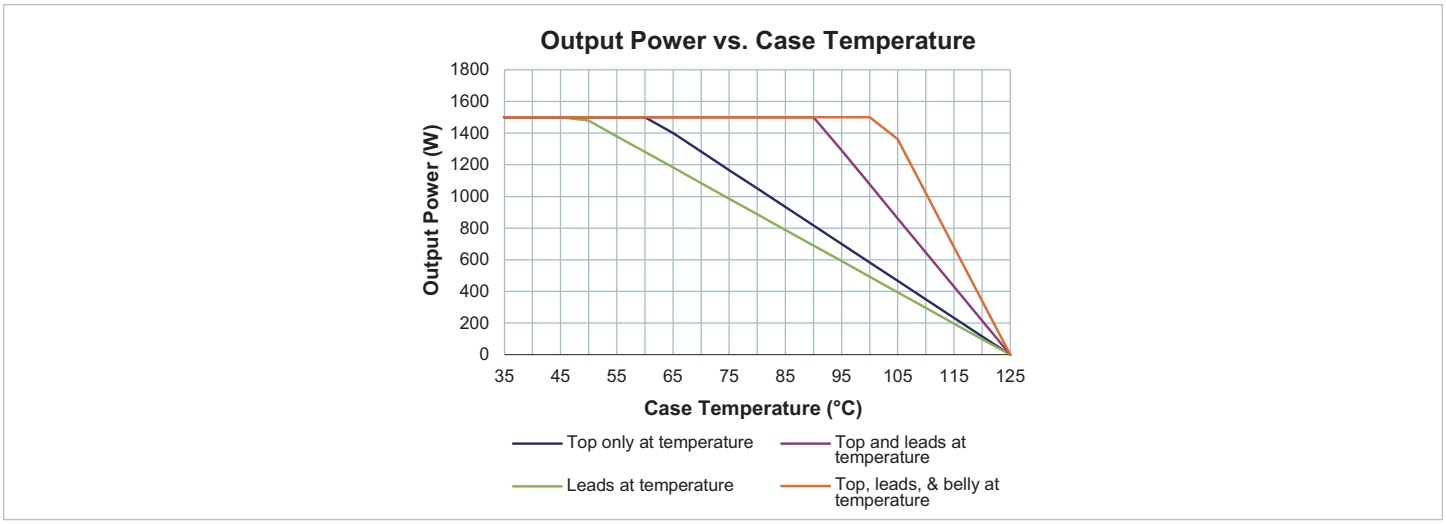


Figure 1 — *Safe thermal operating area*

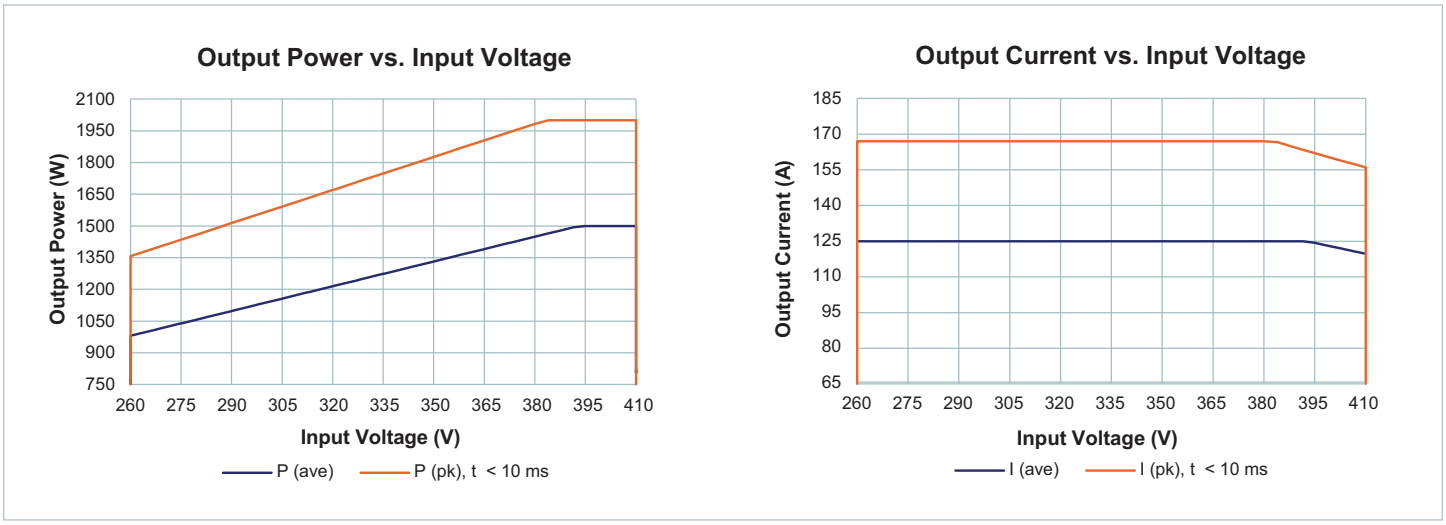


Figure 2 — *Safe electrical operating area*

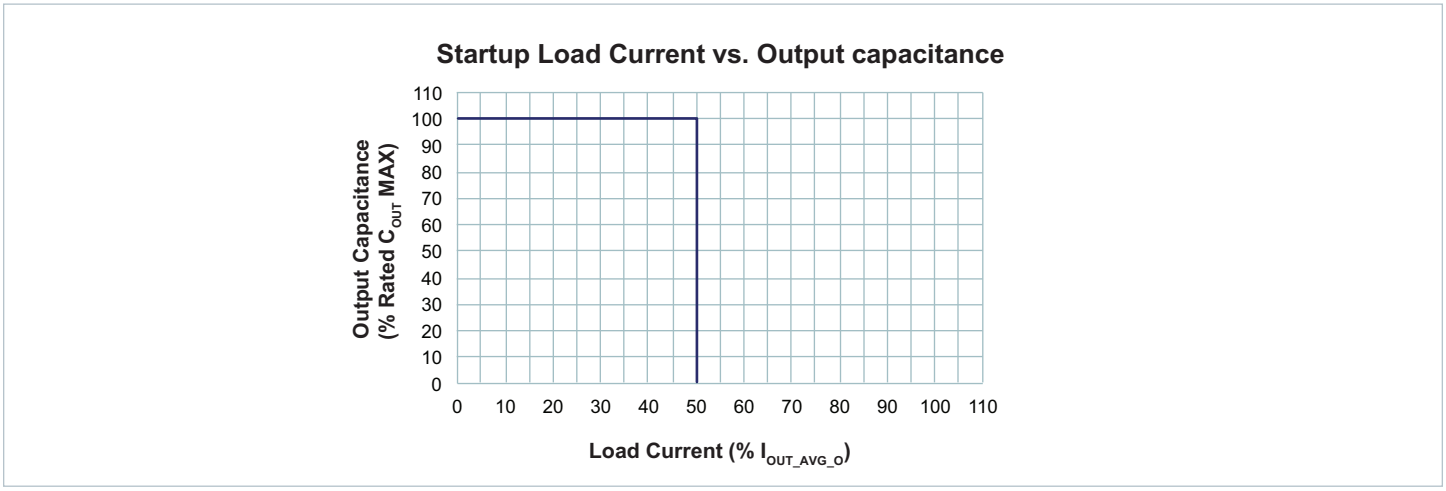


Figure 3 — *Safe operating area; Start Up Load current vs. Output capacitance*

Signal Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Temperature Monitor

- The TM pin is a standard analog I/O configured as an output from an internal µC.
- µC 250 kHz PWM output internally pulled high to 3.3 V.
- The TM pin monitors the internal temperature of the controller IC within an accuracy of ±5°C.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
DIGITAL OUTPUT	Start Up	Powertrain active to TM time	t_{VAUX}	Powertrain active to TM PWM		**100**		µs
	Regular Operation	TM Duty Cycle	V_{TM}		**18.18**		**68.18**	%
		TM Current	I_{TM}				**4**	mA
		Recommended External filtering:						
		TM Capacitance (External)	C_{TM_EXT}	Recommended External filtering		0.01		µF
		TM Resistance (External)	R_{TM_EXT}	Recommended External filtering		1		kΩ
		Specifications using recommended filter:						
		TM Gain	A_{TM}				10	mV/°C
		TM Voltage Reference	V_{TM_AMB}	Controller $T_{INTERNAL}$ = 27°C		1.27		V
		TM Voltage Ripple	V_{TM_PP}	R_{TM_EXT} = 1 KΩ, C_{TM_EXT} = 0.01 µF, V_{IN} = 384 V, I_{OUT} = 125 A		28		mV
				$T_{INTERNAL}$ ≤ 100°C			**40**	mV

ENABLE Control

- The EN pin is a standard analog I/O configured as an input to an internal µC.
- It is internally pulled high to 3.3 V.
- When held low the BCM® internal bias will be disabled and the powertrain will be inactive.
- In an array of BCMs, EN pins should be interconnected to synchronize startup and permit startup into full load conditions.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Start Up	EN Pull-down Resistance (External)	R_{EN_EXT}	Module may not start with lower value	**0.4**			kΩ
		EN to Powertrain active time	t_{EN_START}	V_{IN} > V_{IN_UVLO+}, EN held low both conditions satisfied for t > t_{UVLO+_DELAY}		**250**		µs
	Regular Operation	EN Voltage Threshold	V_{EN_TH}		**0.7**			V
		EN Resistance (Internal)	R_{EN_INT}	Internal pull up resistor		1.5		kΩ
		EN Disable Threshold	$V_{EN\_DISABLE\_TH}$				**0.30**	V
	Fault	Time off	t_{ENABLE_OFF}	Module will ignore attempts to . re-enable during time off	**292.5**		**357.5**	ms

Signal Characteristics (Cont.)

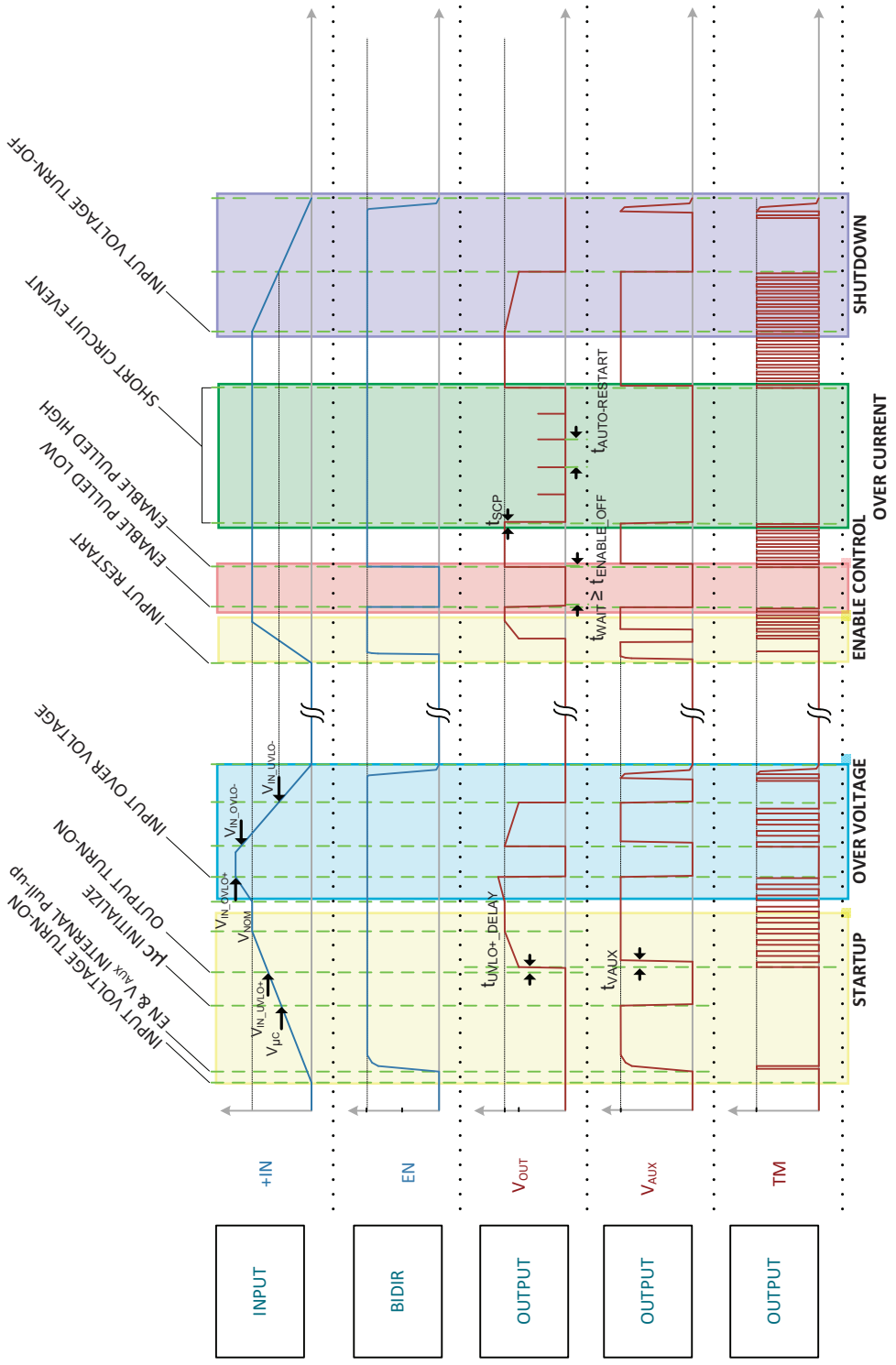
Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Auxilary Voltage Source

- The VAUX pin is a standard analog I/O configured as an output from an internal µC.
- VAUX is internally connected to µC output as internally pulled high to a 3.3 V regulator with 2% tolerance, a 1% resistor of 1.5 KΩ.
- VAUX can be used as a "Ready to process full power" flag. This pin transitions VAUX voltage after a 2 ms delay from the start of powertrain activating, signaling the end of softstart.
- VAUX can be used as "Fault flag". This pin is pulled low internally when a fault protection is detected.

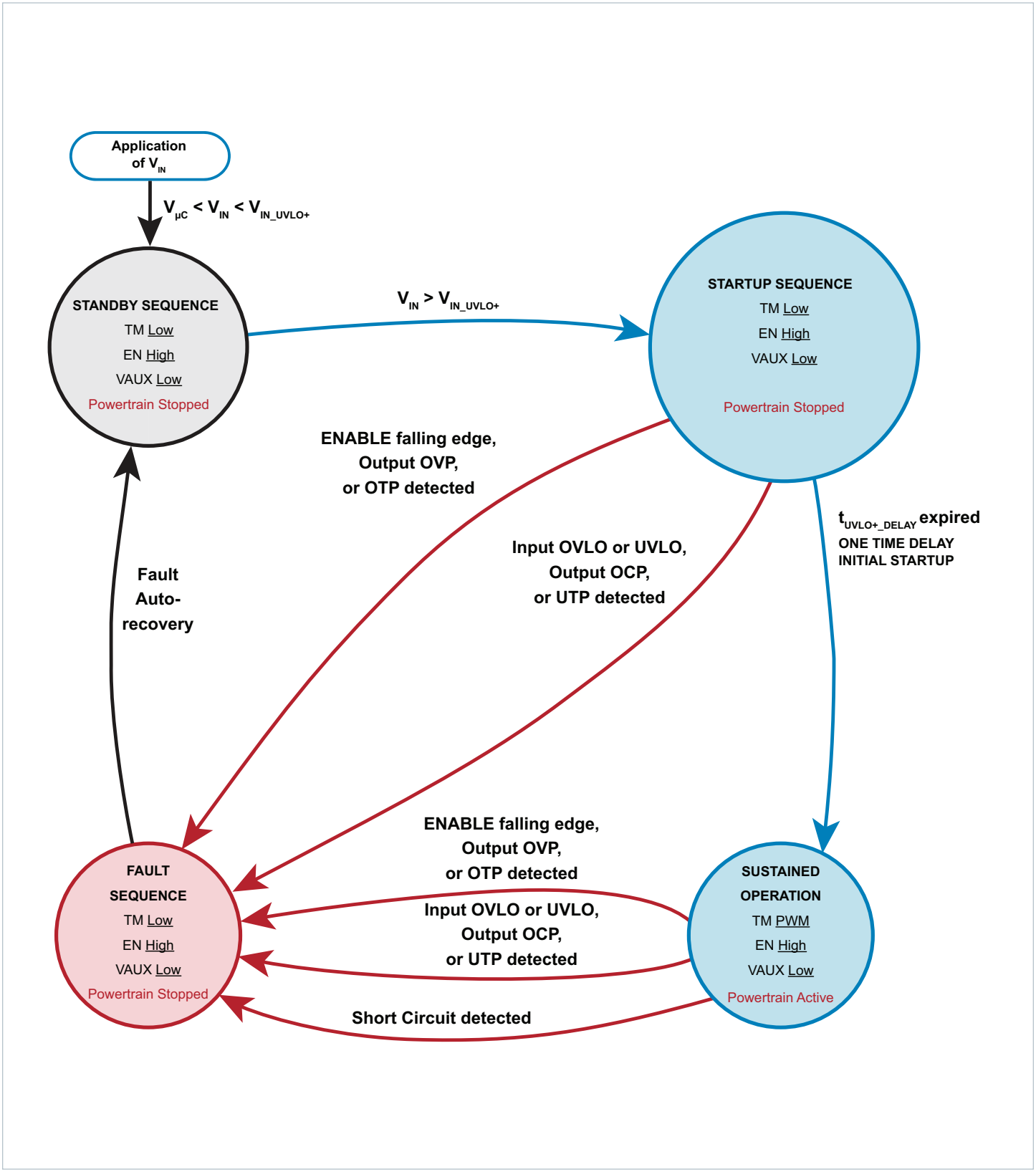
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Start Up	Powertrain active to VAUX time	t_{VAUX}	Powertrain active to VAUX high		**2**		ms
	Regular Operation	VAUX Voltage	V_{VAUX}		**2.8**		**3.3**	V
		VAUX Avaliable Current	I_{VAUX}				**4**	mA
		VAUX Voltage Ripple	V_{VAUX_PP}			50		mV
				$T_{INTERNAL}$ ≤ 100°C			**100**	mV
		VAUX Capacitance (External)	C_{VAUX_EXT}				0.01	µF
		VAUX Resistance (External)	R_{VAUX_EXT}	$V_{IN} < V_{µC\_ACTIVE}$	1.5			kΩ
	Fault	VAUX Fault Response Time	t_{FR_TM}	From fault detection to VAUX = 2.8 V, C_{VAUX} = 0 pF		10		µs

BCM Module Timing diagram



High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



Application Characteristics

Product is mounted and temperature controlled via top side cold plate, unless otherwise noted. See associated figures for general trend data.

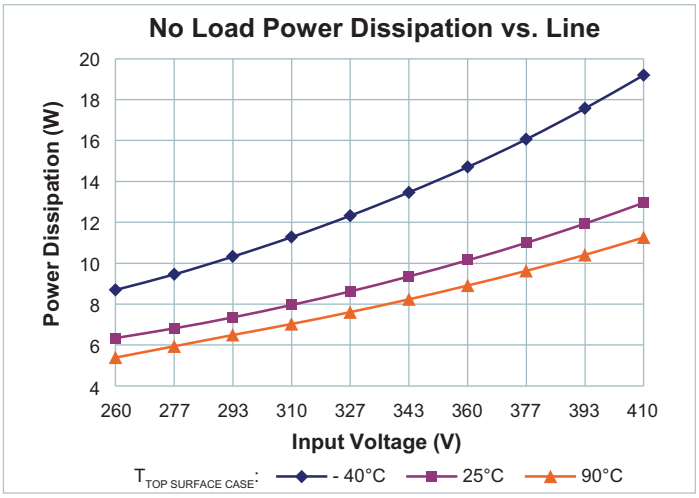


Figure 4 — *No load power dissipation vs. V_{IN}*

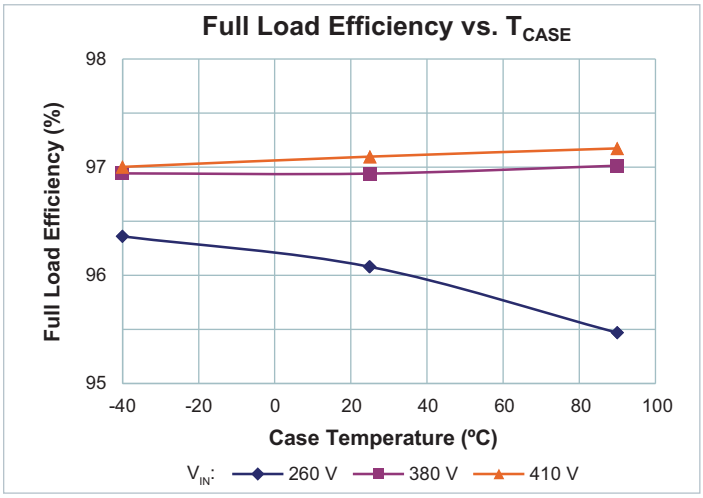


Figure 5 — *Full load efficiency vs. temperature; V_{IN}*

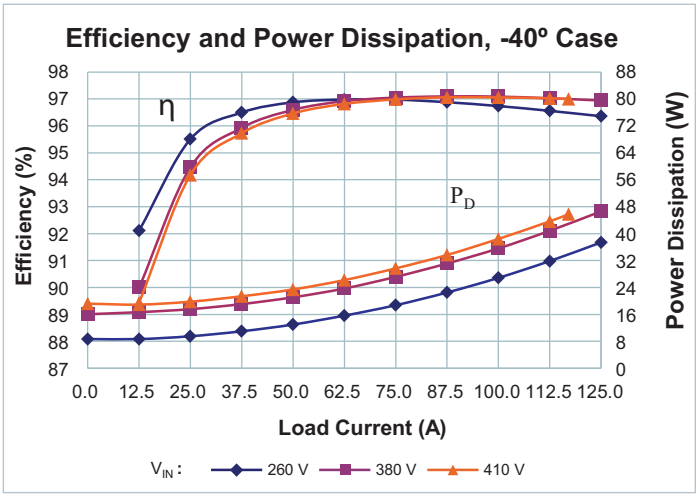


Figure 6 — *Efficiency and power dissipation at $T_{INTERNAL}$ = -40°C*

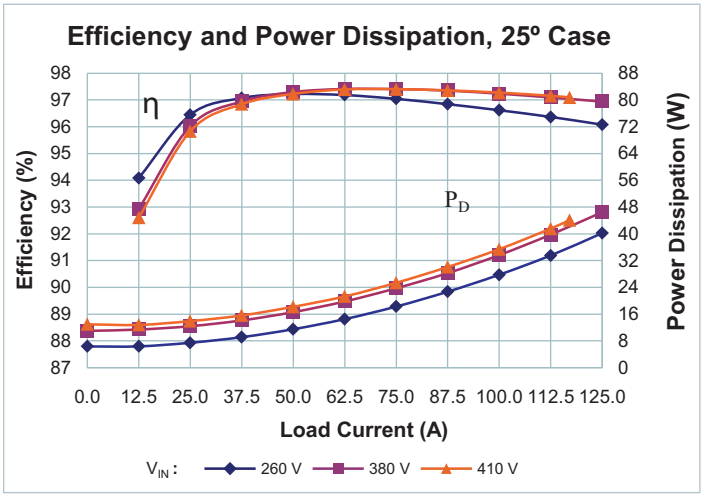


Figure 7 — *Efficiency and power dissipation at $T_{INTERNAL}$ = 25°C*

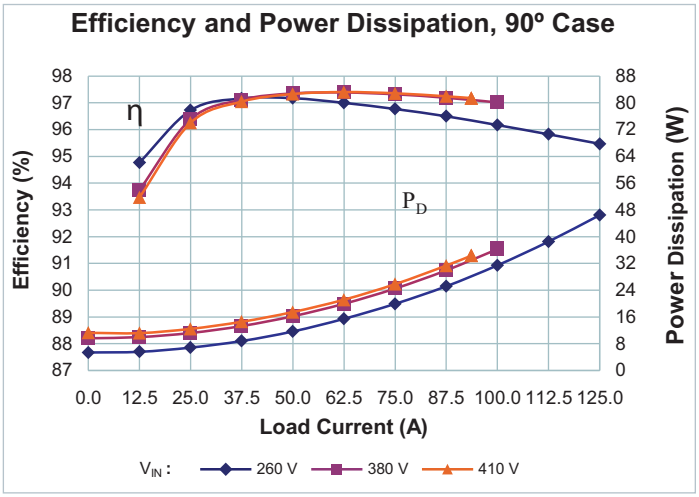


Figure 8 — *Efficiency and power dissipation at $T_{INTERNAL}$ = 90°C*

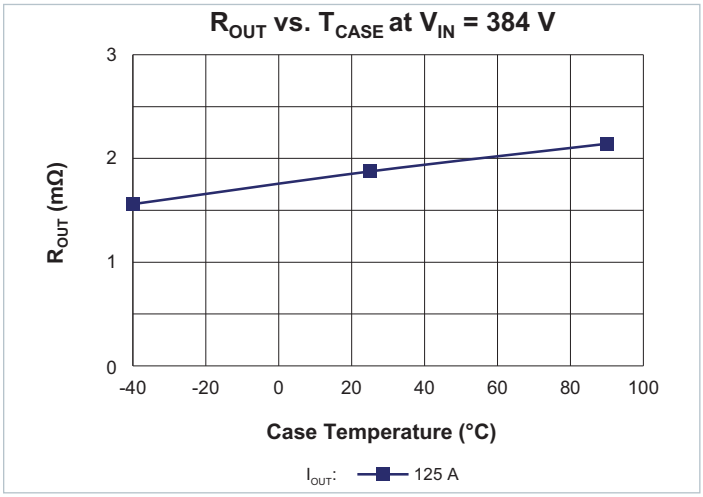


Figure 9 — *R_{OUT} vs. temperature*

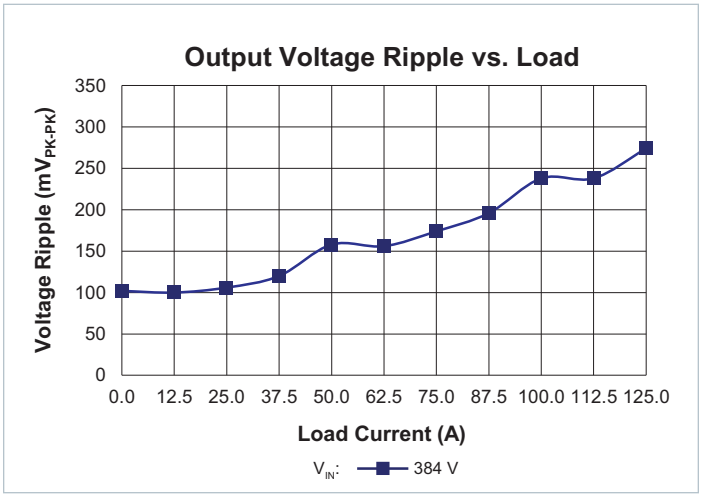


Figure 10 — *V_{RIPPLE} vs. I_{OUT} ; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW*

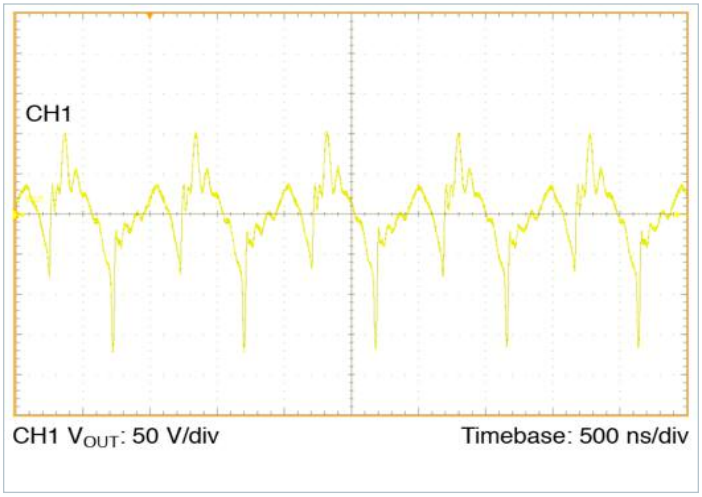


Figure 11 — *Full load ripple, 10 µF C_{IN}; No external C_{OUT}. Board mounted module, scope setting : 20 MHz analog BW*

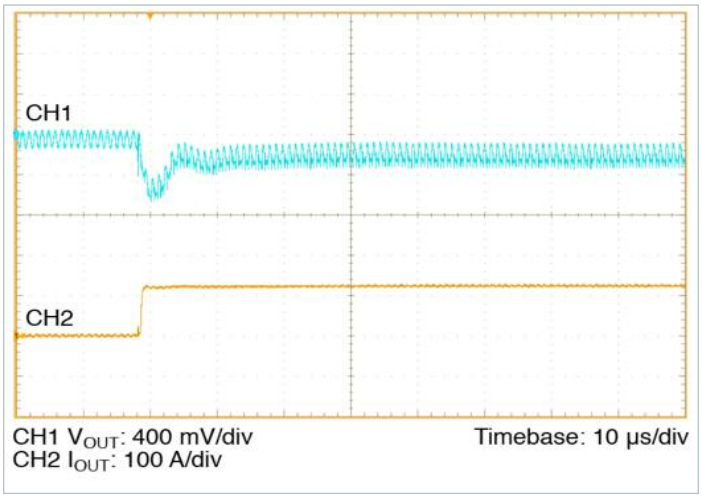


Figure 12 — *0 A– 125 A transient response: C_{IN} = 10 µF, no external C_{OUT}*

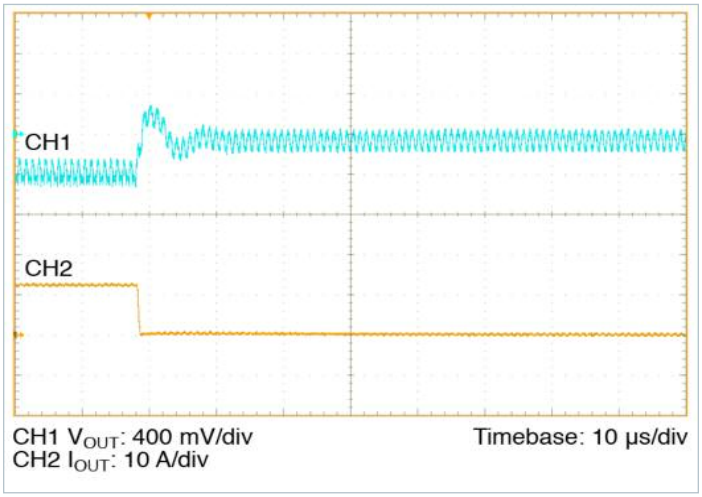


Figure 13 — *125 A – 0 A transient response: C_{IN} = 10 µF, no external C_{OUT}*

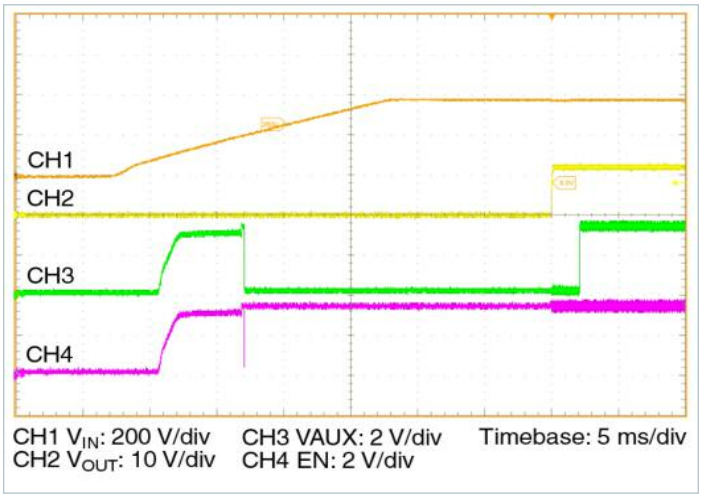


Figure 14 — *Start up from application of V_{IN} = 384 V, 50% I_{OUT}, 100% C_{OUT}*

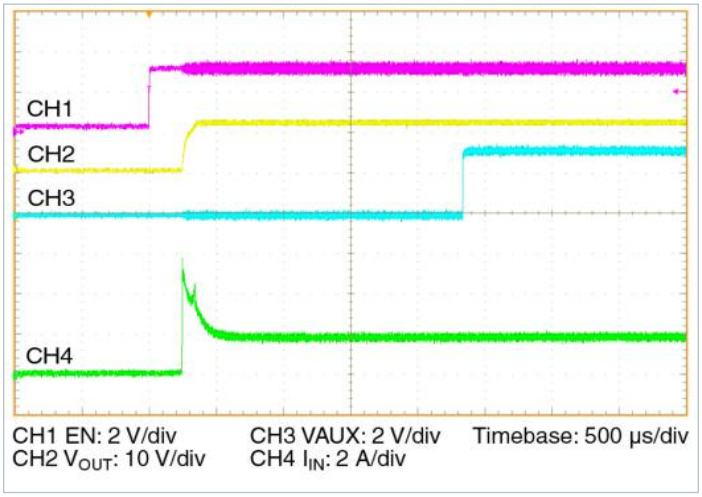


Figure 15 — *Start up from application of EN with pre-applied V_{IN} = 384 V, 50% I_{OUT}, 100% C_{OUT}*

General Characteristics

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
		Mechanical				
Length	L		63.00 / [2.480]	63.13 / [2.485]	63.26 / [2.491]	mm / [in]
Width	W		24.76 / [0.975]	25.14 / [0.990]	25.52 / [1.005]	mm / [in]
Height	H		7.21 / [0.284]	7.26 / [0.286]	7.31 / [0.288]	mm / [in]
Volume	Vol	Without heatsink		11.52 / [0.703]		cm^3/ [in^3]
Weight	W			41 / [1.45]		g / [oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
		Thermal				
Operating temperature	$T_{INTERNAL}$	BCM384P120T1K5AC0 (T-Grade)	-40		125	°C
		BCM384P120M1K5AC0 (M-Grade)	N/A		N/A	°C
Thermal resistance top side	$\phi_{INT-TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		1.14		°C/W
Thermal resistance leads	$\phi_{INT-LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		1.35		°C/W
Thermal resistance bottom side	$\phi_{INT-BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		1.07		°C/W
Thermal capacity				34		Ws /°C
		Assembly				
Storage Temperature	T_{ST}	BCM384P120T1K5AC0 (T-Grade)	-55		125	°C
		BCM384P120M1K5AC0 (M-Grade)	N/A		N/A	°C
ESD Withstand	ESD_{HBM}	Human Body Model, "ESDA / JEDEC JDS-001-2012" Class I-C (1kV to < 2 kV)				
	ESD_{CDM}	Charge Device Model, "JESD 22-C101-E" Class II (200V to < 500V)				

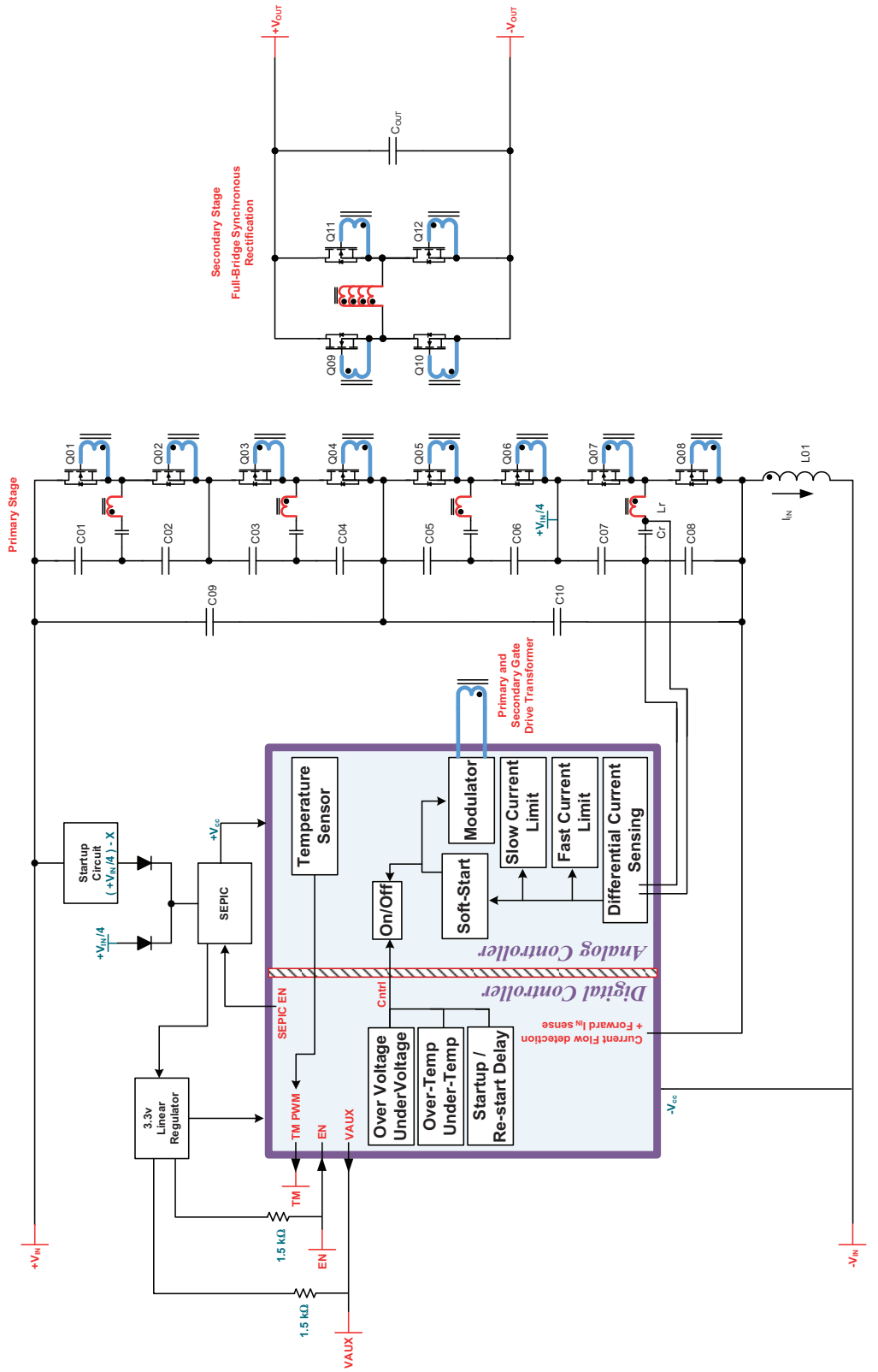
General Characteristics (Cont.)

Specifications apply over all line, load conditions, unless otherwise noted; **Boldface** specifications apply over the temperature range of -40°C ≤ $T_{INTERNAL}$ ≤ 125°C (T-Grade); All other specifications are at $T_{INTERNAL}$ = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
		Soldering [1]				
Peak temperature Top case					135	°C
Peak temperature gradient (Top CASE - Lead)		Temp Gradient is measured at the time the lead is in solder and reaches its maximum temp of 257°C			141	°C/s
Peak temperature gradient (Top CASE - Lead) interconnect		Temp Gradient is at the moment that the lead top (interconnect) reaches its maximum temp of 199°C. At that time temp of top of the ChiP is 117°C.			82	°C/s
		Safety				
Isolation voltage	V_{HIPOT}	IN to OUT	**4,242**			VDC
		IN to CASE	**2,121**			
		OUT to CASE	**2,121**			
Isolation capacitance	C_{IN_OUT}	Unpowered unit	**620**	**780**	**940**	pF
Isolation resistance	R_{IN_OUT}	At 500 Vdc	**10**			MΩ
MTBF		MIL-HDBK-217Plus Parts Count - 25°C Ground Benign, Stationary, Indoors / Computer		2.31		MHrs
		Telcordia Issue 2 - Method I Case III; 25°C Ground Benign, Controlled		TBD		MHrs
Agency approvals / standards		cTUVus				
		cURus				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

[1] Product is not intended for reflow solder attach.

BCM Module Block Diagram



Sine Amplitude Converter™ Point of Load Conversion

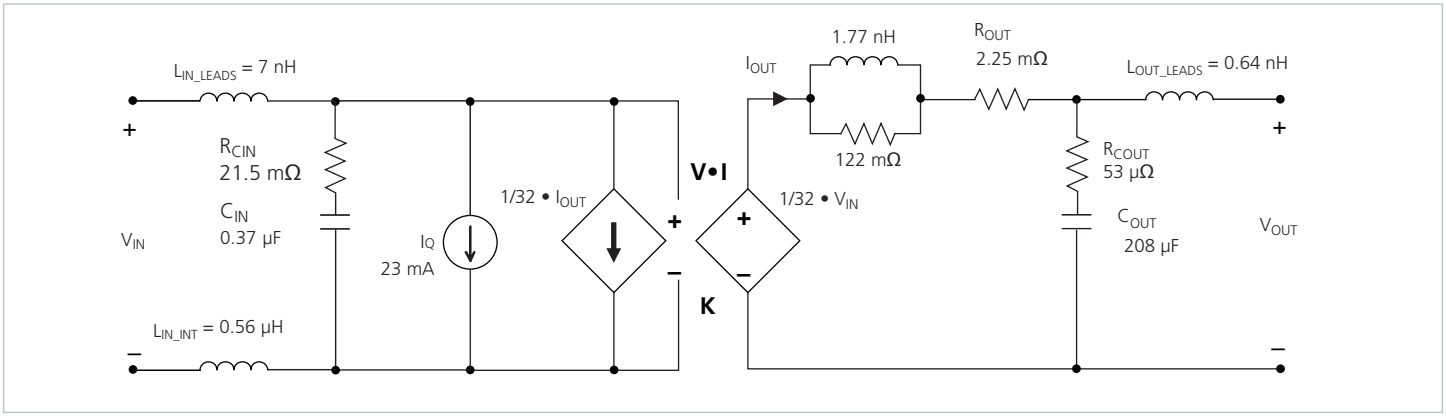


Figure 16 — *BCM module AC model*

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. (The resonant tank is formed by Cr and leakage inductance Lr in the power transformer windings as shown in the BCM module Block Diagram). The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

The BCM384y120x1K5AC0 SAC can be simplified into the preceeding model.

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC.
Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, V_{OUT} is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and I_{OUT} is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. I_Q represents the quiescent current of the SAC control, gate drive circuitry, and core losses.

The use of DC voltage transformation provides additional interesting attributes. Assuming that $R_{OUT} = 0\ \Omega$ and $I_Q = 0$ A, Eq. (3) now becomes Eq. (1) and is essentially load independent, resistor R is now placed in series with V_{IN}.

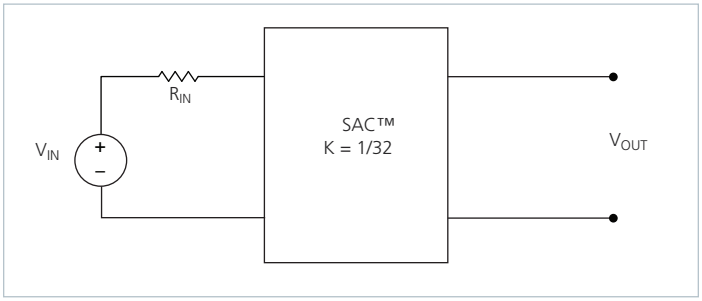


Figure 17 — *K = 1/32 Sine Amplitude Converter with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R_{IN}) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{IN} \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 1 mΩ, with K = 1/32 .

A similar exercise should be performed with the additon of a capacitor or shunt impedance at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 16.

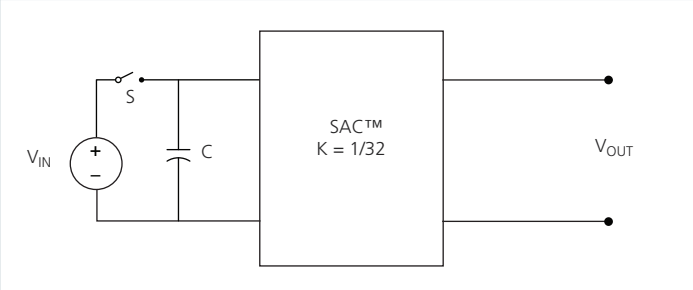


Figure 18 — *Sine Amplitude Converter with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dV_{IN}}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \qquad (8)$$

substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \qquad (9)$$

The equation in terms of the output has yielded a K^2 scaling factor for C, specified in the denominator of the equation.

A K factor less than unity results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/32 as shown in Figure 17, C=1 µF would appear as C=1024 µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared. However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies also reduces core losses.

The two main terms of power loss in the BCM module are:

- No load power dissipation (P_{NL}): defined as the power used to power up the module with an enabled powertrain at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the BCM® module modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{R_{OUT}} \qquad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} \qquad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

Input and Output Filter Design

A major advantage of SAC™ systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

- Guarantee low source impedance:

  To take full advantage of the BCM module's dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the bus converter module to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 1 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

- Further reduce input and/or output voltage ripple without sacrificing dynamic response:

  Given the wide bandwidth of the module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.

- Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and induce stresses:

  The module input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even when disabled, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Total load capacitance at the output of the BCM module shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the module, low-frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the module. At frequencies <500 kHz the module appears as an impedance of R_{OUT} between the source and load.

Within this frequency range, capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. (13).

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad (13)$$

This enables a reduction in the size and number of capacitors used in a typical system.

Thermal Considerations

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 1.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 18 shows the "thermal circuit" for a VI Chip® BCM module 2361 in an application where the top, bottom, and leads are cooled. In this case, the BCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed using a SPICE simulator with simple resistors, voltage sources, and a current source. The results of the simulation would provide an estimate of heat flow through the various pathways as well as internal temperature.

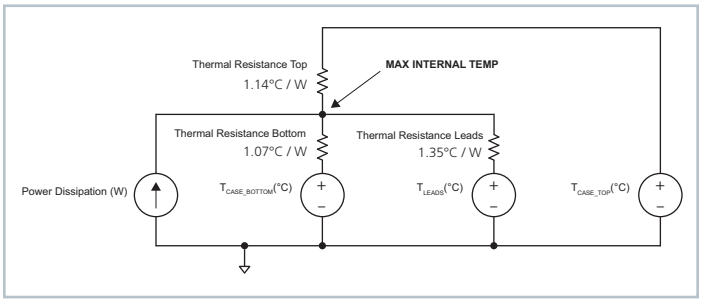


Figure 19 — *Double side cooling and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE\_TOP}$

$T_{INT} - PD_2 \bullet 1.24 = T_{CASE\_BOTTOM}$

$T_{INT} - PD_3 \bullet 7 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_2 + PD_3$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads respectively.

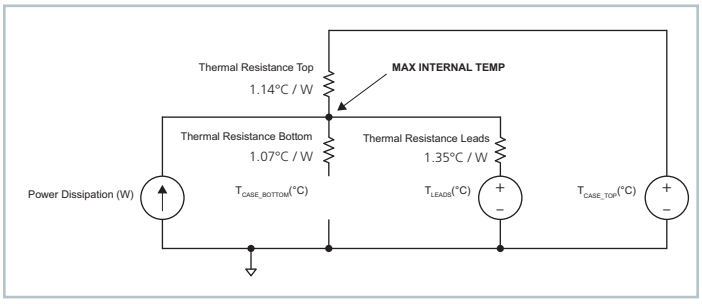


Figure 20 — *One side cooling and leads thermal model*

Figure 19 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE\_TOP}$

$T_{INT} - PD_3 \bullet 7 = T_{LEADS}$

$PD_{TOTAL} = PD_1 + PD_3$

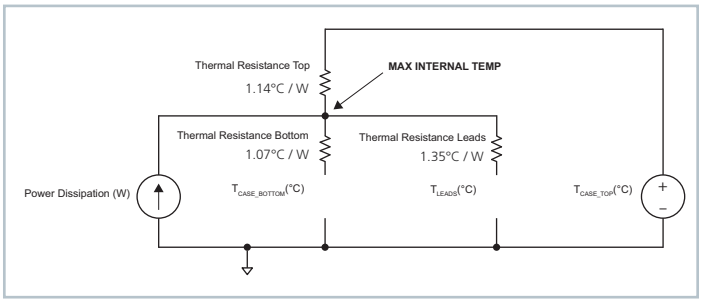


Figure 21 — *One side cooling thermal model*

Figure 20 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$T_{INT} - PD_1 \bullet 1.24 = T_{CASE\_TOP}$

$PD_{TOTAL} = PD_1$

Please note that Vicor has a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a BCM thermal configuration is valid for a given condition. These tools can be found at: http://www.vicorpower.com/powerbench.

Current Sharing

The performance of the SAC™ topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances include:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide as symmetric a PCB layout as possible among modules
- An input filter is required for an array of BCMs in order to prevent circulating currents.

For further details see AN:016 Using BCM Bus Converters in High Power Arrays.

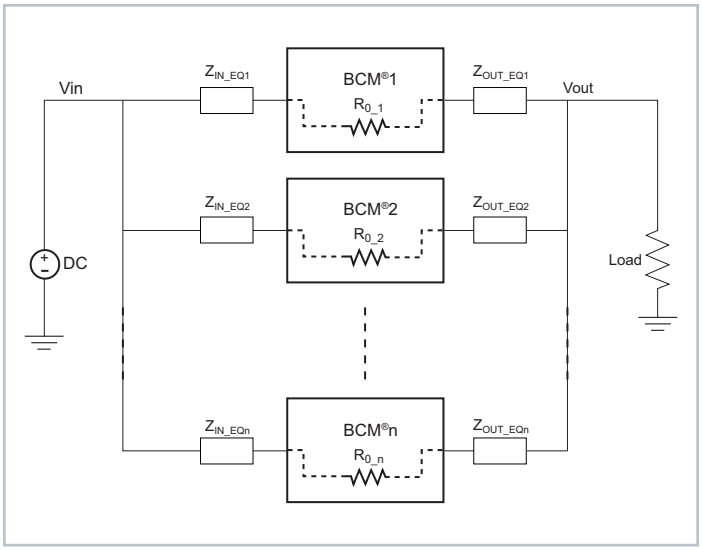


Figure 22 — *BCM module array*

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® modules are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating
  (usually greater than maximum current of BCM module)
- Maximum voltage rating
  (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommend fuse: ≤ 5 A Bussmann PC-Tron

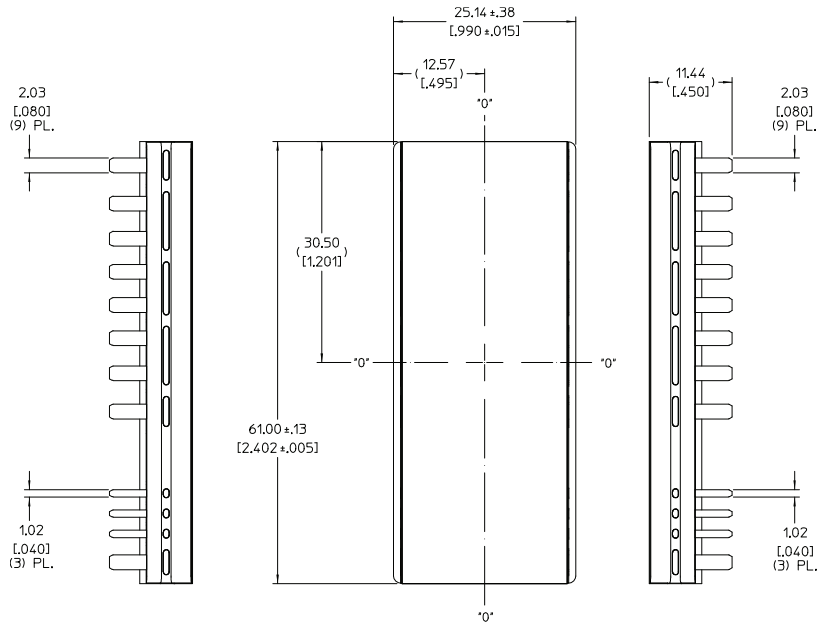
Reverse Operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds $V_{IN} \bullet K$. The module will continue operation in this fashion for as long as no faults occur.

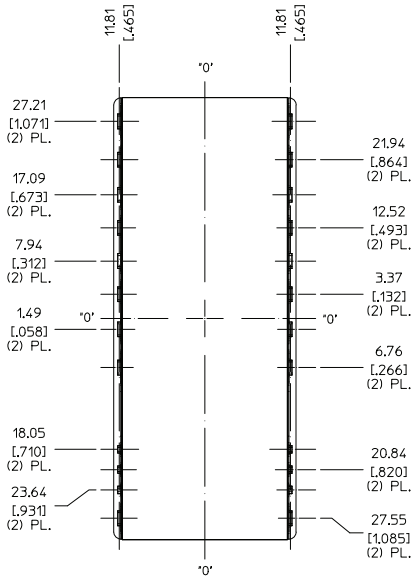
The BCM384y120x1K5AC0 has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10 ms, 10% duty cycle is permitted and has been qualified to cover these cases.

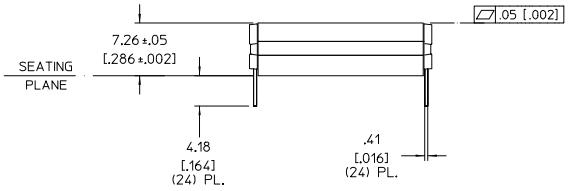
BCM Module Through Hole Package Mechanical Drawing and Recommended Land Pattern



TOP VEIW (COMPONENT SIDE)

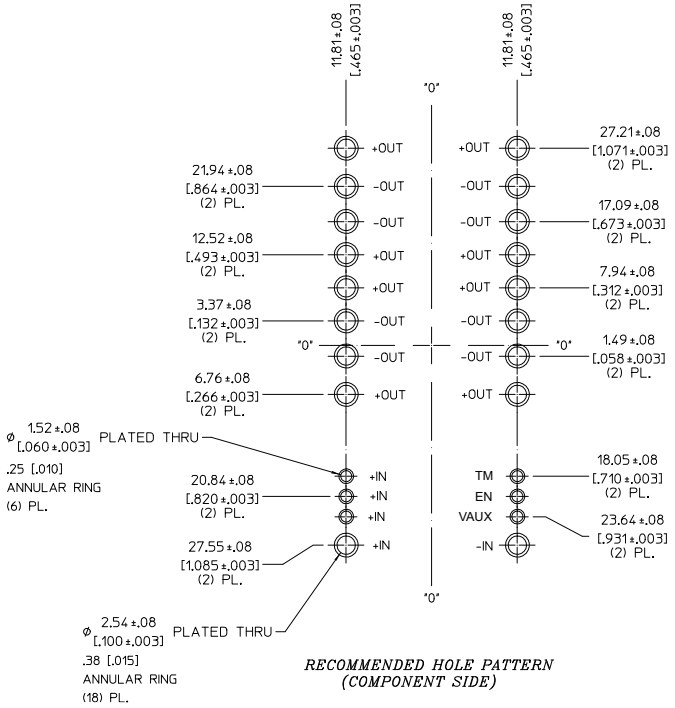


BOTTOM VIEW



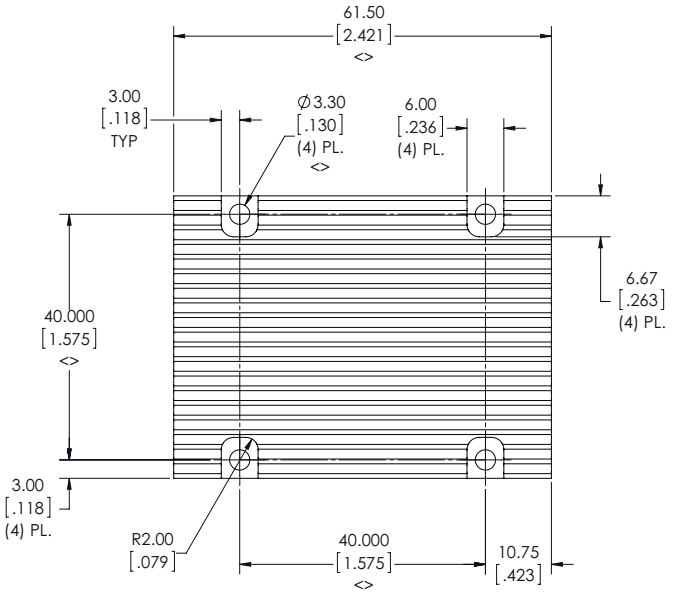
NOTES:

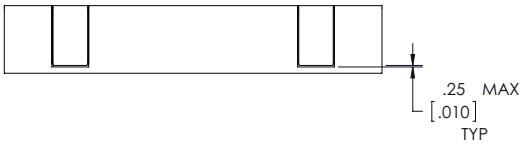
1- RoHS COMPLIANT PER CST-0001 LATEST REVISION.

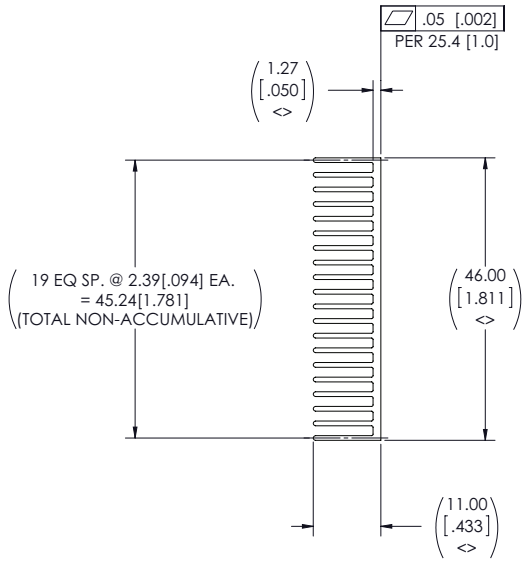


RECOMMENDED HOLE PATTERN (COMPONENT SIDE)

BCM Module Recommended Top Heat Sink Push Pin Location







NOTES:

1- MAKE FROM VICOR P/N 30827.

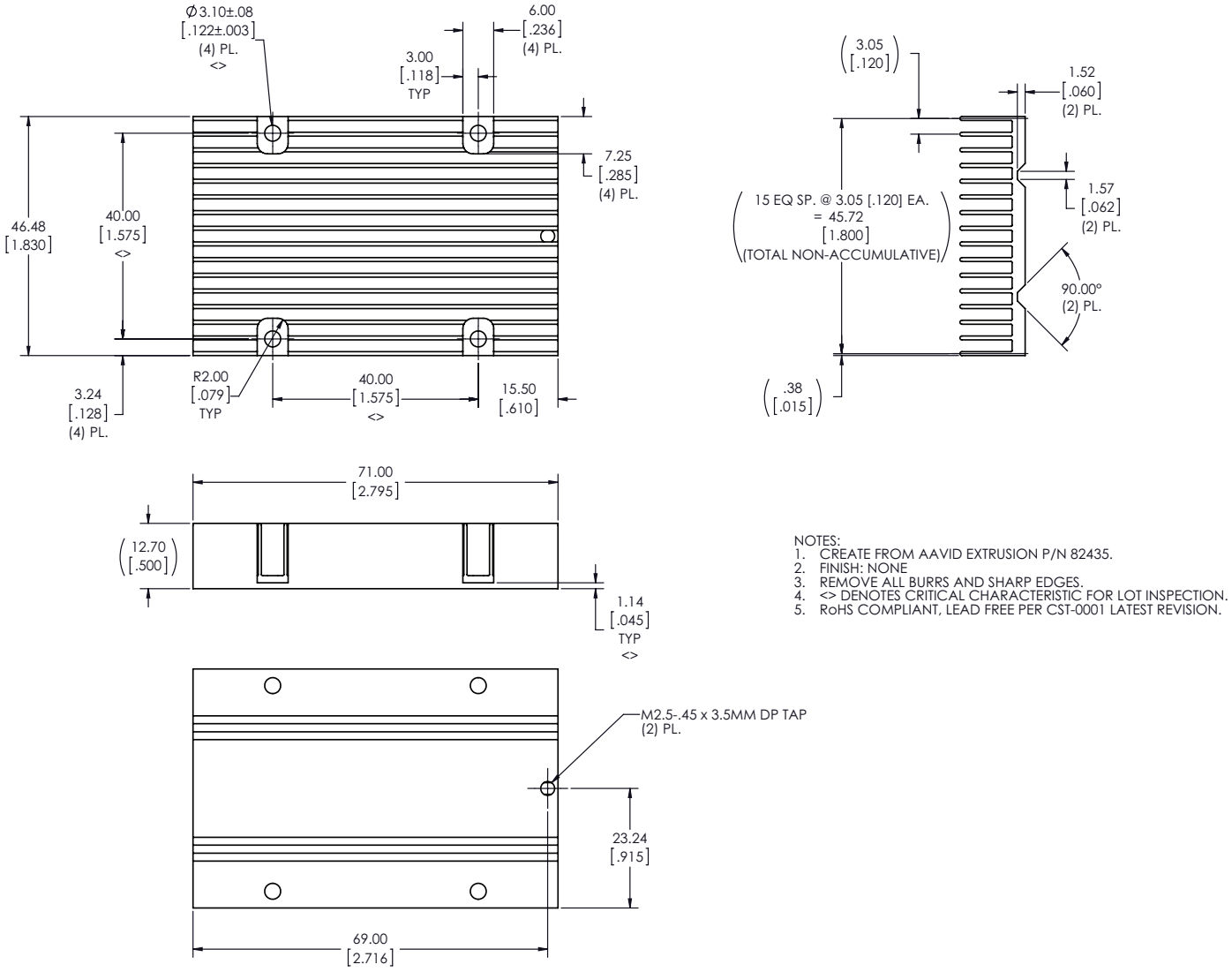
2- FINISH: CLEAR FINISH, RoHS COMPLIANT PER CST-0001, LATEST REVISION PER
A.) CHROMIUM FREE, OR
B.) TRIVALENT CHROMIUM IN ACCORDANCE WITH MIL-DTL-5541, TYPE II, CLASS 1A OR 3. SEE CST-0003 FOR TYPES OF AVAILABLE FINISHES.

3- REMOVE ALL BURRS AND SHARP EDGES.

4- <> DENOTES CRITICAL CHARACTERISTIC FOR LOT INSPECTION.

5- ROHS COMPLIANT, LEAD FREE PER CST-0001 LATEST REVISION.

BCM Module Recommended Bottom PCB Heat Sink Mounting Location



NOTES:
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2. FINISH: NONE
3. REMOVE ALL BURRS AND SHARP EDGES.
4. <> DENOTES CRITICAL CHARACTERISTIC FOR LOT INSPECTION.
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Vicor Corporation
25 Frontage Road
Andover, MA, USA 01810
Tel: 800-735-6200
Fax: 978-475-6715

email
Customer Service: custserv@vicorpower.com
Technical Support: apps@vicorpower.com