Single Stage Primary Side Regulation Flyback Controller with Active PFC for LED 4-Step Dimming and PWM Dimming

FEATURES

Excellent Compatibility and Performance

- Flickerless 4-Step Dimming and PWM Dimming
- Primary Side Regulation (PSR)
- Constant Current output (+/- 1.5%)
- Universal Input Voltage Range (85V – 265V)

Energy Efficient

- Boundary Conduction Mode (BCM) with Valley Switching reduces EMI and enhances Efficiency
- Power Factor Correction (PF > 0.95)
- High Efficiency (> 87%)
- Low Startup Current: 1.0μA
- Low Operating Current: 1.6mA
- Low Quiescent Current: 1.3mA

Advanced Protection and Safety Features

- Open and Short LED Protection
- Cycle by Cycle Current Limit
- VCC Over Voltage Protection (OVP)
- VCC Under Voltage Lockout (UVLO)
- Over Temperature Protection (OTP)

Package

- SOP-8 Package Available

DESCRIPTION

The offline primary side control LED lighting controller, SE8326, provides accurate output current, high power factor and low total harmonic distortion. High efficiency is achieved by low operating current and valley turn-on of the primary MOSFET. Constant on-time control is utilized for a better PFC performance, and DCM provides a lower output dimming current.

Two kinds of 4-Step Dimming are provided by SE8326. PWM Dimming can also be adopted.

The multi-protection of SE8326, including open LED protection, short LED protection, cycle by cycle current limit, VCC UVLO and over temperature protection can greatly enhance the system reliability. Current limit threshold is adjusted automatically in a low output condition not only ensures a soft start, but also minimizes the output current when LED is shorted.

APPLICATIONS

- Isolated LED Driver with 4-Step Dimming
- Isolated LED Driver with PWM Dimming

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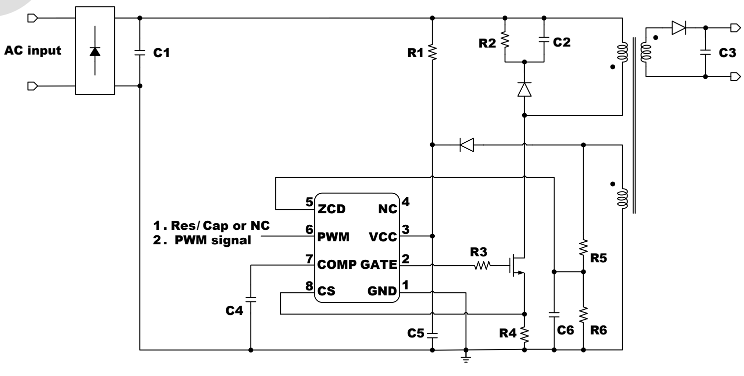

Figure 1. Typical Application

FUNCTIONAL BLOCK DIAGRAM

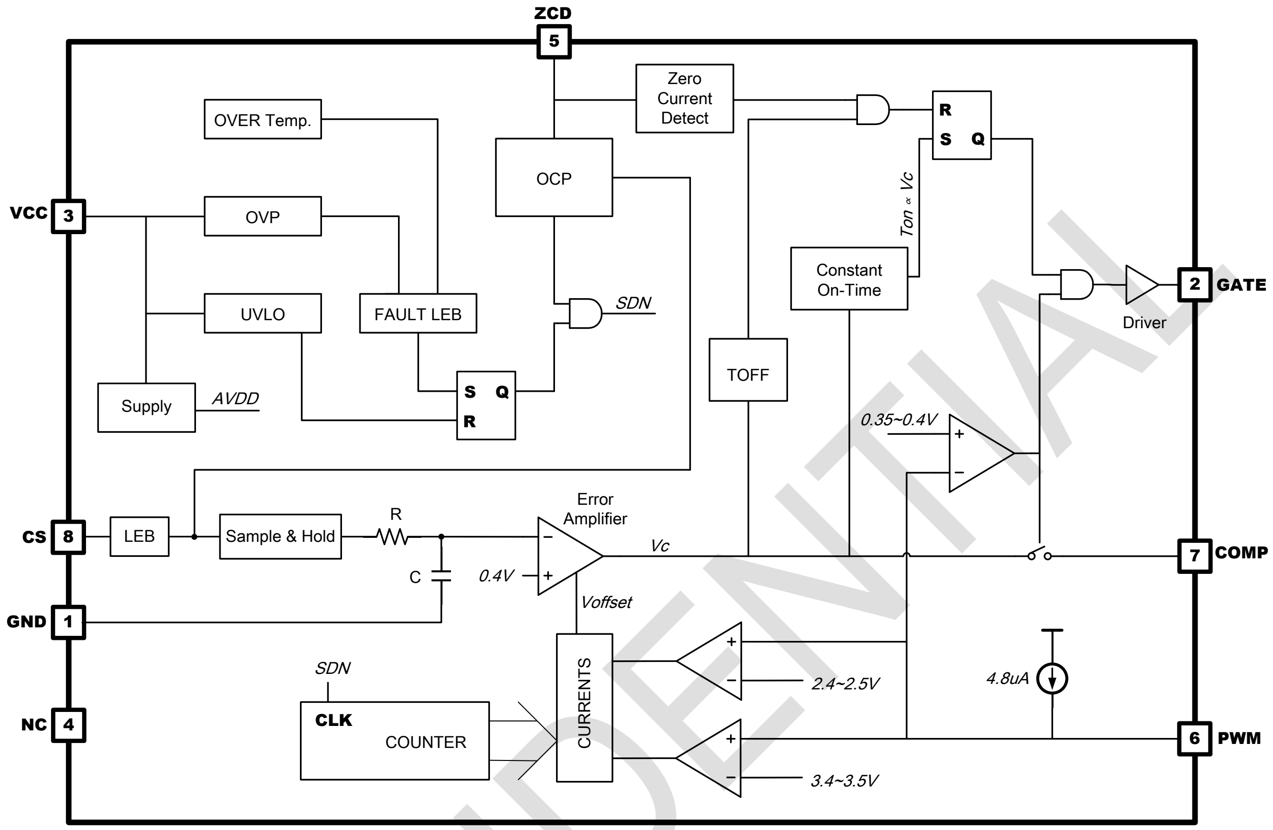

Figure 2. Functional Block Diagram

PIN FUNCTIONS

Pin #	Name	Description
1	GND	Ground.
2	GATE	Gate drive output pin. The totem pole output stage is able to drive high power MOSFET.
3	VCC	Power supply pin. This pin supply power both for IC operating current and GATE driving current.
4	NC	Not connected.
5	ZCD	Zero current detection pin. Connect this pin through a resistor divider from the auxiliary winding to GND in order to detect the inductor current zero crossing point. This pin also detects the output voltage for OCP.
6	PWM	Dimming mode choosing and PWM signal input.
7	COMP	Loop Compensation pin. Connect a compensation network to stabilize the loop.
8	CS	Current sense pin. The MOSFET current is sensed via a resistor for constant current regulation and cycle-to-cycle current limit.

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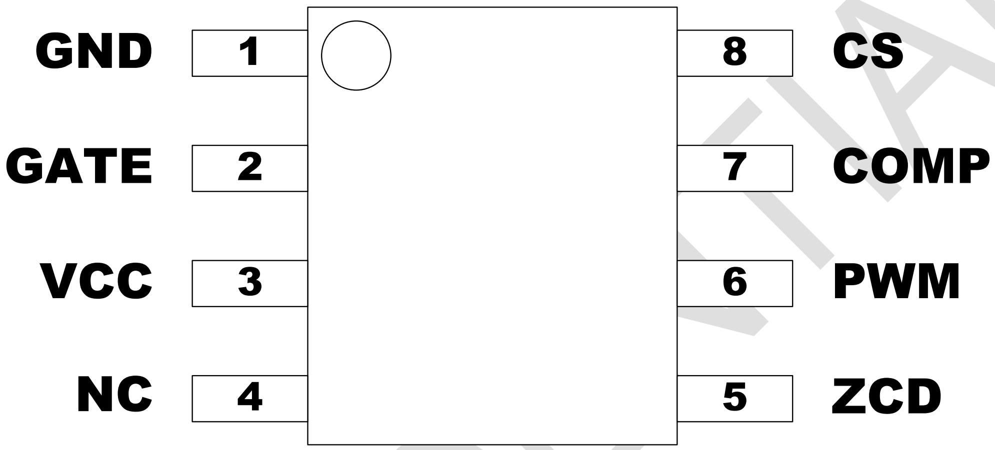
ORDERING INFORMATION

ORDERING NUMBER	PINS	PACKAGE
SE8326-SO-L	8	SOP-8

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
GATE Pin Input Voltage	V_{GATE}	-0.3 to 30.0	V
Power Supply Voltage	V_{CC}	<30	V
ZCD Pin Input Voltage	V_{ZCD}	-0.3 to 7.0	V
PWM Pin Input Voltage	V_{PWM}	-0.3 to 7.0	V
COMP Pin Input Voltage	V_{COMP}	-0.3 to 7.0	V
CS Pin Input Voltage	V_{CS}	-0.3 to 7.0	V
Maximum Junction Temperature	T_J	<150	°C
Storage Temperature	T_{STG}	-55 to 150	°C
Lead Temperature (Soldering, 10s)	T_{Lead}	<260	°C

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ELECTRICAL CHARACTERISTICS

V_{CC}=20V, T_A=+27°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SUPPLY SECTION (T_A = -40°C to 125°C)						
V_{CC}	Operating Range		9		24	V
V_{CC-ON}	Turn-On Threshold Voltage		14	16	18	V
V_{CC-OFF}	Turn-Off Threshold Voltage		7	8	9	V
V_{CC-HYS}	V_{CC} Hysteretic Voltage		7	8	9	V
I_{CC}	Operating Current	Switch Period = 15μs	1.0	1.6	2.2	mA
I_Q	Quiescent Current	No switch	1.0	1.4	1.9	mA
I_{ST}	Startup Current	V_{CC} = V_{CC-ON} - 0.16V	1.1	1.1	1.8	μA
V_{CLAMP}	V_{CC} Over-Voltage-Protection		22	26	30	V
CONSTANT ON-TIME SECTION (T_A = -40°C to 125°C)						
T_{ON-MIN}	Minimum On Time			400		ns
T_{ON-MAX}	Maximum On Time		18	23	28	μs
DCM SECTION (T_A = -40°C to 125°C)						
$T_{OFF-MIN}$	Minimum Off Time		40	50	60	μs
ERROR AMPPLIFIER SECTION						
G_M	Transconductance			120		μA/V
A_{EA}	Voltage Gain			9000		V/V
V_{COMP}	COMP Voltage Range		0.9		3.4	V
$I_{C-SOURCE}$	Max Source Current		35	48	65	μA
I_{C-SINK}	Max Sink Current		-220	-290	-360	μA
GATE DRIVER SECTION (T_A = -40°C to 125°C)						
V_{CLAMP}	Output Clamp Voltage		11	13.5	14	V
$I_{G-SOURCE}$	Max Source Current		0.97	1.2	1.4	A
I_{G-SINK}	Max Sink Current		-1.2	-1.7	-2.1	A
ZERO CURRENT DETECTOR SECTION						
V_{ZCD}	ZCD Threshold			0.4		V
V_{ZCD_HYS}	ZCD Hysteresis			0.5		V
$T_{OFF-MIN}$	Minimum Off Time			3.6		μs
AUTO START SECTION						
T_{START}	Auto Start Time	-40°C < T_A < 125°C	100	135	190	μs

Continued on the following page...

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ELECTRICAL CHARACTERISTICS

V_{CC}=20V, T_A=+27°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
OVER-CURRENT PROTECTION SECTION						
V_{OCP-H}	CS High Threshold Voltage for OCP			2.5		V
V_{OCP-L}	CS Low Threshold Voltage for OCP			1		V
$V_{HOCP-EN}$	ZCD Threshold Voltage to Enable High OCP level			0.9		V
$V_{LOCP-EN}$	ZCD Threshold Voltage to Enable Low OCP level			0.6		V
T_{LEB}	CS Sampling Leading-Edge Blanking Time			215		ns
OVER-VOLTAGE PROTECTION SECTION						
V_{OVP}	OVP Threshold Voltage			4.4		V
V_{OVP_HYS}	OVP Hysteresis Voltage			0.6		V
SHORT-CURRENT PROTECTION SECTION						
V_{SCP}	SCP Threshold Voltage			4.4		V
V_{SCP_HYS}	SCP Hysteresis Voltage			0.6		V
OVER TEMPERATURE PROTECTION SECTION						
T_{OTP}	Over Temperature Protection		140	150	160	°C
$T_{OTP-HYS}$	OTP Hysteresis		22	25	28	°C
4-LEVEL SWITCH DIMMING SECTION						
V_{DIM_H}	Maximum V_{LD} at Low Brightness		10	11.5	13	V
V_{DIM_L}	Maximum V_{LD} at High Brightness		4	5	6	V
I_{DIM}	V_{LD} vs. $V_{EA-OFFSET}$ Slope at High Brightness			60		μA
V_{EN}	Enable Voltage on PWM pin			2.5		V
I_{PWM}	PWM pin output current			4		μA

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FUNCTIONAL DESCRIPTION

SE8326 is a 4-Level Switch and PWM dimmable single stage Flyback and PFC controller for LED lighting applications. Primary side control is applied so that the system is simplified, and high power factor is achieved by constant on-time model. Boundary Conduction Mode (BCM) with valley switching improves efficiency and EMI performance. The multi-protection function stabilizes system and protects external components.

Startup

The capacitor C_{ST} across V_{BUS} and GND is charged by BUS through a start up resistor R_{ST} once BUS is powered on. After V_{CC} rises up to $V_{CC\text{-}ON}$, the internal blocks start to work and the gate driver begins to switch. Then V_{CC} will be pulled down by internal consumption until the power supply is taken over by the auxiliary winding.

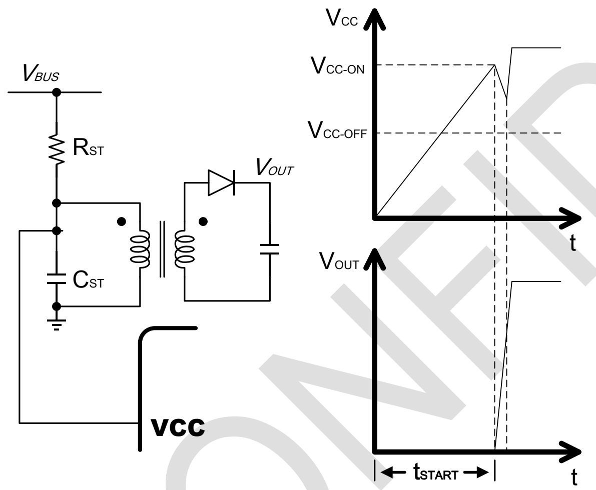

Figure 3. Startup Sequence

In order that V can rise when start up, and fall when OVP and OTP, R_{ST} should be preset following this:

$$\frac{V_{BUS}}{I_Q} < R_{ST} < \frac{V_{BUS}}{I_{ST}}$$

Select C_{ST} for an ideal t_{ST}:

$$t_{ST} = \frac{C_{ST}V_{BUS}}{\frac{V_{BUS}}{R_{ST}} - I_{ST}}$$

For a more stable V_{CC}, a bigger C_{ST} is needed, and R_{ST} should be decreased in order that t_{ST} is not changed. Obviously, the low I_{ST} of SE8326 makes it easier to design R_{ST}.

BCM Operation

Boundary Conduction Mode (BCM) and valley switching provides low turn-on switching losses.

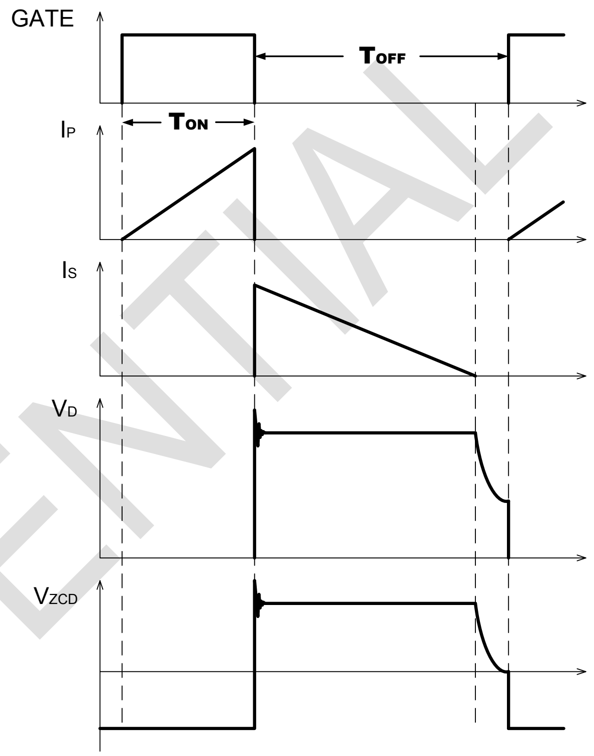

Figure 4. Boundary Conduction Mode

The voltage across drain and source of the external MOSFET is detected by the ZCD pin. The current of the inductor begins to decrease linearly as soon as the external MOSFET is turned off. When the current falls to zero, the MOSFET Drain-Source Voltage decreases, which is also detected by the ZCD pin through a resistor divider. The external MOSFET would be turned on by a turn on signal sent by the Zero Current Detector once the ZCD voltage is lower than 0.4V.

DCM Operation

Discontinuous Conduction Mode (DCM) is applied when COMP voltage is low. DCM can reduce the duty cycle down to less than 1%, and consequently a lower output current is obtained.

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FUNCTIONAL DESCRIPTION

Primary Side Constant Current Control

The output mean current can be represented as

$$I_{OUT} = \frac{N \times 0.4V}{2R_{CS}}$$

N—The winding turns ratio of primary side to secondary side of the transformer.
R_{CS}—The current sense resistor connected between the CS pin and GND.

Power Factor Correction

Internal Constant On-Time Block affords a constant gate on-time T_{ON}, which is in proportion to COMP potential. The peak current of the primary side winding is

$$I_P = \frac{T_{ON} V_{BUS}}{L_P}$$

L_P—The primary inductance.
As L_P and T_{ON} is constant, I_P is accordingly in proportion to V_{BUS} (as shown in Figure 5).

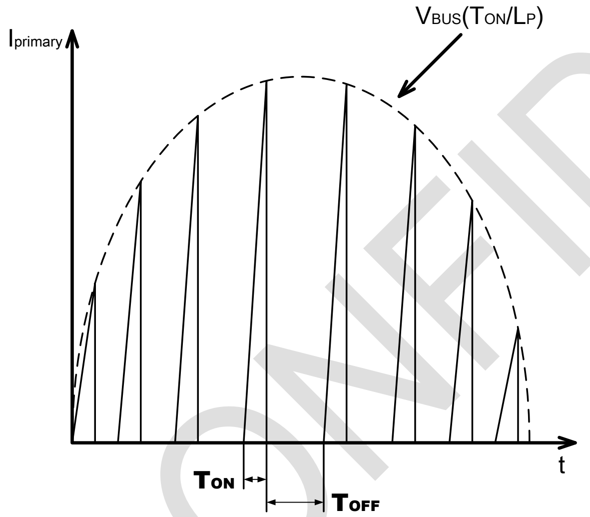

Figure 5. Power Factor Correction

As a result, the input current I_{IN} of the system follows the input voltage V_{IN}, and the Power Factor is improved.

4-Level Switch Dimming Control

SE8326 can implement 4-Level Switch Dimming function by internal dimming block and the external light switch. Figure 6 shows how 4-Level Switch Dimming works.
The first time switch turns on, the LED brightness is 100%. The brightness levels are traversed in an on-off manner if and only if the switch off time is less than T_{DIM}. Once the off time is larger than T_{DIM}, then the brightness would be reset to 100%.
Different PWM pin settings choose different 4-Level Switch Dimming mods:
1. A 1nF cap connected to PWM pin chooses 100%, 50%, 20%, 5% and then back to 100% mod.
2. A 750k res connected to PWM pin chooses 100%, 50%, 25%, 12.5% and then back to 100% mod.
3. Setting PWM voltage lower than 2.5V (for example, connect to GND or input a 0 to 2V PWM signal) can abandon 4-Level Switch Dimming.

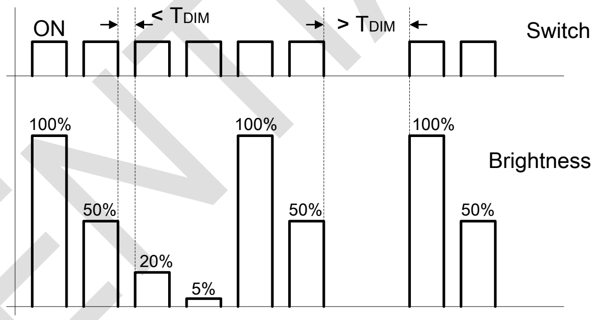

Figure 6. Dimming Function

VCC Under-Voltage Lockout (UVLO)

When the V_{CC} voltage drops below $V_{CC\text{-}OFF}$ (typically 8V), the whole chip shuts down, and GATE switching stops. The system would not work again until VCC capacitor is charged to $V_{CC\text{-}ON}$ through the external startup resistor.

Auto Start

A auto start block is integrated in SE8326 to avoid unnecessary shut down. The auto start block starts timing as soon as the external MOSFET turns on in every period. If the ZCD pin fails to send a turn on signal after T_{START} (typically 140μs), the auto start block would turn on GATE automatically.
When the GATE is turned on, auto start timing stops.

Minimum Off Time

To limit the maximum switching frequency and to obtain a better EMI performance, a internal block is integrated to limit the minimum GATE off time. The external MOSFET cannot turn on again in less than 3.6μs after its latest turning off.

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FUNCTIONAL DESCRIPTION

Leading Edge Blanking (LEB)

An internal leading edge blanking (LEB) block is employed in order to avoid the premature termination of the GATE switching pulse due to the peak voltage of the CS pin caused by the parasitic capacitor discharging when the external MOSFET turns on. V_{CS} sampling is disabled during the LEB time.

Open-LED Protection

When the load of the system is open, the output capacitor is charged up rapidly. As the voltage of the ZCD pin reflects the output voltage when the switch is on, the open-LED situation can be detected through the ZCD pin. Once ZCD voltage exceeds V_{OVP}, GATE would be shut down and the chip enters FAULT state, which would last until UVLO.

Cycle-by-Cycle Over-Current Protection

If the ZCD voltage in GATE on period is lower than 0.6V, the cycle-by-cycle current limit would be 1V. The current limit threshold voltage becomes up to 2.5V when the ZCD voltage in GATE on period is higher than 0.9V. Figure 6 shows this function. A lower OCP voltage can protect the external MOSFET as well as reduce power dissipation.

Short-Current Protection

No output signal is fed back to the chip when the load is short, and consequently COMP voltage will rise rapidly. The chip enters FAULT state as soon as COMP reaches V_{OVP} (typically 4.4V).

Over-Temperature Protection (OTP)

When the junction temperature is above 150°C, the chip enters FAULT state, and GATE driver is shut down. The UVLO signal can relive the system of FAULT state if the junction temperature drops below 125°C.

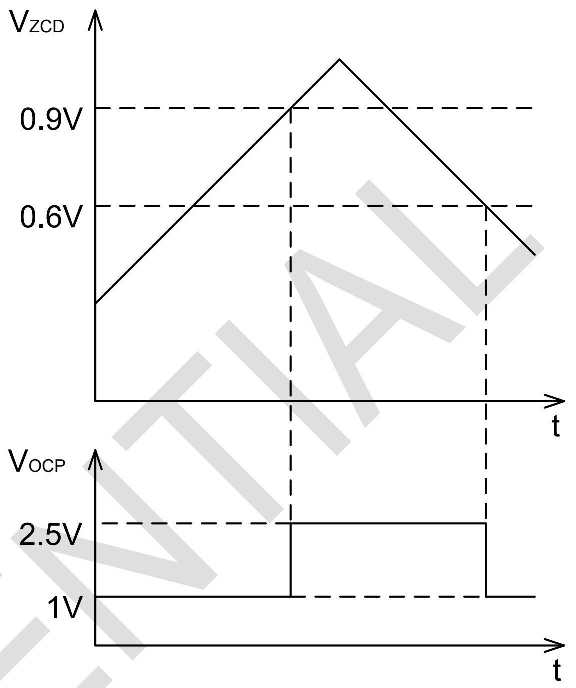

Figure 6. OCP Function

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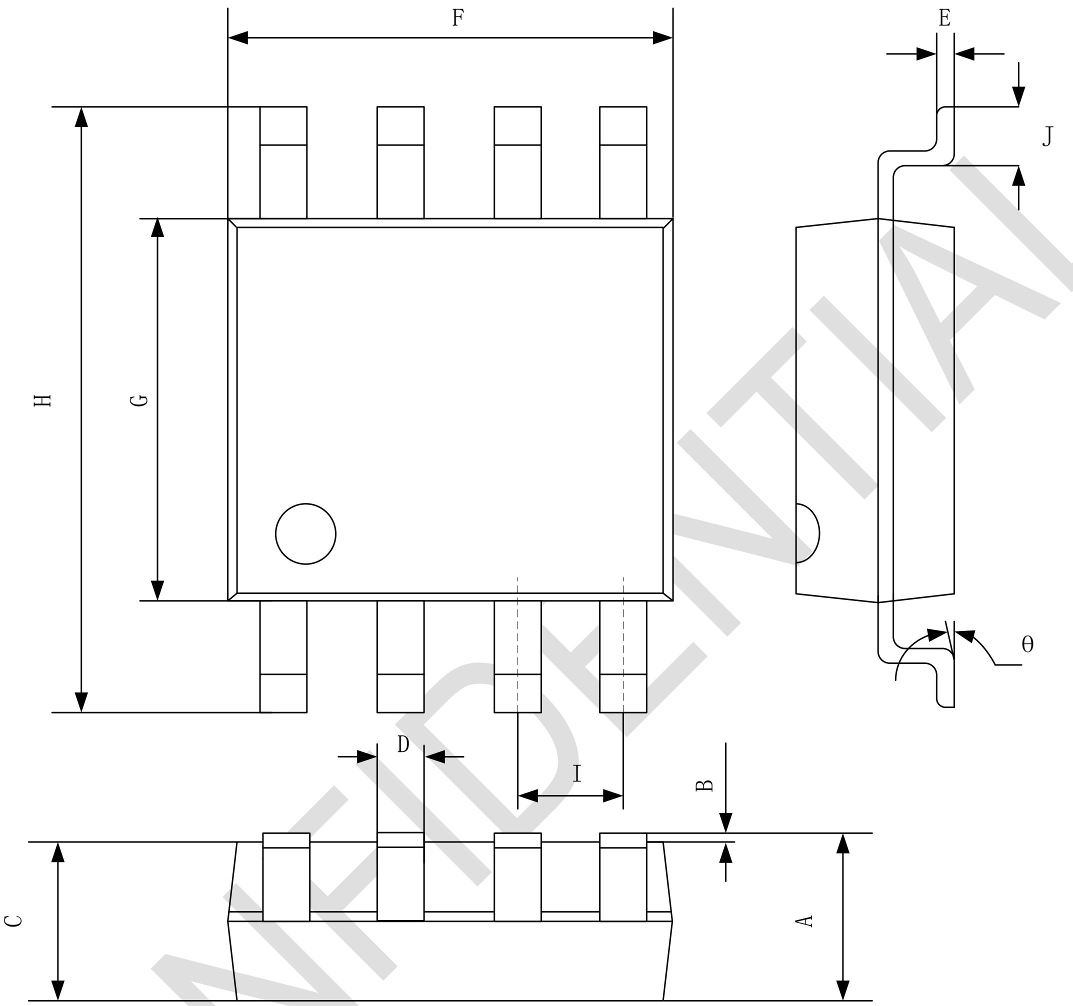
PACKAGE INFORMATION



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Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
B	0.100	0.250	0.004	0.010
C	1.350	1.550	0.053	0.061
D	0.330	0.510	0.013	0.020
E	0.170	0.250	0.006	0.010
F	4.700	5.100	0.185	0.200
G	3.800	4.000	0.150	0.157
H	5.800	6.200	0.228	0.244
I	1.270(BSC)		0.050(BSC)	
J	0.400	1.270	0.400	1.270
θ	0°	8°	0°	8°

SOLDERING INDICATION

This section gives a very brief insight to a complex technology. There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow Soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250°C. The top-surface temperature of the packages should preferable be kept below 220°C for thick/large packages, and below 235°C for small/thin packages.

Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used, the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch:
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis must be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250°C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

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Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320°C.

Suitability of Surface Mount IC Packages for Wave and Reflow Soldering Methods

Package	Soldering Method	
	Wave	Reflow (1)
BGA, HBGA, LFBGA, SQFP, TFBGA	Not suitable (2)	Suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	Not suitable	Suitable
PLCC (3), SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3)(4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

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Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect).
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch equal to or smaller than 0.5 mm.

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