



(Preliminary) MG20U202
Switching Regulator LED Driver

MG20U202

Data Sheet

Version: V0.30

Features

- Operation voltage, 7.0V ~ 200V
- Linear or PWM dimming control
- Open loop current peak detector
- Provide constant frequency or constant off-time control

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1 Description

The MG20U202 is a current feedback control, buck type LED driver IC. It achieves good output current regulation without the need of external compensation components.

The MG20U202 integrates a HV start-up circuit, 7.0V ~ 200V linear regulator, precision comparator, PWM control and ring oscillator into one chip. With those building circuits, a precision current output buck mode converter with dimming control (linear or PWM type) can be easily achieved with only few external components. The linear dimming control input is 0~0.25V and The PWM dimming range is 0~100% duty at a frequency of up to 10KHz.

The chip is available in 8-pin SOP package.

2 Order Information

| | |
|----------------|---------------------|
| | MG20U202ASC1 |
| Package | SOP8 |

3 Application Field

DC-DC LED driver application

Backlighting LED driver

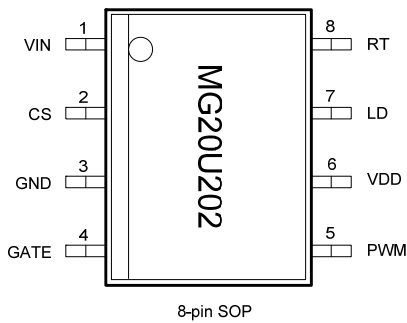
General-purpose constant current source

4 Pin Description

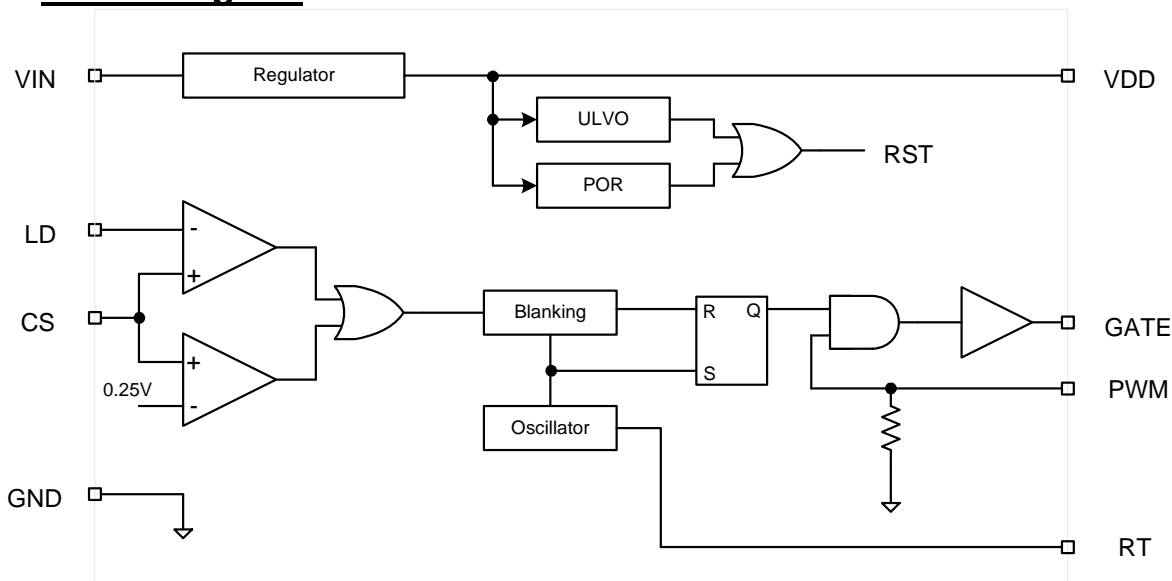
4.1 Pin Definition

| SOP8 | Pin Name | Description |
|------|----------|---|
| 1 | VIN | 7.0V ~ 200V high voltage input. |
| 2 | CS | Current sense input pin. |
| 3 | GND | Ground pin. |
| 4 | GATE | Driver for external power MOS. |
| 5 | PWM | PWM dimming input. |
| 6 | VDD | Regulated core supply. |
| 7 | LD | Linear dimming input. If current sense threshold is required less than 0.25V, an external voltage can be applied to this pin. |
| 8 | RT | Ring oscillator bias input. When RT is connected to ground via a resistor, the MG20U202 operates in constant frequency mode. When the resistor is connected between RT & GATE, the MG20U202 operates in constant off-time mode. |

4.2 Pin Configuration

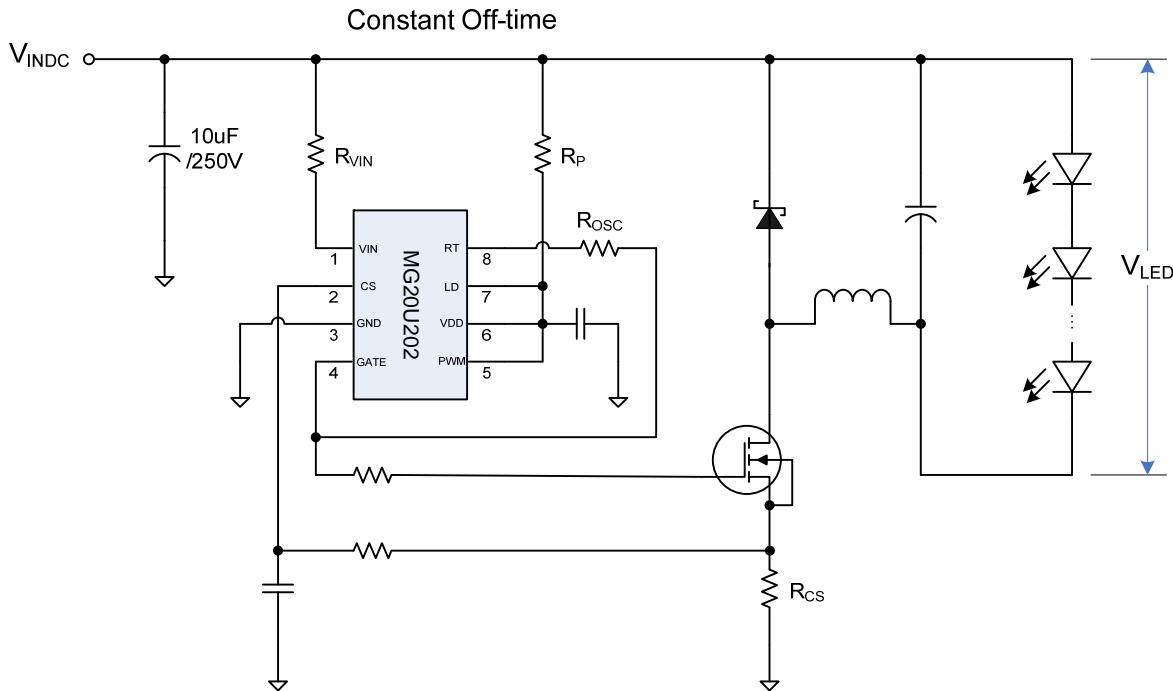


5 Block Diagram



6 Application Circuit

Buck Driver Example



7 Application Information

Input Voltage Regulator

The MG20U202 integrates one high voltage regulator to generate the power for internal core logic. The internal power is taken from the high voltage input directly. When a voltage (7~200V) is applied at the VIN pin, the regulator maintains a constant 5.6V at the VDD pin. The VDD pin must be bypassed by a low ESR capacitor to provide a low impedance path for the high frequency current of the output date driver.

Since the current driving capability of the regulator is limited to around 0.7mA. It's not suitable for driving the external components. User must make sure the switching frequency should not be too high and the load at the GATE pin should not be too heavy.

It's recommended to add a pull-high resistor (R_P) between V_{INDC} and VDD pin to provide more driving current for large I_{LED} application.

Selection of the Switching Control Scheme

The MG20U202 provides two control schemes, constant frequency and constant off time. For a buck converter, the duty of PWM control signal is determined as $D = V_O / V_{IN}$, where V_O is the voltage drop on LED strings (V_{LED}). For a heavy load application (large V_{LED} drop, $D > 0.45$), user should select the constant off time mode.

Selection of the Switching Frequency (F_s)

Rule of thumb, the range of 20KHz ~ 100KHz is recommended.

For detail frequency setting, please check design assistant file "MG20U202 DesignAssistantFileV1_0.xls".

GATE Output

The GATE output of the MG20U202 is used to drive an external MOSFET. It is recommended that the gate charge Q_G of the external MOSFET should satisfy the equation as below:

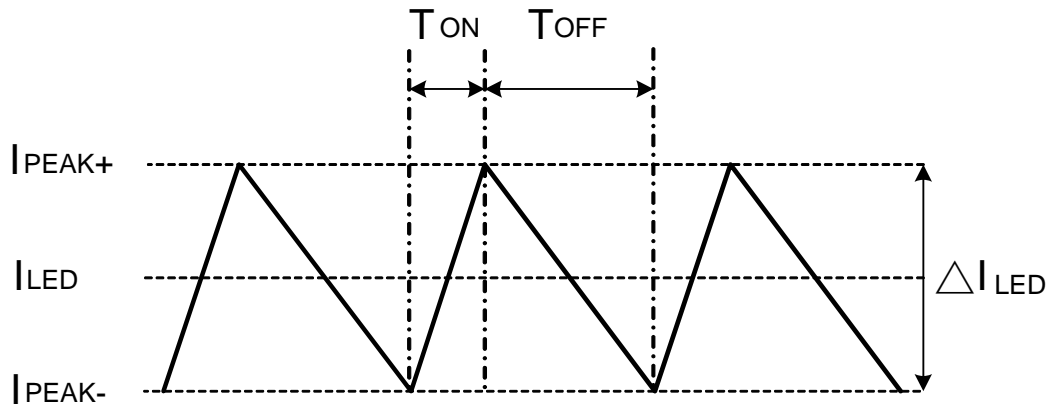
$$(V_{INDC} - 5.6V)/R_P + 0.7mA \geq F_s * Q_G$$

In the above equation, Q_G is the GATE charge of the external FET obtained from the manufacturer's datasheet.

Selection of the Sense Resistor (R_{CS})

The MG20U202 is an open loop buck converter with peak current control. The peak current is decided by the equation $I_{PEAK+} = V_{CSTH} / R_{CS}$, where V_{CSTH} is around 0.27V. The average current (I_{LED}) is described as follow:

The ΔI_{LED} is determined by T_{OFF} , L value and V_{LED} load.



8 Absolute Maximum Rating

| Parameter | Rating | Unit |
|------------------------------|---------------------------------|------|
| VIN to GND | -0.5 to +225 | V |
| VDD to GND | 7 | V |
| CS, LD, PWM, GATE, RT to GND | -0.3 to (V _{DD} + 0.3) | V |
| Junction Temperature | -40 to +125 | °C |
| Storage temperature | -55 to +155 | °C |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9 Electrical Characteristics

All typical numbers are at Ta=25°C and VIN=12V, unless otherwise noted.

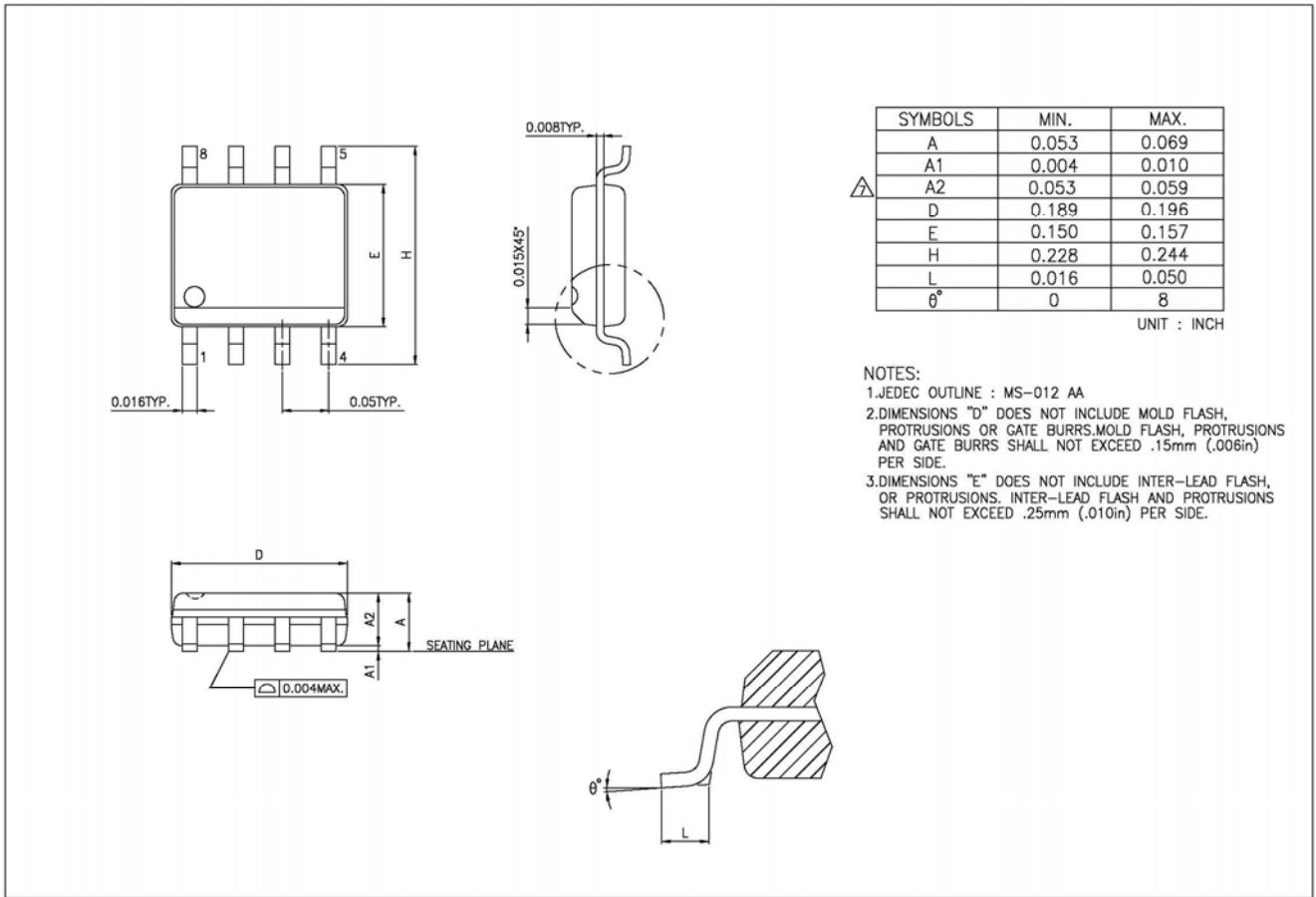
| Parameter | Sym. | Conditions | Min. | Typ. | Max. | Unit |
|---|---------------------|---|------|------|-------------------|------|
| Input DC supply voltage range | V _{INDC} | DC input voltage | 7.0 | - | 200 | V |
| Shut down mode supply current | I _{INSD} | PWM=0 | - | 0.5 | - | mA |
| Operating Current | I _{OP} | V _{IN} > 7.5V, R _{OSC} =226K and C _{GATE} =500P | - | 0.8 | 1.2 | mA |
| Internal Regulator | | | | | | |
| Internally regulated Voltage | V _{DD} | V _{IN} =7.5V ~ 200V, R _{OSC} =226K, C _{GATE} = 500pF, No load in pin VDD | 5.0 | 5.6 | 6.0 | V |
| Maximal pin VDD voltage | V _{DDMAX} | When an external voltage applied to pin VDD | - | - | 7.0 | V |
| Output current of the regulator | I _{SOURCE} | V _{DD} = 5.6V | - | 0.7 | - | mA |
| VDD under-voltage lockout threshold | V _{UVLO} | V _{IN} rising | - | 5.30 | - | V |
| VDD under-voltage lockout hysteresis | ΔUVLO | V _{IN} falling | 100 | 300 | 500 | mV |
| PWM Dimming | | | | | | |
| Pin PWM input high voltage | V _{PWM(H)} | V _{IN} =7.5V ~ 200V | 2.0 | - | - | V |
| Pin PWM input low voltage | V _{PWM(L)} | V _{IN} =7.5V ~ 200V | - | - | 0.8 | V |
| Pin PWM pull-down resistance | R _{PWM} | V _{DD} =5.5V | 50 | 100 | 150 | KΩ |
| PWM signal duty | D _{PWM} | | 0 | - | 100 | % |
| Current Sense Input | | | | | | |
| Current sense pull-in threshold voltage | V _{CSTH} | Ta= 0°C to +125°C, V _{DD} = 5.6V | 255 | 275 | 285 | mV |
| | | Ta= -40°C, V _{DD} = 5.6V | 200 | - | - | mV |
| Offset voltage of comparator | V _{OS} | | -20 | - | 20 | mV |
| Linear dimming pin voltage range | V _{LD} | | 0 | - | V _{CSTH} | mV |

Electrical Characteristics (continued)

| | | | | | | |
|----------------------------------|-----------------------|--|----------------------|------|------|----|
| Current sense blanking interval | t_{BLANK} | $V_{\text{CS}}=0.55 V_{\text{LD}}, V_{\text{LD}}=V_{\text{DD}}$ | 150 | 215 | 285 | nS |
| Delay from CS trip to GATE IO | t_{DELAY} | $V_{\text{LD}}=V_{\text{DD}}, V_{\text{CS}}= V_{\text{CSTH}} +50\text{mV}$ after t_{BLANK} | - | - | 300 | nS |
| Gate Driver | | | | | | |
| GATE output high voltage | $V_{\text{GATE (H)}}$ | | $V_{\text{DD}} -0.4$ | - | - | V |
| GATE output low voltage | $V_{\text{GATE (L)}}$ | | - | - | 0.4 | V |
| GATE output high driving current | $I_{\text{GATE (H)}}$ | $V_{\text{GATE}}= V_{\text{DD}}-0.4\text{V}$ | - | 10 | - | mA |
| GATE output low sinking current | $I_{\text{GATE (L)}}$ | $V_{\text{GATE}}= 0.4\text{V}$ | - | 25 | - | mA |
| GATE output rise time | t_{RISE} | $C_{\text{GATE}} = 500\text{pF}$ | - | 30 | 50 | nS |
| GATE output fall time | t_{FALL} | $C_{\text{GATE}} = 500\text{pF}$ | - | 30 | 50 | nS |
| Oscillator | | | | | | |
| Oscillator frequency | F_{OSC} | $R_{\text{OSC}}= 1.0\text{M}\Omega$ | 22K | 27K | 32K | Hz |
| | | $R_{\text{OSC}}= 226\text{K}\Omega$ | 90K | 110K | 120K | |

10 Package Dimension

10.1 SOP8 Package Dimension



11 Revision History

| Rev | Descriptions | Date |
|-------|--|------------|
| V0.10 | Initial release. | 2013/01/05 |
| V0.20 | Modify the supply voltage range. | 2013/03/05 |
| V0.30 | Modify the application circuit and add gate output notification. | 2013/06/17 |