Vicor’s Bus Converter Module Analysis

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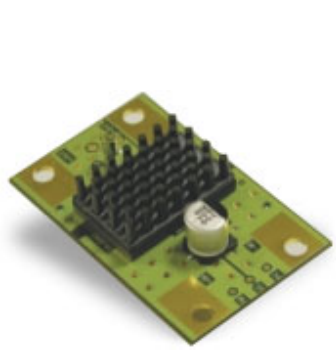
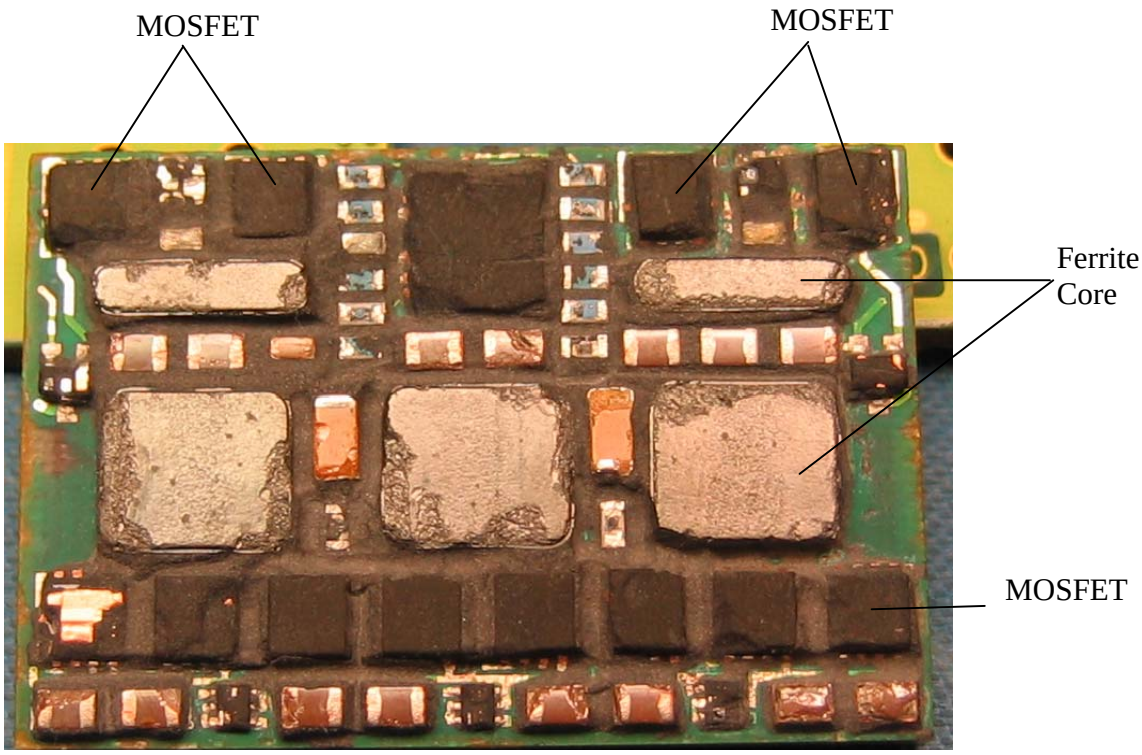
1. Outline:



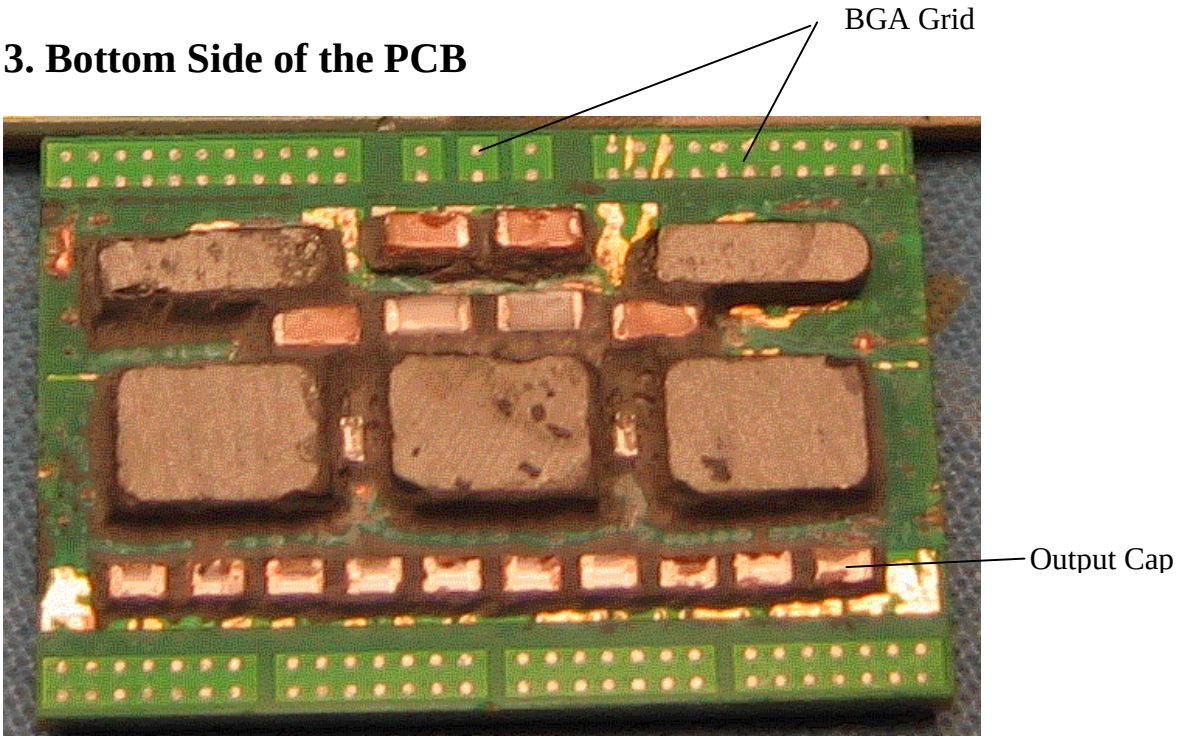
With Heatsink

Without Heatsink

2.Top side of the PCB



3. Bottom Side of the PCB

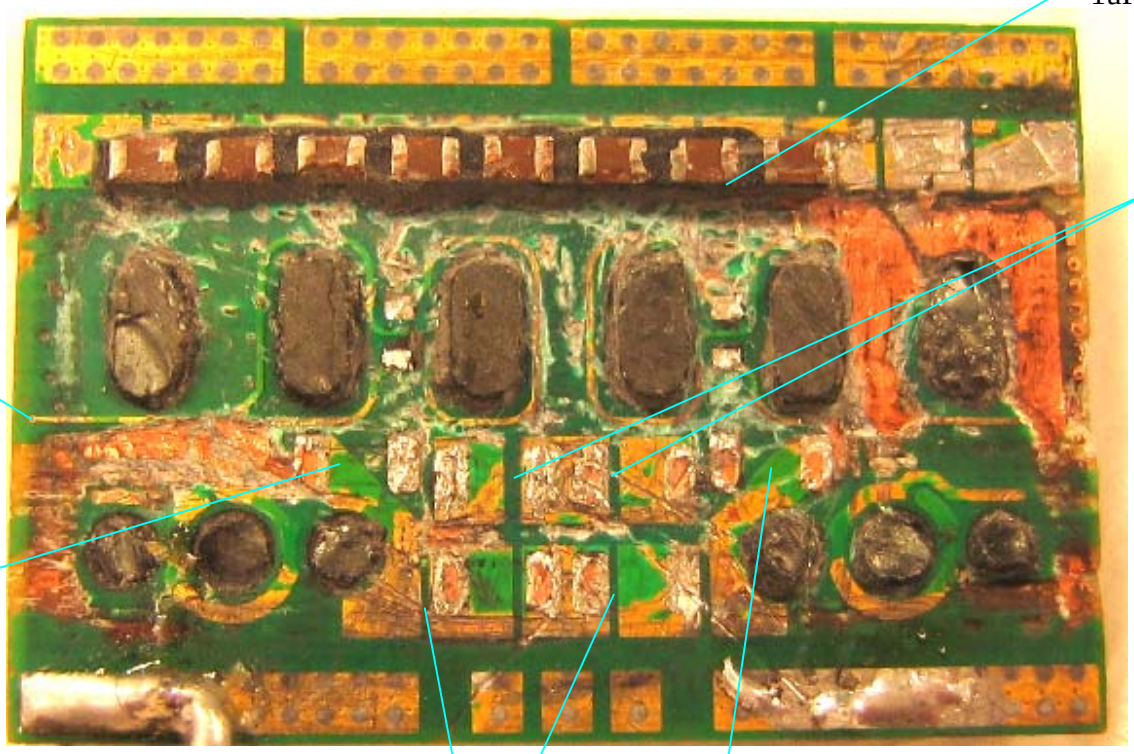


4. material filled

Proterty	Dielectric constant	Dissipation factor (tan d)	Electrical resistivity (O/cm)	Thermal conductivity W/mC	CTE (ppm/°C)
Material					
Silicon (Si)	12	-	10^5	125-150	2,5-4,5
Alumina	9-10	0,001	$>10^{14}$	20-40	6,5-7,2
AlN	8,5-10	-	$>10^{14}$	150-260	3,0-4,5
BeO	7-9	<0,001	$>10^{15}$	250-300	6,8-8,5
SiC	20-40	0,06	$>10^{14}$	100-270	3,0-4,6
Glass	6-7	0,005	$>10^{14}$	1,6-2,0	5-9
Glass-ceramic	5-9	0,0025	$>10^{13}$	1,0-2,5	3-7
Sealing-glass	11,5		$> 10^{12}$	0,6	6,3-7

It’s electricity non-conductivity thermal material.
Estimated: Silicon, Glass-ceramic mixed.

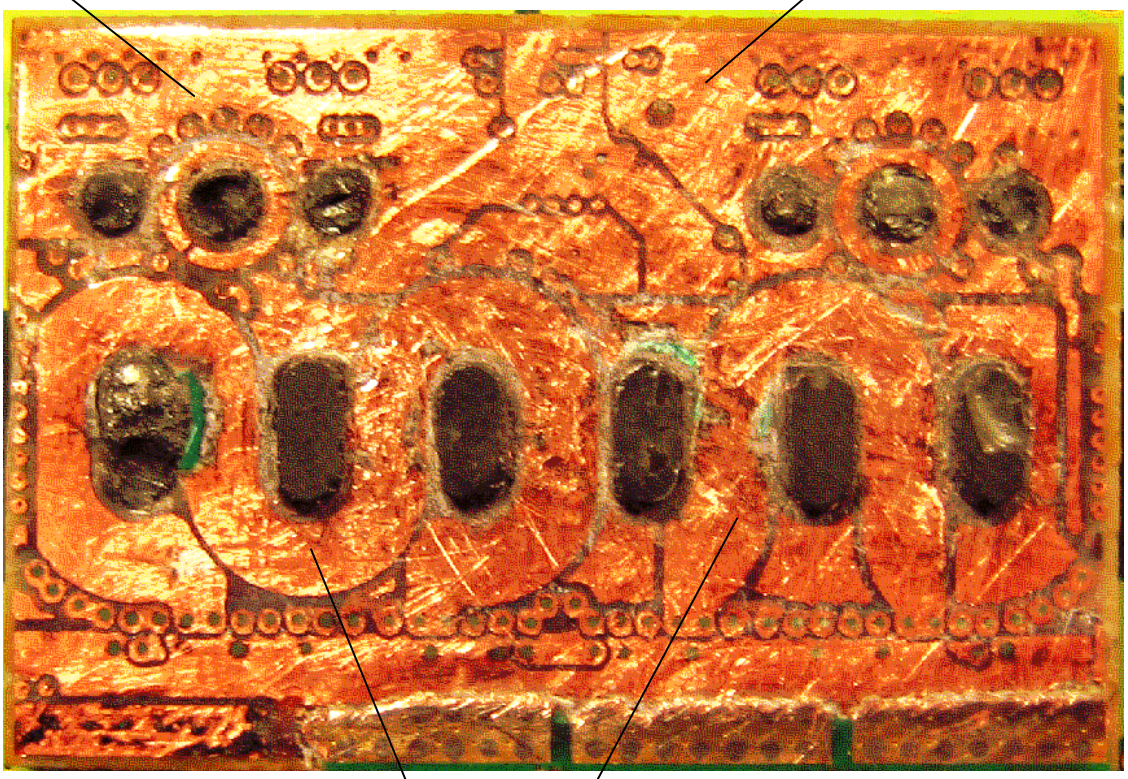
5. Pictures for all layes



Bottom layer

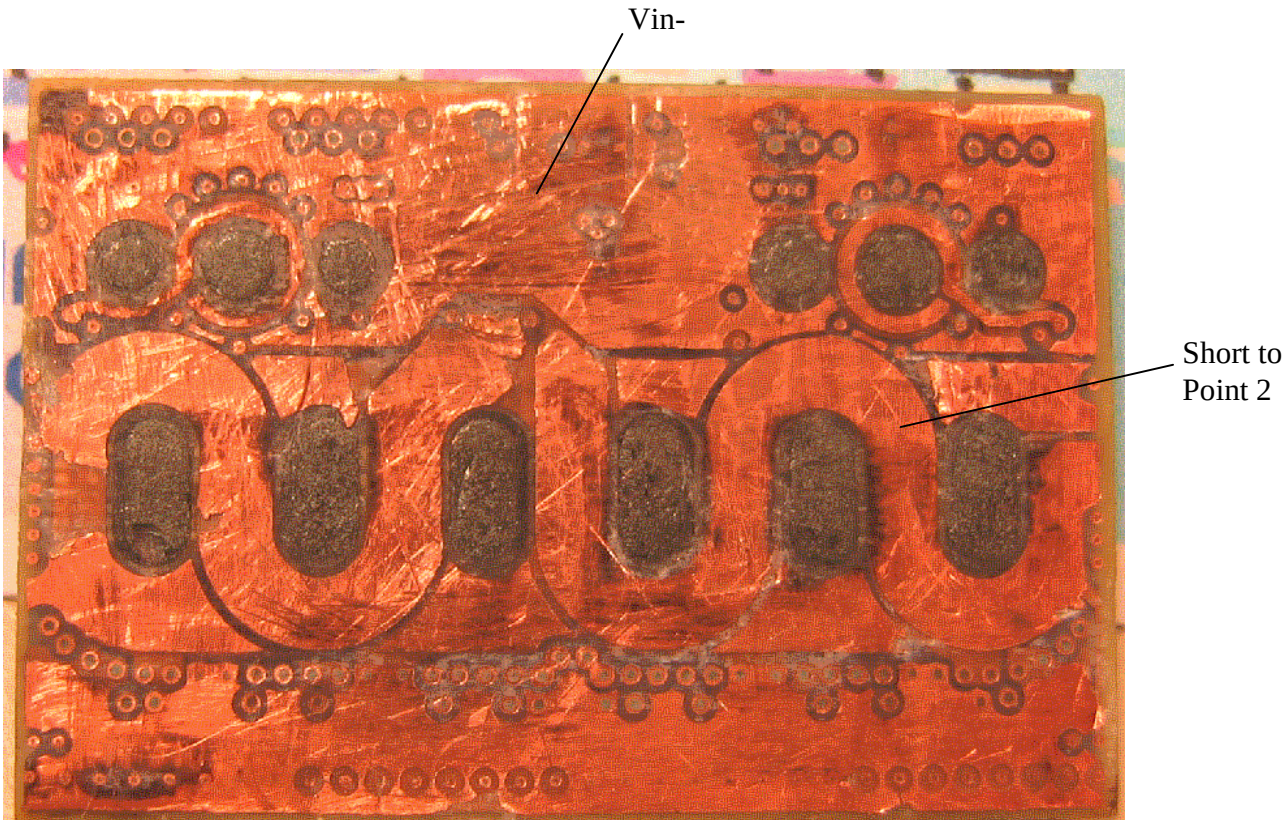
Vin+

Connected to point 2

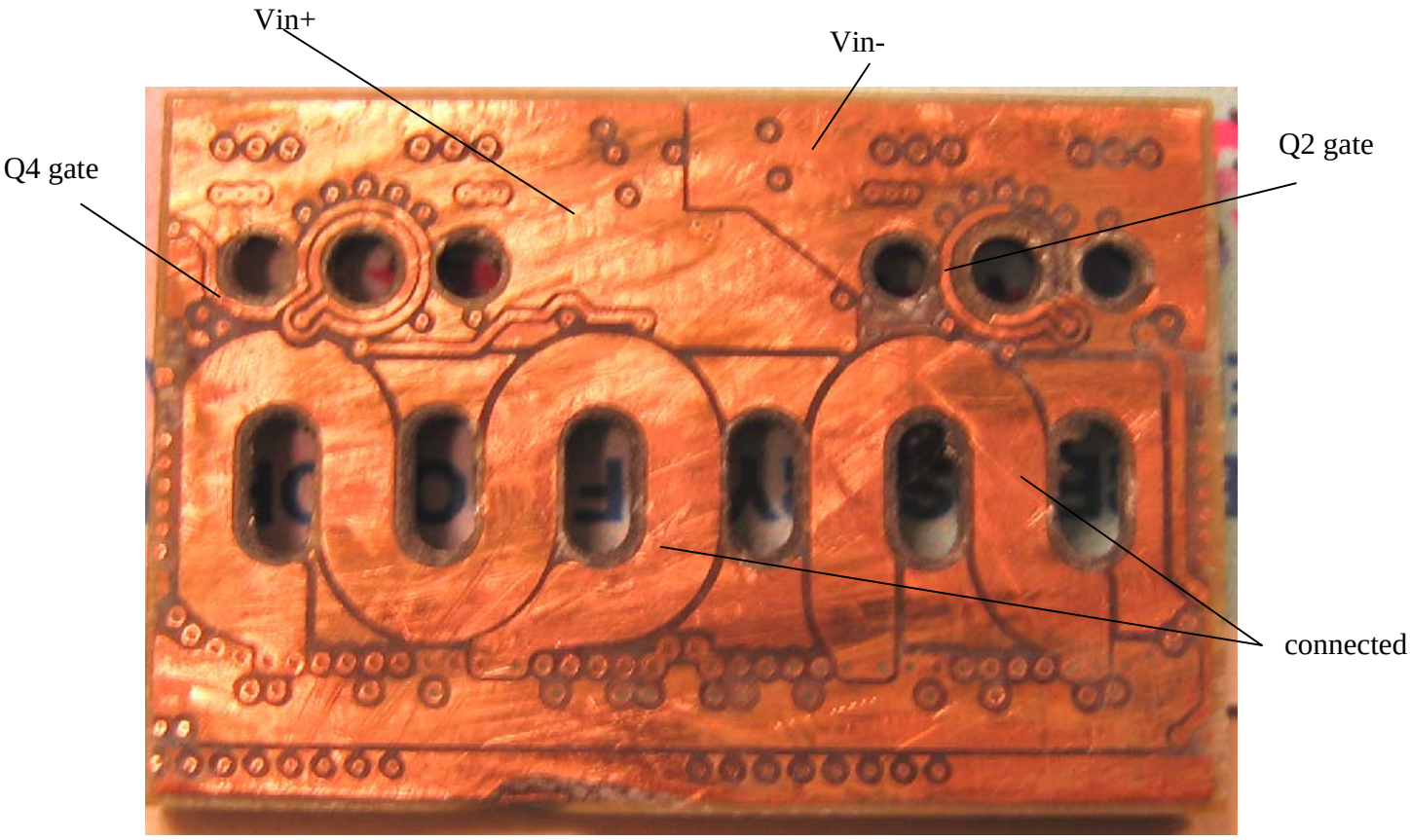


Short to Vout measured by multimeter

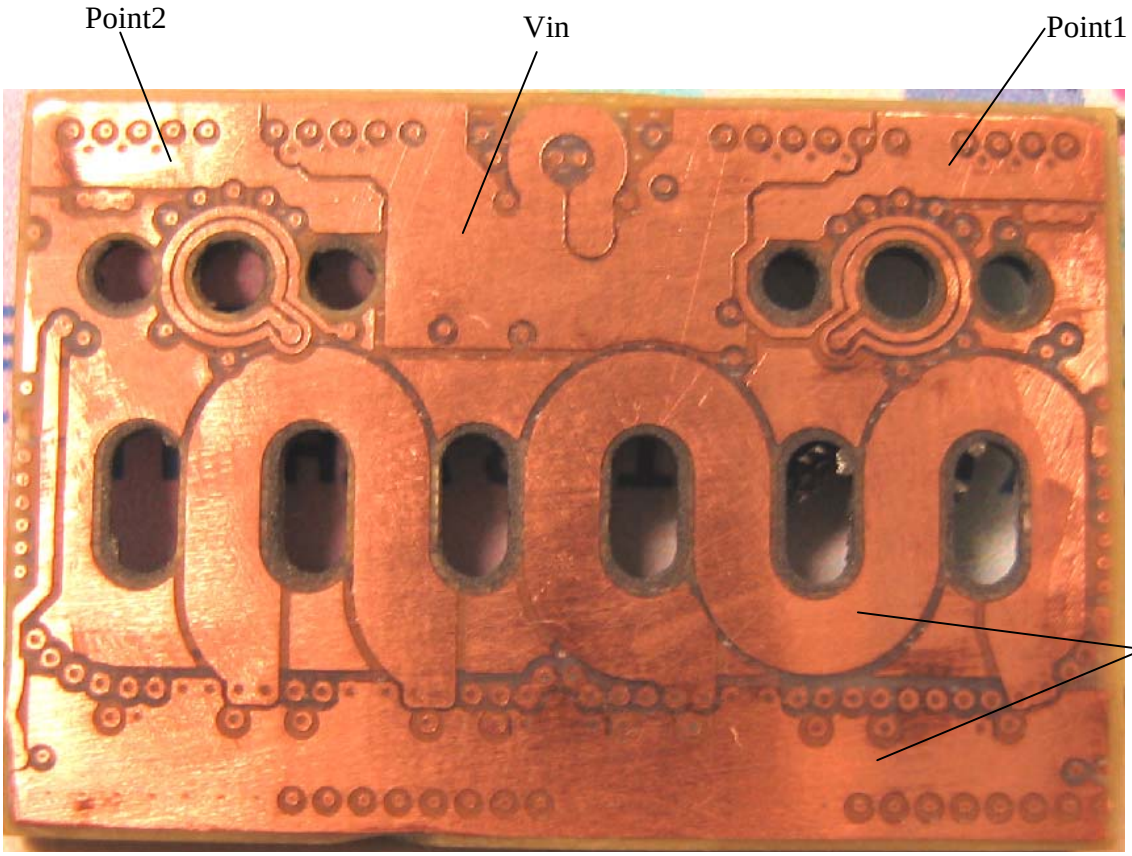
2nd layer(from botttom)



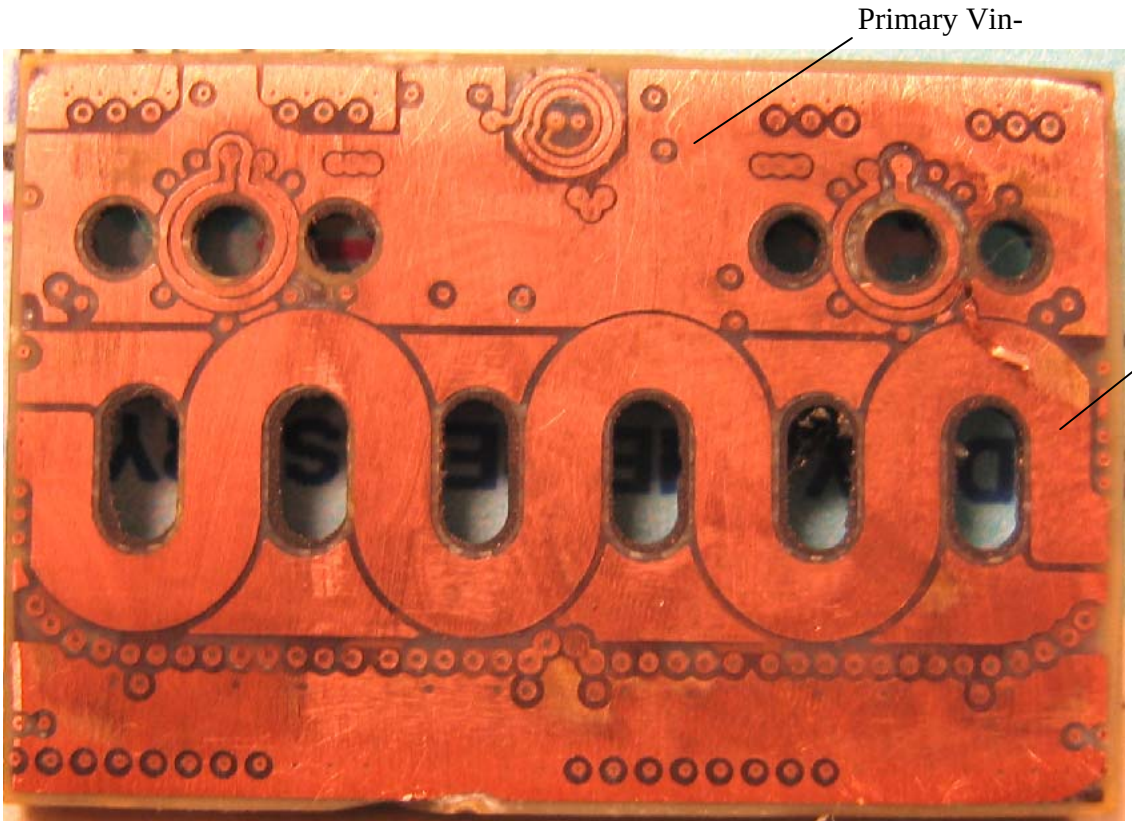
3th layer(from botttom)



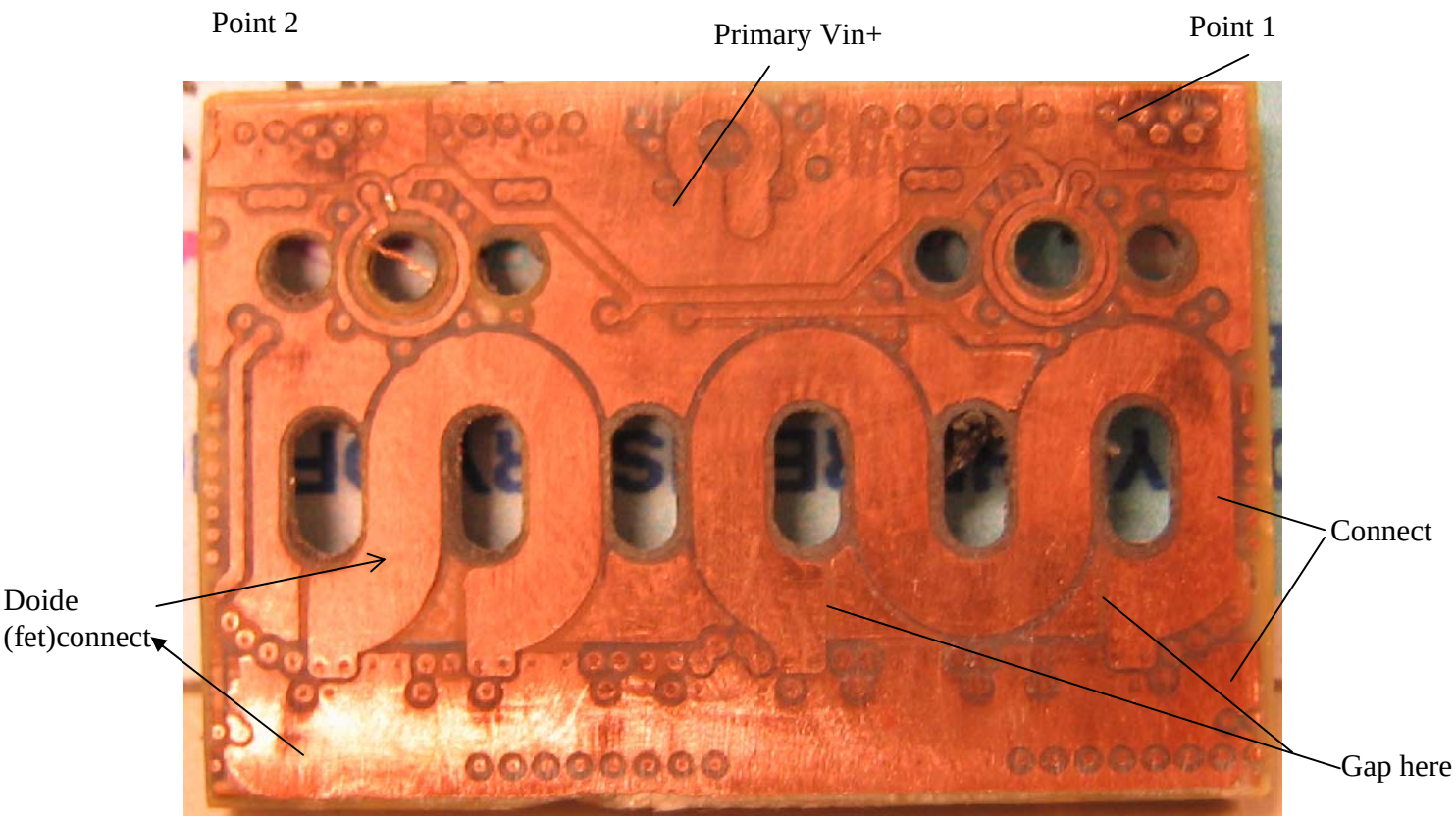
4th layer(from bottom)



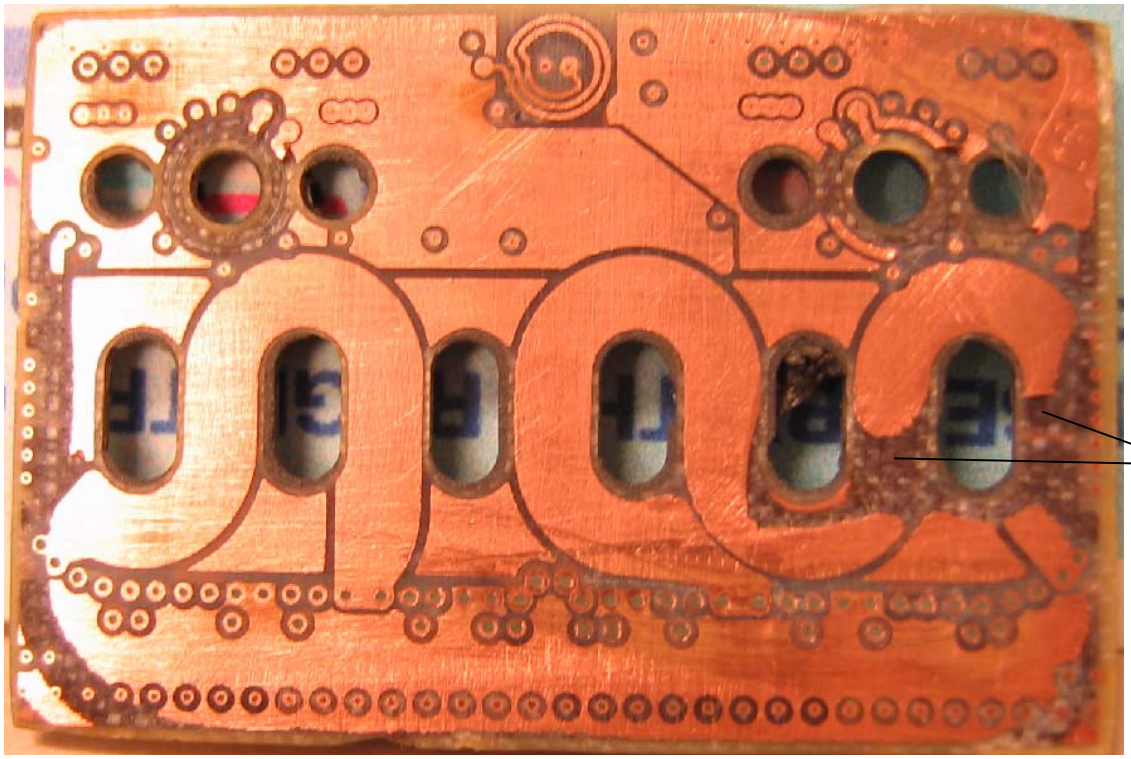
5th layer(from bottom)



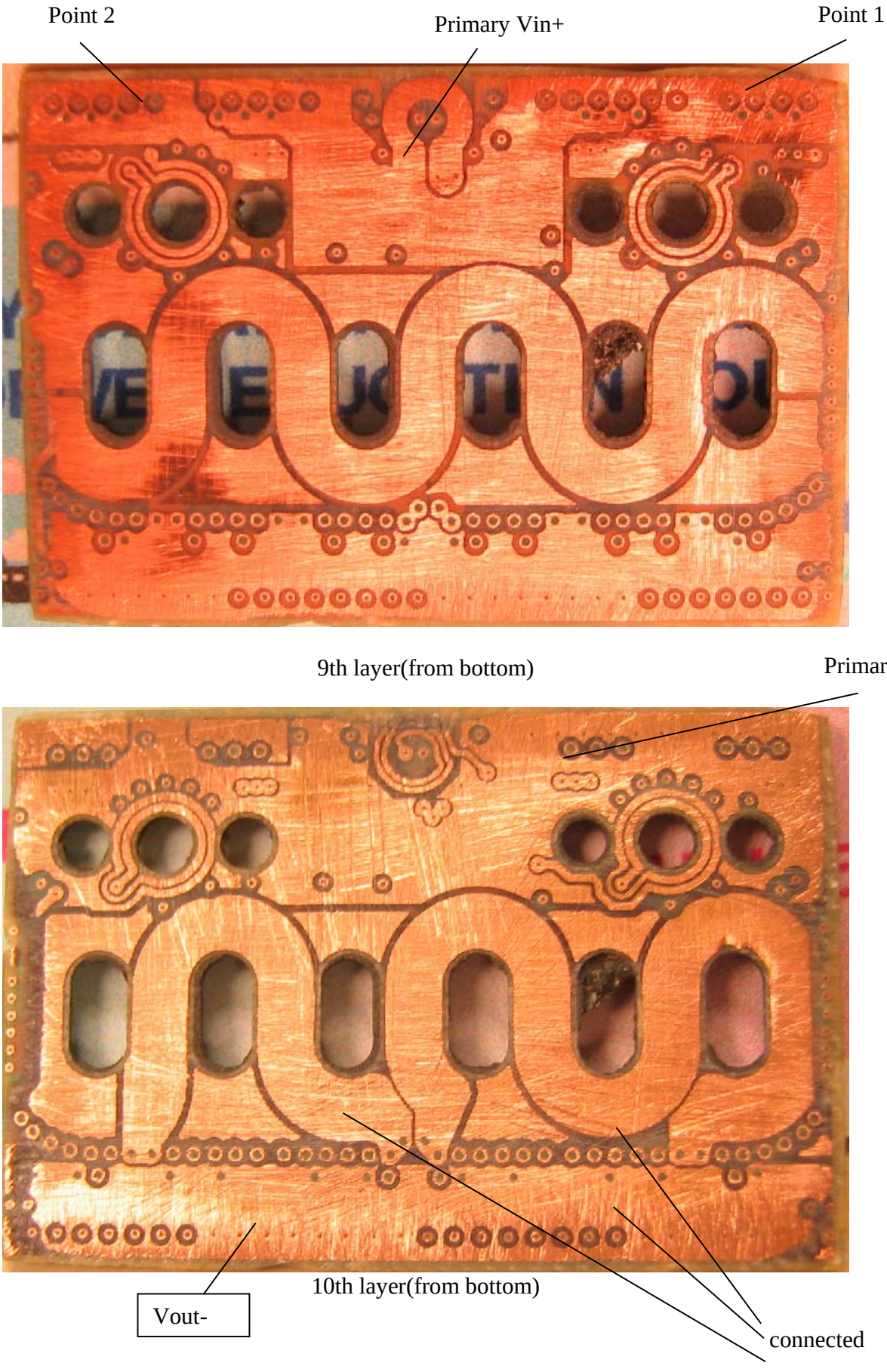
6th layer(from bottom)

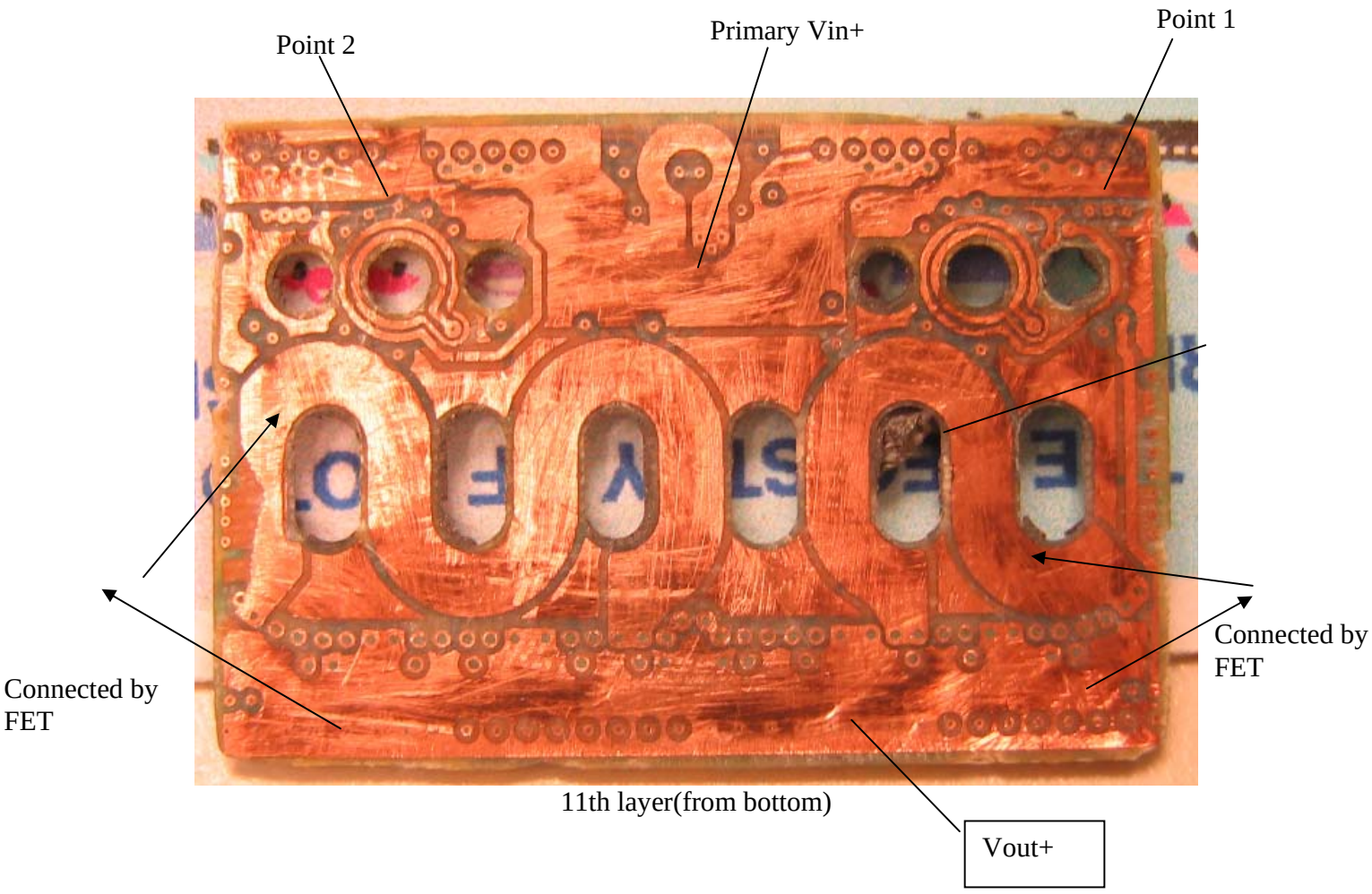


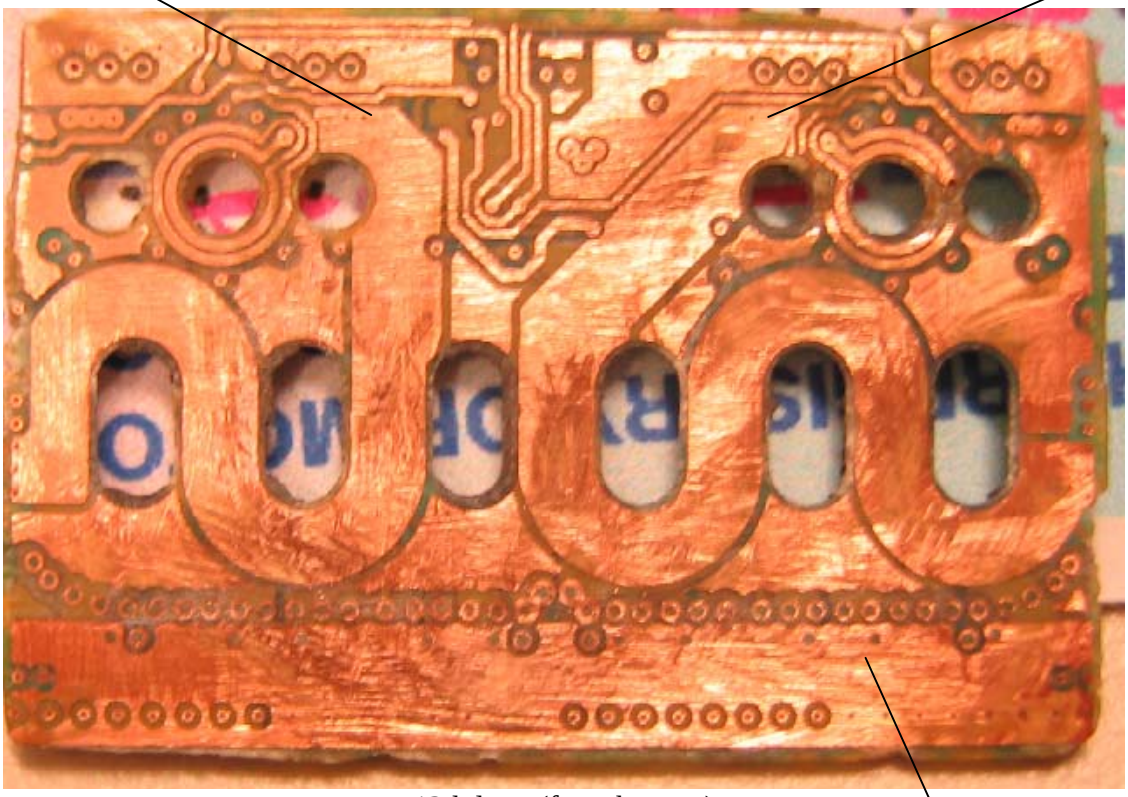
7th layer(from bottom)

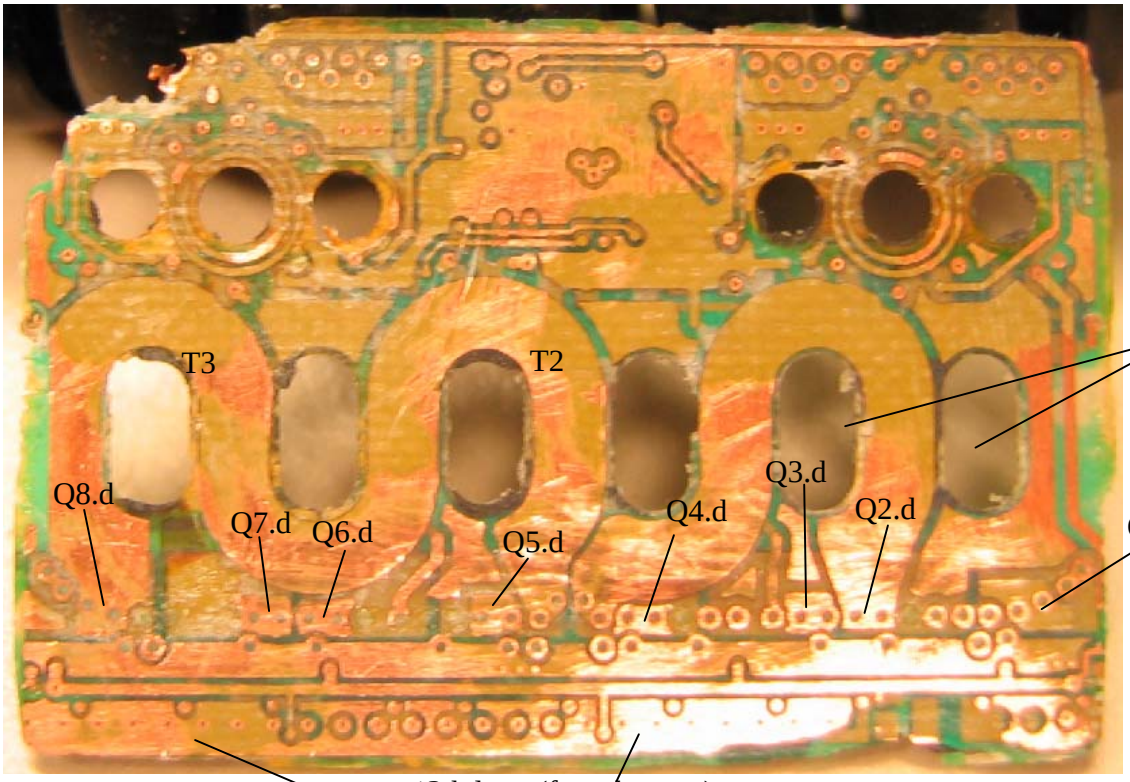


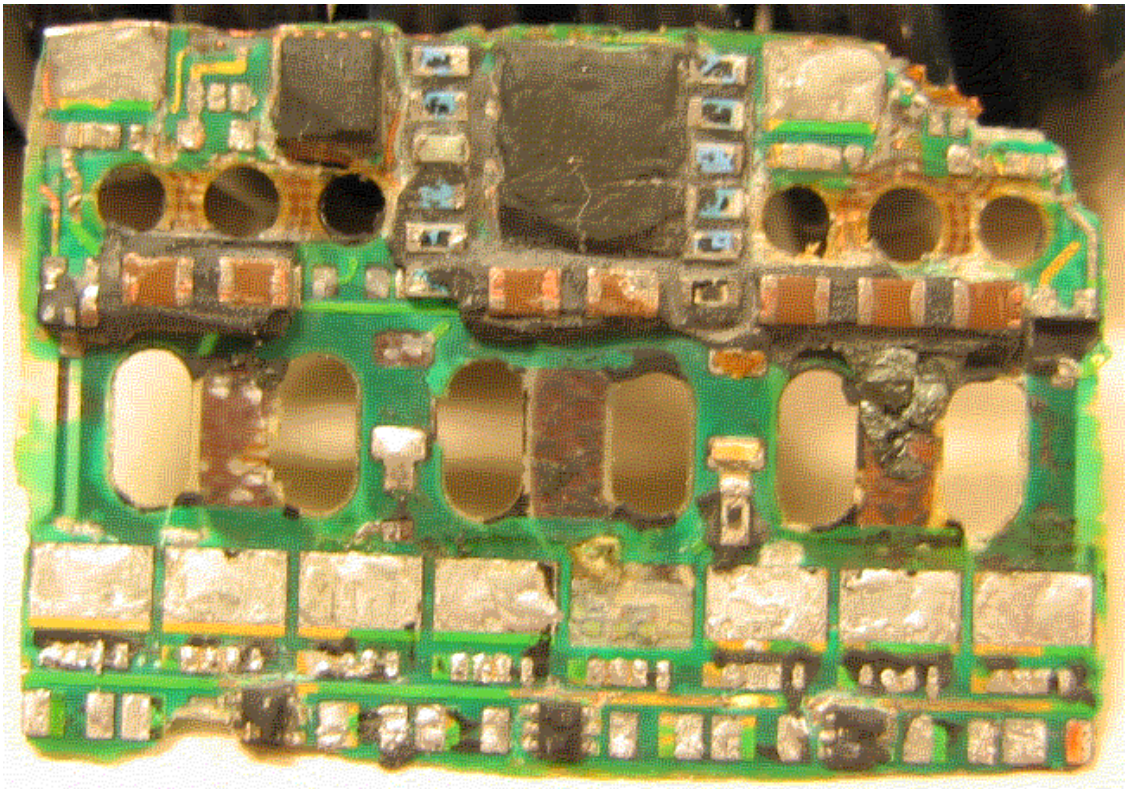
8th layer(from bottom)


Point 2
Primary Vin+
Point 1
9th layer(from bottom)
Primary Vin-
10th layer(from bottom)
Vout-
connected


Point 2
Primary Vin+
Point 1
Connected by FET
Connected by FET
11th layer(from bottom)
Vout+


Point 1
Point 2
12th layer(from bottom)
Vout-


T3
T2
T1
Q8.d
Q7.d
Q6.d
Q5.d
Q4.d
Q3.d
Q2.d
Q1.d
13th layer(from bottom)
Vout+



top layer

1.transformer windings distribution:

layer

Primary: 3,6,9,12

Secondary: 2, 4,5, 7,8, 10,11, 13

Layer1(bottom), Layer14(top) are components layers.

Q1~Q8 souces are in parellel

Q1.d, Q3.d, Q6.d, Q8.d gates in parellel

Q2.d, Q4.d, q5.d, q7.d gates in parellel

Q1,Q3,Q6,Q8, Drains are in parellel

Q2,Q5,Q7,Q4 Drains are in parellel.

So Q1,Q3,Q6,Q8 are in parellel and Q2,Q4,Q5,Q7 are in parellel

All FETs Drain pins are connected togather(layer 13), then tie to Vout-(layer 12),

Layer8: Q2d-Q4d-Q5d-Q7d are connected together by common copper.

Layer4: Q1d-Q3d-Q6d-Q8d are connected together by common copper.

2. Secondary transformer windings

Given current direction is from FET to Vout+

From		Through	To		Cores crossed	Flux direction
layer	part	Layer	layer	Part		
13	Q2.d	10	11	Vout+	T1,T2,T1	Left out,right in
13	Q8.d	10	11	Vout+	T3,T2,T3	Left in,right out
7	Q6.d	4	7	Vout+	T3,T3,T2	Left in,right out
7	Q4.d	4	7	Vout+	T2,T1,T1	Left out,right in
5	Q7.d	2	5	Vout+	T3,T2,T3	Left out,right in
5	Q1.d	2	3	Vout+	T1,T2,T1	Left in,right out
11	Q3.d	8	11	Vout+	T1,T1,T2	Left in,right out
11	Q5.d	8	11	Vout+	T2,T3,T3	Left out,right in

3.Primary transformer windings

Given current direction from Q1,Q2 to Q3,Q4

Layer14 Q1.d,Q2.s->layer 12T2,T1,->layer 6 T1,T2,T3,->layer3 T3 ->capacitor.

Magnetic flux direction: left in, righ out

capaciotr->layer3 T2,T1,->layer9, T1,T2,T3,->layer12,T3->layer 14 Q3.s(Q4.d)

Magnetic flux direction: left in,righ out

4. schematic of power stage