SSC2005S
Application Note Rev.0.4

The contents in this application note are preliminary, and are subject to changes without notice.

SANKEN ELECTRIC CO., LTD.
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CONTENTS

General Description

SSC2005S is a Critical Conduction Mode (CRM) control IC for power factor correction (PFC).

Since no input voltage sensing and no auxiliary winding for inductor current detection are required, the IC allows the realization of low standby power and the low number of external components. The product achieves high cost-performance and high efficiency PFC converter system.

Package

SOIC8

Not to scale

Features and Benefits

- Inductor Current Detection
  (No auxiliary winding required)
- Low Standby Power
  (No input voltage sensing required)
- Soft-Overvoltage Protection to limit Audible Noise
- Minimum Off-time Limitation Function to restrict the Rise of Operation Frequency
- High Accuracy Overcurrent detection: 0.6 V ± 5 %
- Protection Functions
  - Overcurrent Protection (OCP) ----- pulse-by-pulse
  - High-speed Overvoltage Protection (HOVP)
    ----------auto restart (with Hysteresis)
  - Soft Overvoltage Protection (SOVP) ---auto restart
  - Thermal Shutdown Protection (TSD)---auto restart (with Hysteresis)

Application

- PFC Circuit up to 200 W of Output Power such as:
  - AC/DC Power Supply
  - Digital appliances for large size LCD/PDP television and so forth
  - OA equipment for Computer, Server, Monitor, and so forth
  - Communication facilities

1. Absolute Maximum Ratings

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as "+", and a source as "−", referencing the IC.
- Unless specifically noted Ta = 25 °C

Characteristic	Pins	Symbol	Rating	Unit
VCC Pin Voltage	8 – 6	V_{CC}	28	V
OUT Pin Source Current	7 – 6	$I_{OUT(SRC)}$	−500	mA
OUT Pin Sink Current	7 – 6	$I_{OUT(SNK)}$	1000	mA
CS Pin Voltage	5 – 6	V_{CS}	−5 to +0.3	V
RDLY Pin Current	4 – 6	I_{RDLY}	−500 to 0	µA
RT Pin Current	3 – 6	I_{RT}	−500 to 0	µA
COMP Pin Current	2 – 6	I_{COMP}	−200 to +200	µA
FB Pin Voltage	1 – 6	V_{FB}	−0.3 to +5	V
Allowable Power Dissipation	—	P_D	0.5	W
Operating Ambient Temperature	—	T_{OP}	−40 to +150	°C
Storage Temperature	—	T_{stg}	−40 to +150	°C
Junction Temperature	—	T_j	150	°C

2. Recommended Operating Conditions

- Recommended operating conditions means the operation conditions maintained normal function shown in electrical characteristics.
- The IC should be used within the recommended conditions.

Characteristic	Pins	Symbol	Rating		Unit
			Min.	Max.	
VCC Pin Voltage in Operation	8 – 6	$V_{CC(OP)}$	14	26	V
RT Pin Resistance	3 – 6	R_{RT}	15	47	kΩ
RDLY Pin Resistance	4 – 6	R_{RDLY}	15	47	kΩ
Pin Resistance	—	$T_{j(OP)}$	−20	125	°C

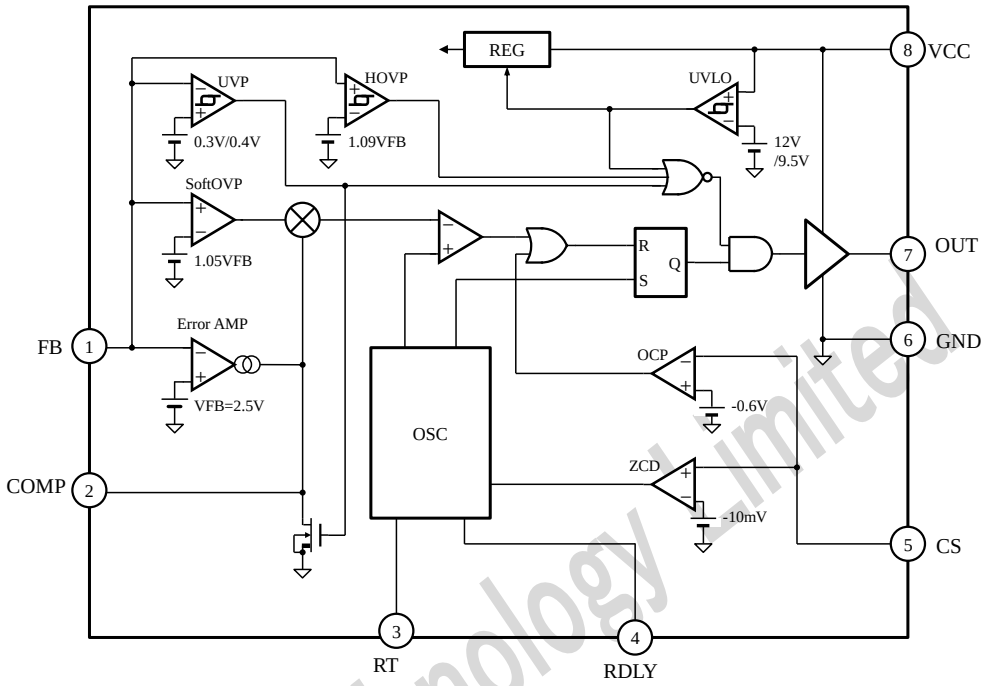
3. Electrical Characteristics

- For additional details, refer to the datasheet.
- The polarity value for current specifies a sink as "+", and a source as "–", referencing the IC.
- Unless specifically noted, V_{CC} = 14 V, V_{CS} = 0.1 V, Ta = 25 °C

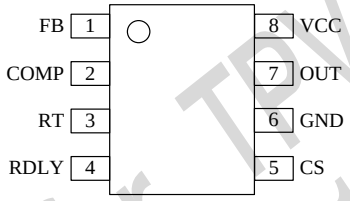
Characteristic	Pins	Symbol	Rating			Unit	Note
			Min.	Typ.	Max.		
Power Supply Operation							
Operation Start Voltage	8 – 6	$V_{CC(ON)}$	10.5	12	13.5	V	
Operation Stop Voltage	8 – 6	$V_{CC(OFF)}$	8.2	9.5	11.0	V	
Operation Voltage Hysteresis	8 – 6	$V_{CC(HYS)}$	—	2.5	—	V	
Circuit Current in Operation	8 – 6	$I_{CC(ON)}$	—	2.9	—	mA	
Circuit Current in Non-Operation	8 – 6	$I_{CC(OFF)}$	—	80	160	µA	V_{CC} = 9.5 V
Oscillation Operation							
Maximum On-Time	7 – 6	$t_{ON(MAX)}$	—	23	—	µs	V_{FB} = 1.5 V R_{DLY} = 22 kΩ
Minimum Off-Time	7 – 6	$t_{OFF(MIN)}$	—	2.4	—	µs	
RT Pin Voltage	3 – 6	V_{RT}	1.3	1.5	1.7	V	
Feedback Control Voltage	1 – 6	V_{FB}	2.46	2.5	2.54	V	
Feedback Line Regulation	1 – 6	$V_{FB(LR)}$	−5	1.0	15	mV	
FB Pin Bias Current	1 – 6	I_{FB}	—	−2	—	µA	
Error Amplifier Transconductance Gain	1, 2 – 6	gm	—	103	—	µS	
COMP Pin Sink Current	2 – 6	$I_{COMP(SNK)}$	—	40	—	µA	
COMP Pin Source Current	2 – 6	$I_{COMP(SRC)}$	—	−40	—	µA	
Zero Duty COMP Voltage	2 – 6	$V_{COMP(ZD)}$	—	0.65	—	V	
Restart Time *	—	t_{RS}	—	50	—	µs	
RDLY Pin Voltage	4 – 6	V_{RDLY}	1.3	1.5	1.7	V	
Zero Current Detection							
Zero Current Detection Threshold Voltage	5 – 6	V_{ZCD}	−20	−10	0	mV	
Zero Current Detection Delay Time	5 – 6	$t_{DLY(ZCD)}$	—	1.25	—	µs	
Drive Output							
Output Voltage (High)	7 – 6	V_{OH}	—	12	—	V	
Output Voltage (low)	7 – 6	V_{OL}	—	0.75	—	V	
Output Rise Time	7 – 6	t_r	—	45	120	ns	C_{OUT} = 1000 pF
Output Fall Time	7 – 6	t_f	—	20	70	ns	C_{OUT} = 1000 pF
Protection Operation							
Overcurrent Protection Threshold Voltage	5 – 6	$V_{CS(OCP)}$	−0.63	−0.6	−0.57	V	
Overcurrent Protection Delay Time	5 – 6	$t_{DLY(OCP)}$	—	200	—	ns	
CS Pin Source Current	5 – 6	I_{CS}	—	−65	—	µA	
High-speed Overvoltage Protection Threshold Voltage	1 – 6	V_{HOVP}	—	1.09	—	× V_{FB}	
High-speed Overvoltage Protection Hysteresis	1 – 6	$V_{HOVPHYS}$	—	100	—	mV	
Soft-overvoltage Protection Threshold Voltage	1 – 6	V_{SOVP}	—	1.05	—	× V_{FB}	
Soft-overvoltage Protection On-time Deviation *	1 – 6	t_{SOVP}	—	65	—	%	
Undervoltage Protection Threshold Voltage	1 – 6	V_{UVP}	—	300	—	mV	
Undervoltage Protection Hysteresis	1 – 6	V_{UVPHYS}	—	100	—	mV	
Thermal Shutdown Threshold *	—	$T_{j(TSD)}$	—	150	—	°C	
Thermal Shutdown Hysteresis *	—	$T_{j(TSDHYS)}$	—	10	—	°C	

* Design assurance item

4. Functional Block Diagram

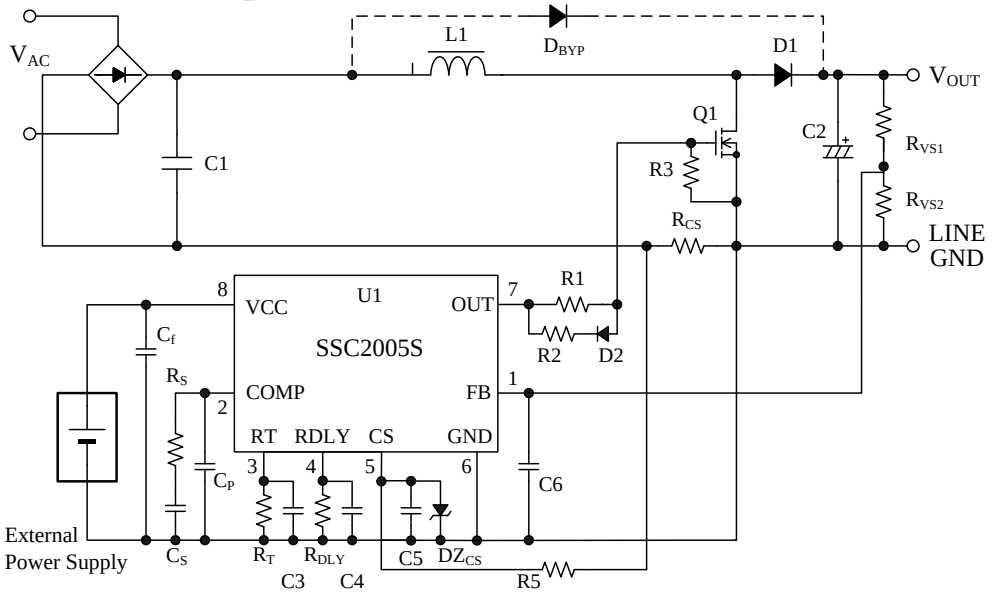


5. Pin-out Diagram



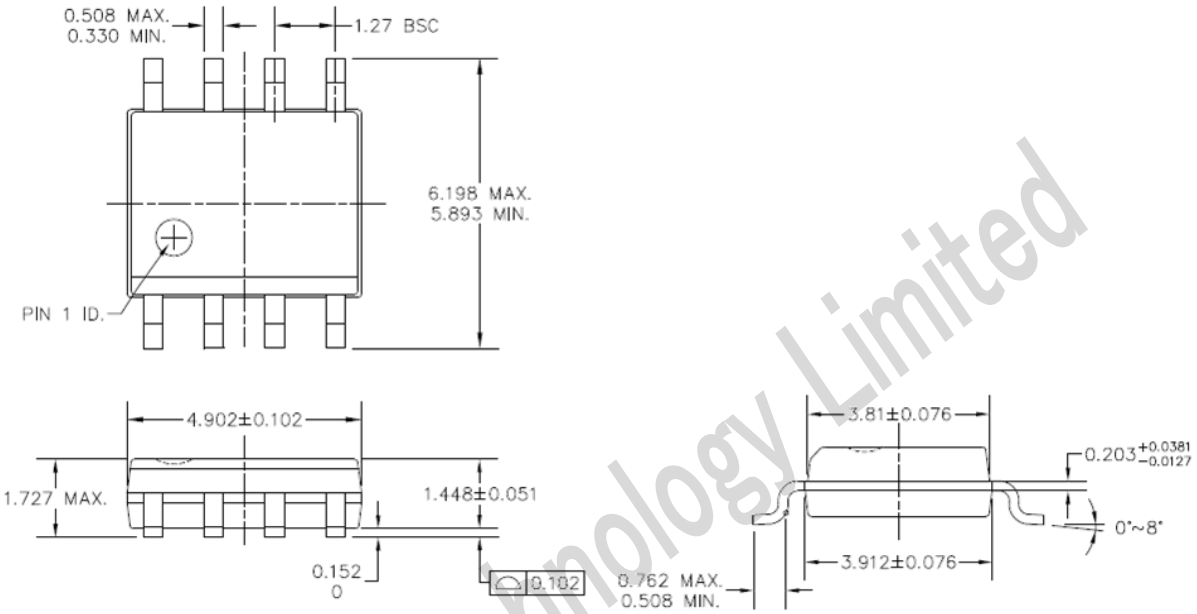
Number	Name	Function
1	FB	Feedback signal input and overvoltage protection signal input and undervoltage Protection signal input
2	COMP	Phase compensation
3	RT	Maximum on-time adjustment
4	RDLY	Zero current detection and delay time adjustment
5	CS	Overcurrent protection and zero current detection signal input
6	GND	Ground
7	OUT	Gate drive output
8	VCC	Power supply input for control circuit

6. Typical Application Circuit



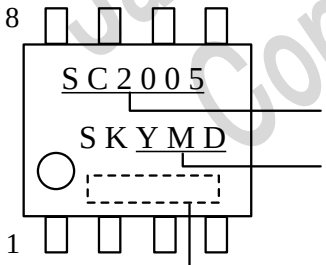
7. Package Diagram

SOIC8



NOTES:
1) All liner dimensions are in millimeters
2) Pb-free. Device composition compliant with the RoHS directive.

8. Marking Diagram



Part Number

Lot Number
Y is the last digit of the year (0 to 9)
M is the month (1 to 9,O,N or D)
D is a period of days
1 : 1st to 10th
2 : 11th to 20th
3 : 21st to 31st

Sanken Control Number

9. Functional Description

- With regard to current direction, "+" indicates sink current (toward the IC) and "–" indicates source current (from the IC).
- All of the parameter values used in these descriptions are typical value, unless otherwise specified.

9.1 Critical Conduction Mode: CRM

Figure 9-1 and Figure 9-2 show the PFC circuit and CRM operation waveform.

The IC performs the on/off operation of switching device Q1 in critical mode (the inductor current is zero) as shown in Figure 9-1.Thus the low drain current variation di/dt of power MOSFET is accomplished. Also, adjusting the turn on timing at the bottom point of V_{DS} free oscillation waveform (quasi-resonant operation), low noise, low switching loss and high efficiency PFC circuit up to 200 W is realized.

The power MOSFET Q1 starts switching operation by self-oscillation.

As shown in Figure 9-3, the detection voltage R_{VS2} is compared with the reference voltage V_{FB} = 2.5 V by using error amplifier (Error AMP) connected to FB pin. The output of the Error AMP is averaged and phase compensated. This signal V_{COMP} is compared with the ramp signal V_{OSC} to achieve on-time control. The off duty D_{OFF} of boost converter in CRM mode have the relation of $D_{OFF}(t) = V_{AC}(t)/V_{OUT}$ and is proportional to input voltage, where $V_{AC}(t)$ is the input voltage of AC line as a function of time. In order to boost the sinusoidal AC input voltage, the voltage control of the system respond to low frequency below 20 Hz in general.

As a result of aforementioned control shown in Figure 9-4, the peak current I_{LPEAK} of the inductance current I_L become sinusoidal. Since the averaged input current become similar to AC input voltage waveform by Low Pass Filter (LPF) at input stage, high power factor is achieved.

The off-time and the bottom on timing of V_{DS} are set by both zero current detection of drain current and the delay time configured by RDLY pin resistance. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

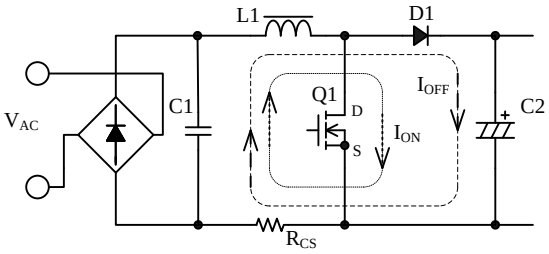


Figure 9-1 PFC Circuit

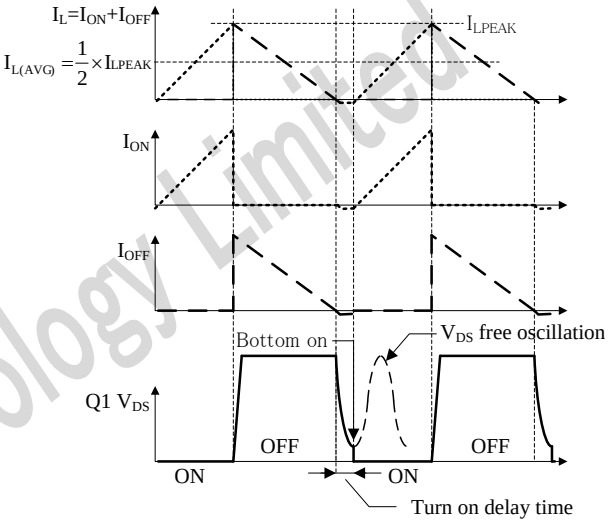


Figure 9-2 CRM operation and bottom on operation

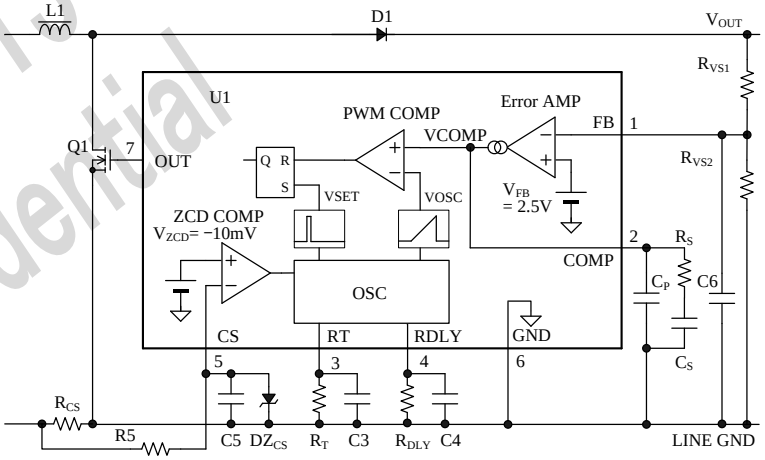


Figure 9-3 CRM Control Operation

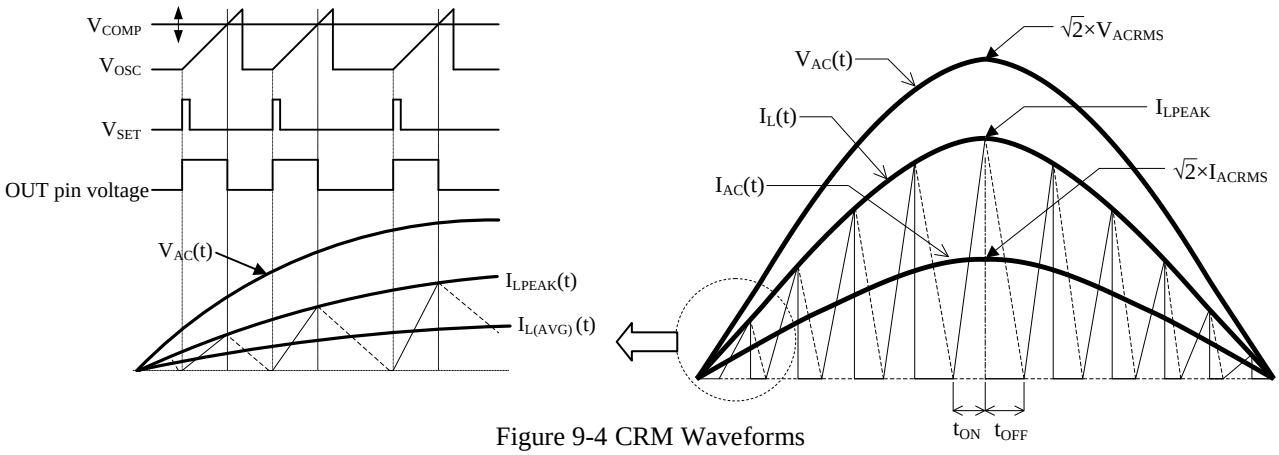


Figure 9-4 CRM Waveforms

9.2 Startup Operation

Figure 9-5 shows the VCC pin peripheral circuit.

VCC pin is a control circuit power supply input. The voltage is supplied by using external power supply. As shown in Figure 9-6, when VCC pin voltage rises to the Operation Start Voltage $V_{CC(ON)}$ = 12 V, the control circuit starts operation.

When the VCC pin voltage decreases to $V_{CC(OFF)}$ = 9.5 V, the control circuit stops operation by Undervoltage Lockout (UVLO) circuit, and reverts to the state before startup.

When VCC pin and the external power supply are distant from each other, placing a film capacitor C_f (approximately 0.1 µF) between the VCC pin and the GND pin is recommended.

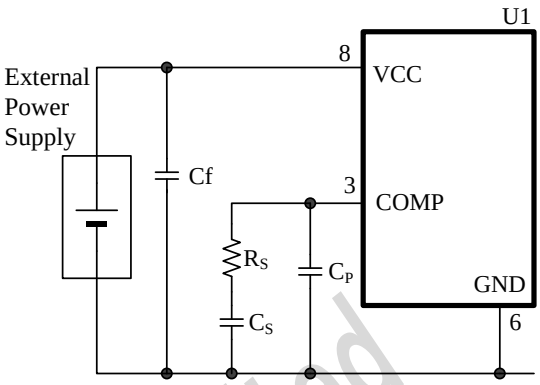


Figure 9-5 VCC pin peripheral circuit

Since the COMP pin voltage rises from zero during startup period, the VCOMP signal shown in Figure 9-3 gradually rises from low voltage. The on-width gradually increased to restrict the rise of output power by the Softstart Function. Thus the stress of the peripheral component is reduced.

9.3 Restart Circuit

Since the IC is self-oscillation type, when the duration of off-state of OUT pin voltage exceeds the Restart Time t_{RST} = 50 µs, OUT pin outputs on-signal as a trigger of switching operation and switching operation starts. At startup and intermittent oscillation period at light load, the restart circuit is activated and the switching operation is stabilized.

Since t_{RST} = 50 µs corresponds to the operational frequency of 20 kHz, set the inductance value high enough compared to this operational frequency. In normal operation, off-time is determined by the zero current detection circuit.

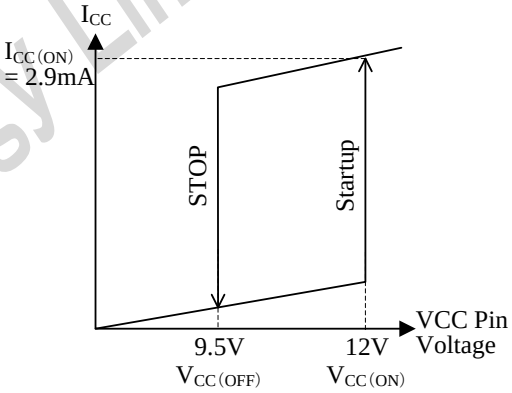


Figure 9-6 V_{CC} pin voltage and I_{CC}

9.4 Maximum On-time setting

In order to reduce audible noise of transformer at transient state, the IC has the Maximun on-time, $t_{ON(MAX)}$. This $t_{ON(MAX)}$ is adjusted by the resistance R_T which is connected to RT pin.

Figure 9-7 shows the relation between R_T value and $t_{ON(MAX}$ in IC design.

The $t_{ON(MAX)}$ is made into a larger value than $t_{ON(SET)MAX}$ that is result of Equation (1) in page13 "Inductor"

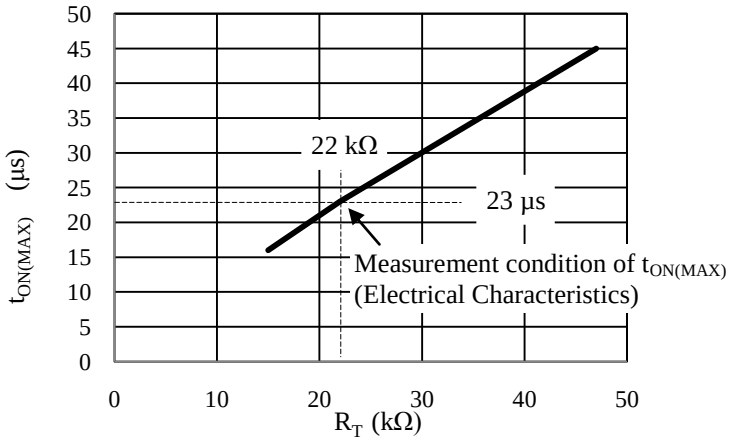


Figure 9-7 R_T vs. $t_{ON(MAX)}$ (IC design)

9.5 Zero Current Detection

The off-time and the bottom on timing of V_{DS} are set by both zero current detection of drain current and the delay time. Thus simple PFC circuit with inductor having no auxiliary winding is realized.

As shown in Figure Figure 9-8, when the voltage of detection resistor R_{CS} become smaller than the absolute value of Zero Current Detection Voltage V_{ZCD} = −10 mV, OUT pin outputs on-signal after the delay time which is determined by the resistor connected to RDLY pin.

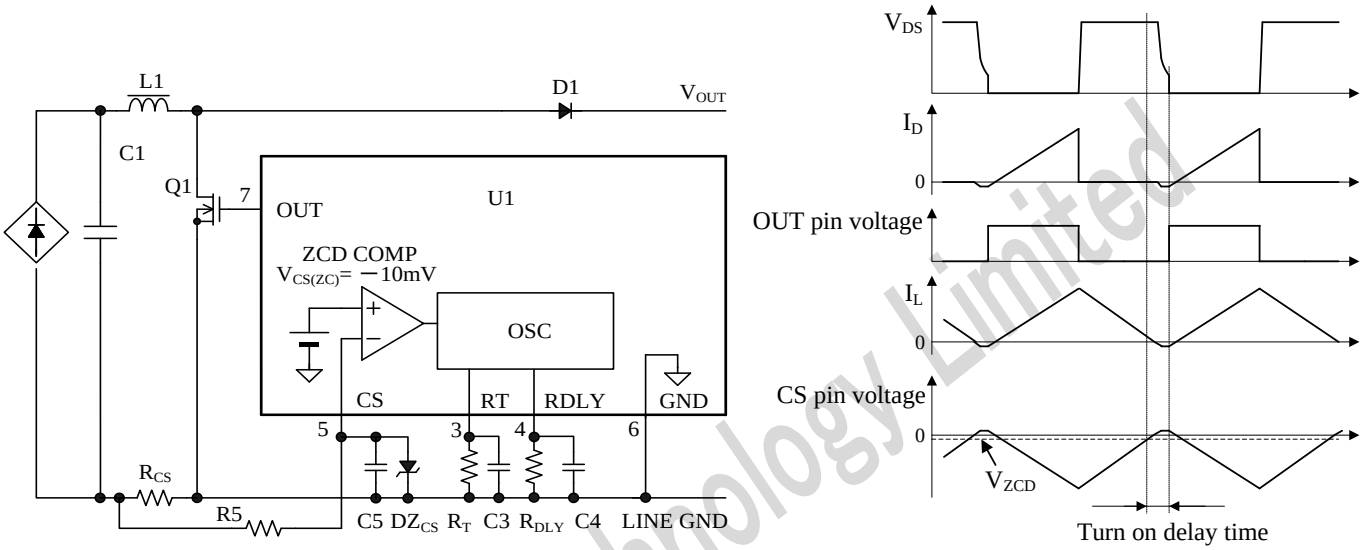


Figure 9-8 Zero current detection

9.6 Bottom-On Timing (Delay Time) Setting

Adjusting the output timing of the on signal to the bottom point of V_{DS} free oscillation waveform (quasi-resonant operation), low noise, low switching loss and high efficiency PFC circuit is realized.

Figure 9-9 shows the relation between R_{DLY} value and the designed delay time, t_{DLY}. As shown in Figure 9-10, adjust the turn on timing to the bottom point of V_{DS} free oscillation waveform.

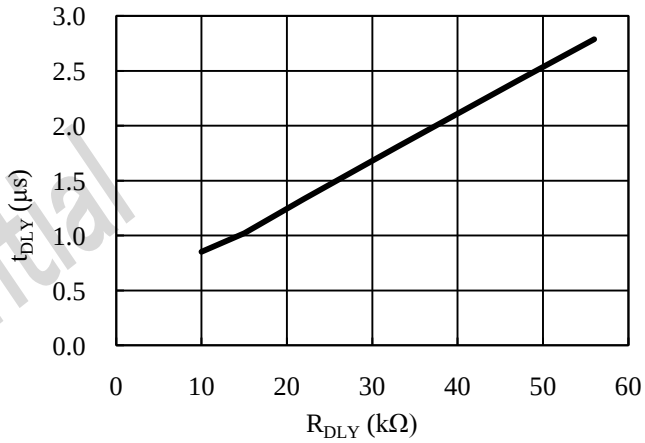


Figure 9-9 R_{DLY} vs. t_{DLY} (IC design)

9.7 Minimum Off-time Limit Function

In order to prevent the rise of operation frequency at light load, the IC have the Minimum Off-Time $t_{OFF(MIN)}$ = 2.4 µs.

If this Minimum Off-Time is shorter than the freewheeling time of inductor, the IC operates in discontinuous condition mode (DCM).

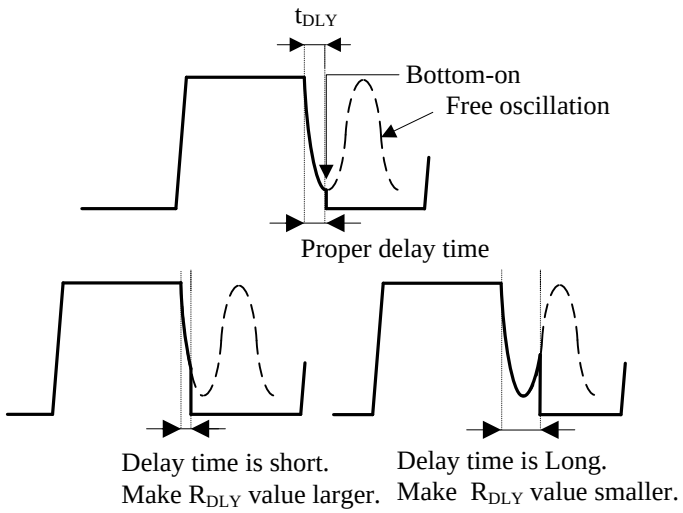


Figure 9-10 V_{DS} turn on timing

9.8 FB pin Short/Open ProtectionFunction

Abnormal rise of V_{OUT} may occur by the lowering of FB pin voltage due to the malfunctions in feedback loop such as open of R_{VS1} or short of R_{VS2}. In this abnormal operation, Overvoltage Protection function is disabled.

In order to prevent this, Under Voltage Protection function is implemented (Figure 9-11).

When FB pin voltage becomes lower than V_{UVP} = 300 mV by malfunction in feedback loop, OUT pin output becomes off immediately and switching operation stops. This prevents the rise of output voltage. When the cause of malfunction is removed and the FB pin voltage rises to 400 mV, the switching operation restarts.

When FB pin is open, FB pin voltage increases by constant current circuit, I_{FB} = –2 µA of inside of FB pin.

When this voltage becomes higher than V_{HOVP} = 1.09 × V_{FB}, the OUT pin voltage becomes Low state and stops switching operation.

When the cause of abnormal is removed and the IC becomes normal control, the switching operation starts.

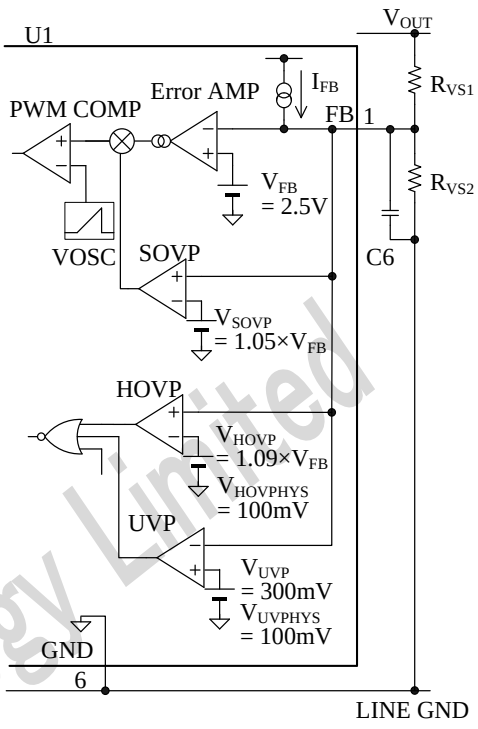


Figure 9-11 Overvoltage Protection Detection Circuit

9.9 Overvoltage Protection Function (OVP)

The IC has two OVP activation methods: Soft Overvoltage Protection (SOVP) and High-speed Overvoltage Protection (HOVP).

- Soft Overvoltage Protection (SOVP)
  Figure 9-12 shows the waveforms of Soft Overvoltage Protection (SOVP) operation.
  The rise of output voltage is restricted by reducing on-time to 65 % when FB pin voltage reaches to V_{SOVP} (1.05 times the reference voltage V_{FB} = 2.5 V).
  SOVP function prevents the rise of output voltage with continuing the switching operation. Thus the generation of audible noise is suppressed.

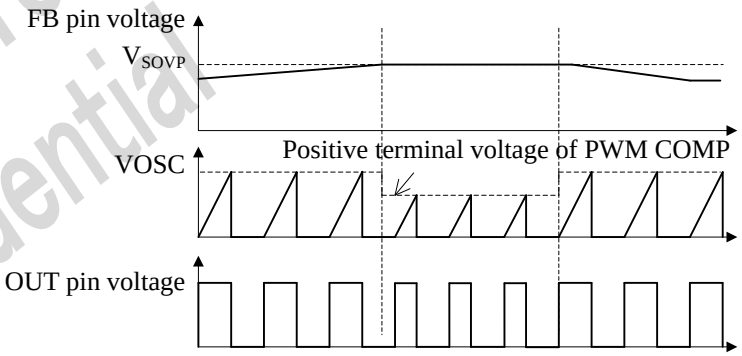


Figure 9-12 Soft Overvoltage Protection (SOVP) operation

- High-speed Overvoltage Protection (HOVP)
  Figure 9-13 shows the waveforms of High-speed Overvoltage Protection (HOVP) operation.
  In case that SOVP function cannot prevent the rise of the output voltage and the FB pin voltage reaches to V_{HOVP} (1.09 times the reference voltage V_{FB} = 2.5 V), OUT pin voltage become Low immediately and the switching operation stops. As a result, the rise of output voltage is prevented.
  When the cause of the overvoltage is removed and FB pin voltage decreases to the $V_{HOVPHYS}$ = 100 mV, the switching operation starts.

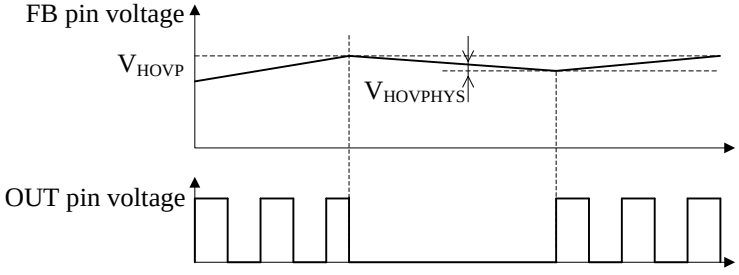


Figure 9-13 High-speed Overvoltage Protection (HOVP) operation

9.10 Overcurrent Protection (OCP)

Figure 9-14 shows the CS pin peripheral circuit.

Overcurrent Protection Function (OCP) detects inductance current I_L by the current detection resistor, R_{CS}, on pulse-by-pulse basis. When the detection voltage, V_{RCS}, increases to an absolute value of OCP Threshold Voltage, $V_{CS(OCP)}$ = −0.6 V, the output of OUT pin is turned off and the output power.

As shown in Figure 9-14, CR filter (R5 and C5), and DZ_{CS} (zenar diode) are connected to CS pin.

When the power MOSFET turns off, surge current may flow through the power MOSFET. As a result of OCP detection of the surge current, it would cause a malfunction. Thus a CR filter (R5 and C5) is inserted at the CS pin.

When the rush current charges the output capacitor C2 at startup, R_{CS} voltage may become high. In order to limit the CS pin voltage within the maximum absolute rating of −5 V, DZ_{CS} is placed.

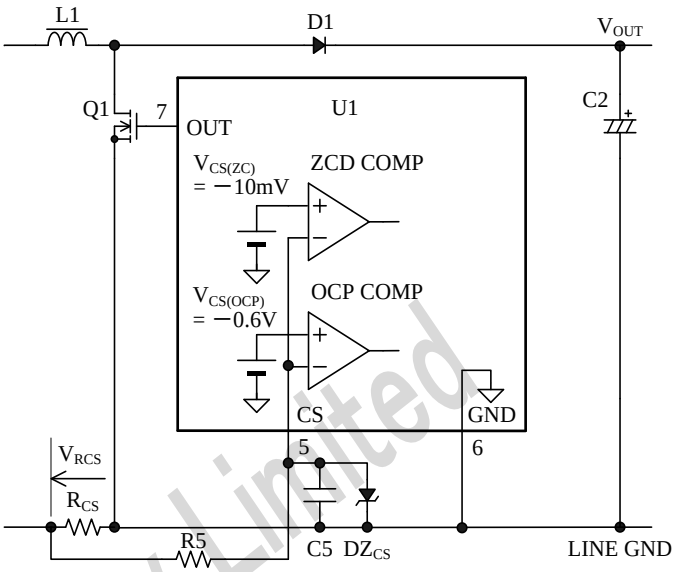


Figure 9-14 CS pin peripheral circuit

10. Desing Notes

10.1 Parameter Design

● Inductor

Apply proper design margin to temperature rise by core loss and copper loss.
Inductance L_P of PFC in CRM mode are calculated as follows:

1) Operational Frequency, $f_{SW(SET)}$ and Maximum On-time, $t_{ON(SET)MAX}$

At first, determine $f_{SW(SET)}$ that is minimum operational frequency at the peak of the AC line waveform. The frequency becomes higher with lowering the input voltage. The frequency at the peak of the AC line waveform, $f_{SW(SET)}$ should be set above frequency of 25 kHz.
The $t_{ON(SET)MAX}$ at $f_{SW(SET)}$ is calculated by Equation (1). The $t_{ON(MAX)}$ described in "9.4 Maximmum on-time setting" should be set above $t_{ON(SET)MAX}$.

$$t_{ON(SET)MAX} = \frac{V_{OUT} - \sqrt{2} \times V_{ACRMS(MIN)}}{f_{SW(SET)} \times V_{OUT}} \text{ (s)} \quad \text{-----(1)}$$

Where,
V_{OUT} : Out put voltage (V)
$V_{ACRMS(MIN)}$: Maximum AC input voltage rms value (V)

2) Output Voltage, V_{OUT}

The output voltage V_{OUT} of boost-converter is higher than input voltage.
Set the voltage of V_{OUT} higher than the peak value of the AC input voltage by approximately 10 V, according to following equation:

$$V_{OUT} \geq \sqrt{2} \times V_{ACRMS(MAX)} + 10 \text{(V)} \quad \text{-----(2)}$$

Where,
$V_{ACRMS(MAX)}$: Maximum AC input voltage rms value (V)

3) Inductance, L_P

Substituting both minimum and maximum of AC input voltage to V_{ACRMS}, choose a smaller one as L_P value.
L_P is calculated as follows:

$$L_P = \frac{\eta \times (V_{ACRMS})^2 \times t_{ON(SET)MAX}}{2 \times P_{OUT}} \text{ (H)} \quad \text{-----(3)}$$

Where,
V_{ACRMS} : AC input voltage rms value (V)
P_{OUT} : Output Power (W)
η : Efficiency of PFC (In general, the range of η is 0.90 to 0.97, depending on on-resistance of power MOSFET $R_{DS(ON)}$ and forward voltage drop of rectifier diode V_F.)

4) Inductor peak current, I_{LP}

I_{LP} is peak current of the peak at the minimum AC input voltage.
I_{LP} calculated as follows:

$$I_{LP} = \frac{2 \times \sqrt{2} \times P_{OUT}}{\eta \times V_{ACRMS(MIN)}} \text{ (A)} \quad \text{--------(4)}$$

Proper margin against peak current, I_{LP}, is necessary in inductor design in order to avoid magnetic saturation.

● FB pin peripheral circuit (Output voltage detection)

Figure 10-1 shows the FB pin peripheral circuit.
The output voltage V_{OUT} is set using R_{VS1} and R_{VS2}. It is expressed by the following formula:

$$V_{OUT} = \left(\frac{V_{FB}}{R_{VS2}} - I_{FB} \right) \times R_{VS1} + V_{FB} \quad \text{------(5)}$$

Where,
V_{FB} : Feedback reference voltage = 2.5 V
I_{FB} : Bias current = –2 µA
R_{VS1}, R_{VS2} : Combined resistance to set V_{OUT}

Since R_{VS1} have applied high voltage and have high resistance value, R_{VS1} should be selected from resistors designed against electromigration or use a combination of resistors for that.
The value of capacitor C6 between FB pin and GND pin is set approximately 100 pF to 3300 pF, in order to reduce the switching noise.

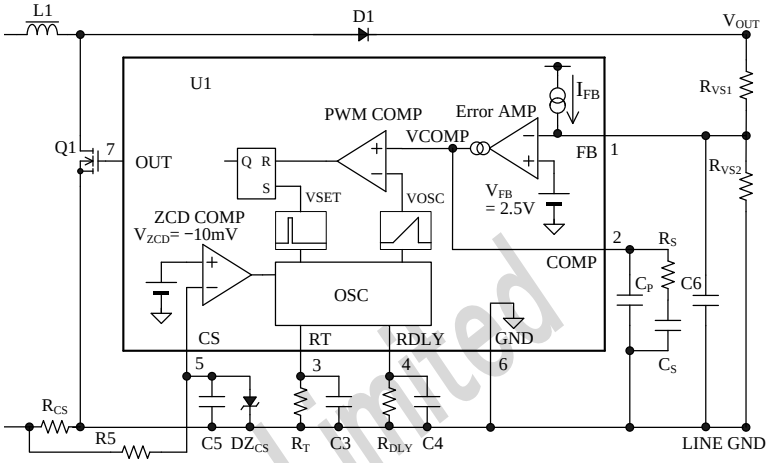


Figure 10-1 IC peripheral circuit

● COMP pin peripheral circuit : R_S, C_S, C_P

Figure 10-1 shows the IC peripheral circuit.
The FB pin voltage is induced into internal Error AMP. The output voltage of the Error AMP is averaged by the COMP pin. The on-time control is achieved by comparing the signal V_{COMP} and the ramp signal V_{OSC}.
C_S and R_S adjust the response speed of changing on-time according to output power.
The typical value of C_S and R_S are 1 µF and 10 kΩ, respectively. When C_S value is too large, the response becomes slow at dynamic variation of output and the output voltage decreases.
Since C_S and R_S affect on the soft-start period at startup, adjustment is necessary in actual operation.
The ripple of output detection signal is averaged by C_P. When the C_P value is too small, the IC operation may become unstable due to the output ripple. The value of capacitor C_P is approximately 0.47 µF.

● RT pin peripheral circuit : R_T ,C3

R_T shown in Figure 10-1 is for the adjustment of maximum on-time, $t_{ON(MAX)}$.
The $t_{ON(MAX)}$ is made into a larger than $t_{ON(SET)MAX}$ value which is the result of Equation (1) in page13 “Inductor.”
The value of capacitor C3 in parallel with R5 is approximately 0.01 µF, in order to reduce the switching noise.

● RDLY pin peripheral circuit : R_{DLY}, C4

R_{DLY} shown in Figure 10-1 is for the adjustment of the turn on timing of V_{DS}.
As shown in “9.6 Bottom-On Timing (Delay Time) Setting,” adjust the turn on timing to the bottom point of V_{DS} free oscillation waveform.
The value of capacitor C4 is approximately 0.01 µF, in order to reduce the switching noise.

● CS pin peripheral circuit

R_{CS} shown in Figure 10-1 is current sensing resistor.
R_{CS} is calculated using the following Equation (6), where Overcurrent Protection Threshold Voltage $V_{CS(OCP)}$ is −0.6 V and I_{LP} is calculated using Equation (4).

$$R_{CS} \leq \frac{\left| V_{CS(OCP)} \right|}{I_{LP}} \ (\Omega) \qquad \text{--------(6)}$$

Both CR filter (R5 and C5) and DZ_{CS}(zenar diode) are connected to CS pin.
R5 value of approximately 47 Ω is recommended, since the CS Pin Source Current affects the accuracy of OCP detection. C5 value is reccommended to be calculated by using following formula in which cut-off frequency of CR filter (C5 and R5) is approximately 1 MHz.

$$C5 = \frac{1}{2 \times \pi \times 1\text{MHz} \times R5} \qquad \text{--------(7)}$$

In case R5 value is 47 Ω, C5 value is approximately 3300 pF.

DZ_{CS} value of approximately 3.9 V is recommended. The value should be higher than $V_{CS(OCP)}$ and be lower than CS pin absolute maximum rating of −5 V.

● OUT pin peripheral circuit (Gate drive circuit)

Figure 10-2 shows the OUT pin peripheral circuit.
The OUT pin is the gate drive output which can drive the external power MOSFET directly.
The maximum output voltage of OUT pin is the VCC pin voltage. The maximum current is −500 mA for source and 1 A for sink, respectively.
R1 is for source current limiting. Both R2 and D2 are for sink current limiting. The values of these components are adjusted to decrease the ringing of GATE pin voltage and the EMI noise. The reference value is several ohms to several dozen ohms.
R3 is used to prevent malfunctions due to steep dv/dt at turn-off of the power MOSFET, and the resistor is connected near the MOSFET, between the gate and source. The reference value of R3 is from 10 kΩ to 100 kΩ.
R1, R2, D2 and R3 are affected by the printed circuit board trace layout and the power MOSFET capacitance. Thus the optimal values should be adjusted under actual operation of the application.

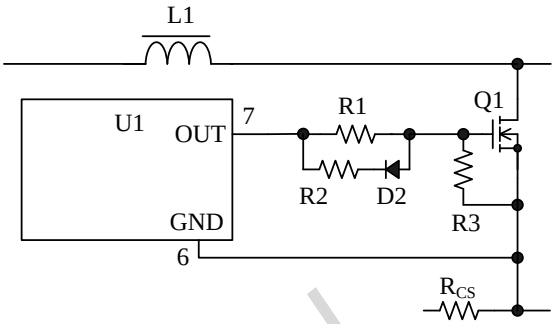


Figure 10-2 OUT pin peripheral circuit

● VCC pin peripheral circuit

Figure 10-3 shows the VCC pin peripheral circuit.
VCC pin is power supply input. VCC pin is supplied from an external power.
The value of capacitor C7 is set approximately 0.47 μF, in order to reduce the switching noise.

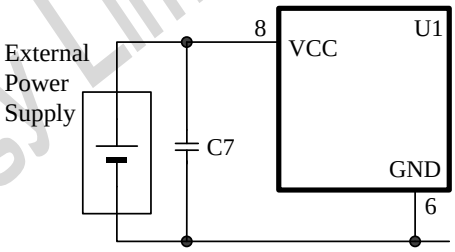


Figure 10-3 VCC pin peripheral circuit

● Power MOSFET : Q1

Choose a power MOSFET having proper margin of V_{DSS} against output voltage V_{OUT}.
The size of heat sink is chosen taking into account some loss by switching and ON resistance of MOSFET.
The RMS value of drain current, I_{DRMS} is expressed as follows:

$$I_{DRMS} = \frac{2\times\sqrt{2}\times P_{OUT}}{\eta\times V_{ACRMS\,(MIN)}}\times\sqrt{\frac{1}{6}-\frac{4\times\sqrt{2}\times V_{ACRMS(MIN)}}{9\times\pi\times V_{OUT}}}\ (A) \quad \text{----------}\ (8)$$

The loss $P_{RDS(ON)}$ by on-resistance $R_{DS(ON)}$ of power MOSFET is calculated as follows:

$$P_{RDS\,(ON)} = (I_{DRSM})^2\times R_{DS(ON)125\,°C} \quad \text{----------}\ (9)$$

where,
$R_{DS(ON)125°C}$: ON resistance of MOSFET at T_{ch} = 125 °C

● Boost Diode : D_{FW}

Choose a boost diode having proper margin of a peak reverse voltage V_{RSM} against output voltage V_{OUT}.
A fast recovery diode is recommended to reduce the switching noise and loss. Please ask our staff about our lineup.

The size of heat sink is chosen taking into account some loss by V_F and recovery current of boost diode.
The loss of V_F, P_{DFW} is expressed as follows:

$$P_{DFW} = V_F\times I_{OUT}\ (W) \quad \text{----------}\ (10)$$

Where,
V_F : Forward voltage of boost diode (V)
I_{OUT} : Out put current (A)

● Bypass Diode : D_{BYP}

Bypass diode protects the boost diode from a large current such as an inrush current. A high surge current tolerance diode is recommended. Please ask our staff about our lineup.

● Output Capacitor : C2

Apply proper design margin to accommodate the ripple current, the ripple voltage and the temperature rise. Use of high ripple current and low impedance types, designed for switch-mode power supplies, is recommended, depending on their purposes.

In order to obtain C2 value Co, caalculate both Equation (11) and (12) described in following and select a larger value.

1) Given the C2 ripple voltage $V_{OUTRIPPLE}$ (V_{PP}) (10 V_{PP} for example), C_O is expressed as follows:

$$C_O > \frac{I_{OUT}}{2 \times \pi \times f_{LINE} \times V_{OUTRIPPLE}} \text{ (F)} \qquad \text{-----(11)}$$

where,

f_{LINE} : Line frequency (Hz)
I_{OUT} : Output current (A)

The C2 voltage is expressed as follows:

$$V_{C2} = V_{OUT} \pm \frac{V_{OUTRIPPLE}}{2}$$

When the output ripple is high, the V_{C2} voltage may reach to High Speed or Low Speed overvoltage Protection voltage (V_{HOVP} or V_{SOVP}) in near the maximum value of V_{C2}, or input current waveform may be distorted due to the stop of the boost operation in near the minmum value of V_{C2}. It is necessary to select large C_O value or change the setting of output voltage (boost voltage)

2) Given the output hold time as t_{HOLD} (s), C_O is expressed as follows:

$$C_O > \frac{2 \times P_{OUT} \times t_{HOLD}}{\left((V_{OUT})^2 - (V_{OUT(MIN)})^2\right) \times \eta} \text{ (F)} \qquad \text{-----(12)}$$

where,

t_{HOLD} : Output hold time (s)
$V_{OUT(MIN)}$: Minmum output voltage of C2 during output hold (V)
η : Efficiency

In case t_{HOLD} = 20 ms, P_O = 200 W, η = 90 % and the output voltage = 330 V to 390 V, C_O value is derived as 205 µF. Thus, C_O value of approximately 220 µF is connected.

10.2 PCB Trace Layout

PCB circuit trace design and component layout affect proper functioning during operation, EMI noise, and power dissipation. Therefore, wide, short traces, and small circuit loops are important to reduce line impedance where high frequency current traces form a loop as shown in Figure 10-5. In addition, local GND and earth ground traces affect radiated EMI noise, and the same measures should be taken into account.

Switching mode power supplies consist of current traces with high frequency and high voltage, and thus trace design and component layouts should be done to comply with all safety guidelines.

Furthermore, because an integrated power MOSFET is being used as the switching device, take account of the positive thermal coefficient of $R_{DS(ON)}$ when preparing a thermal design.

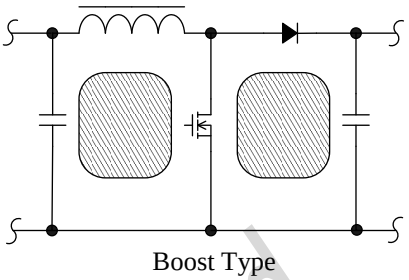


Figure 10-4 High-frequency current loops (hatched areas)

Figure 10-6 shows a circuit layout design example.

(1) Main Circuit Trace
This trace contains switching current, and thus it should be as wide and short as possible.

(2) GND Trace Layout
In order to reduce the effect of switching current in main circuit trace, the control ground circuit and the main circuit ground should be connected at point A in Figure 10-6. Control ground should be connected by dedicated trace.

(3) Current Detection Resistor R_{CS} Trace Layout
In order to reduce the noise in current detection, the connection between R_{CS} and R5 which is connected to CS pin should be dedicated trace.

(4) Peripheral Component of IC
Place the components for phase compensation connected to COMP pin close to both COM pin and GND pin.

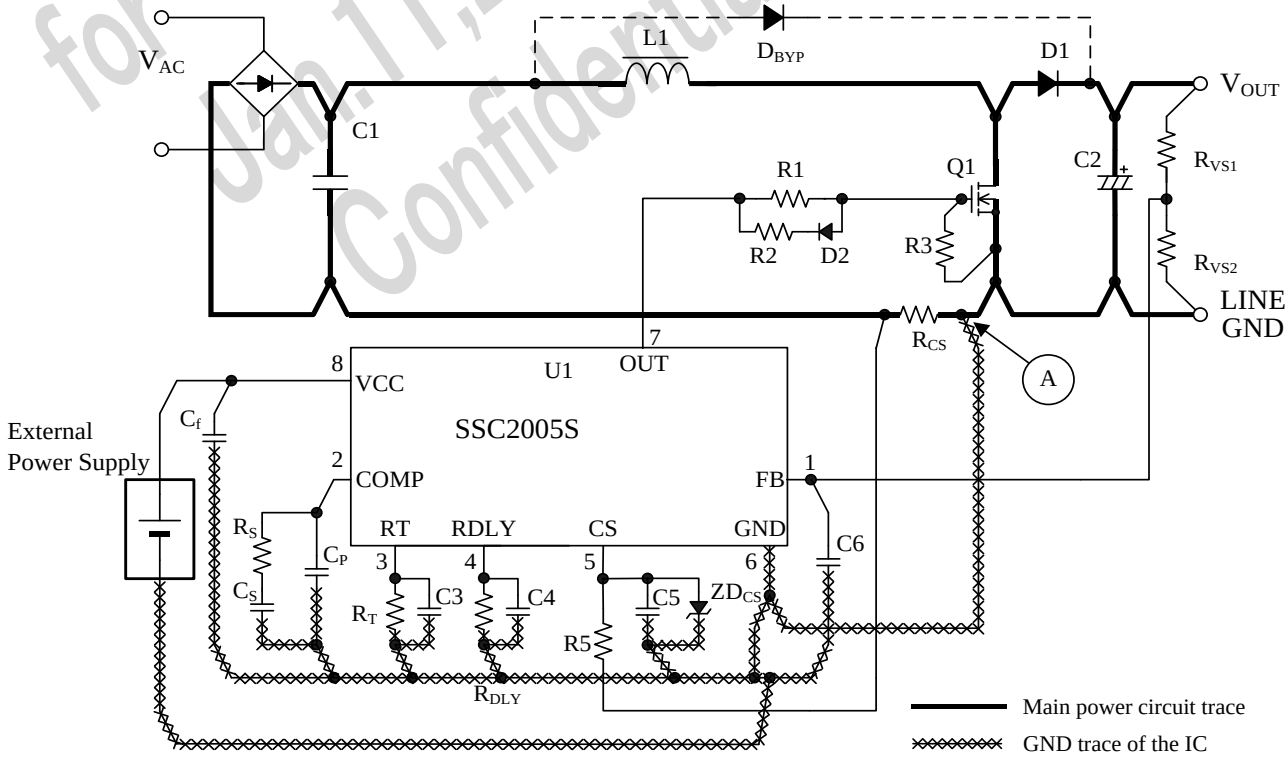


Figure 10-5 Example of connection of peripheral components

11. Example Circuit

The circuit is an example. Adjustment is necessary in actual operation.

Example of Specification

AC input voltage	Input power	Output voltage	Operation frequency (at maximum AC input)
85 V to 265 V	200 W	398 V	60 kHz (AC 265 V)

Example of Schematic

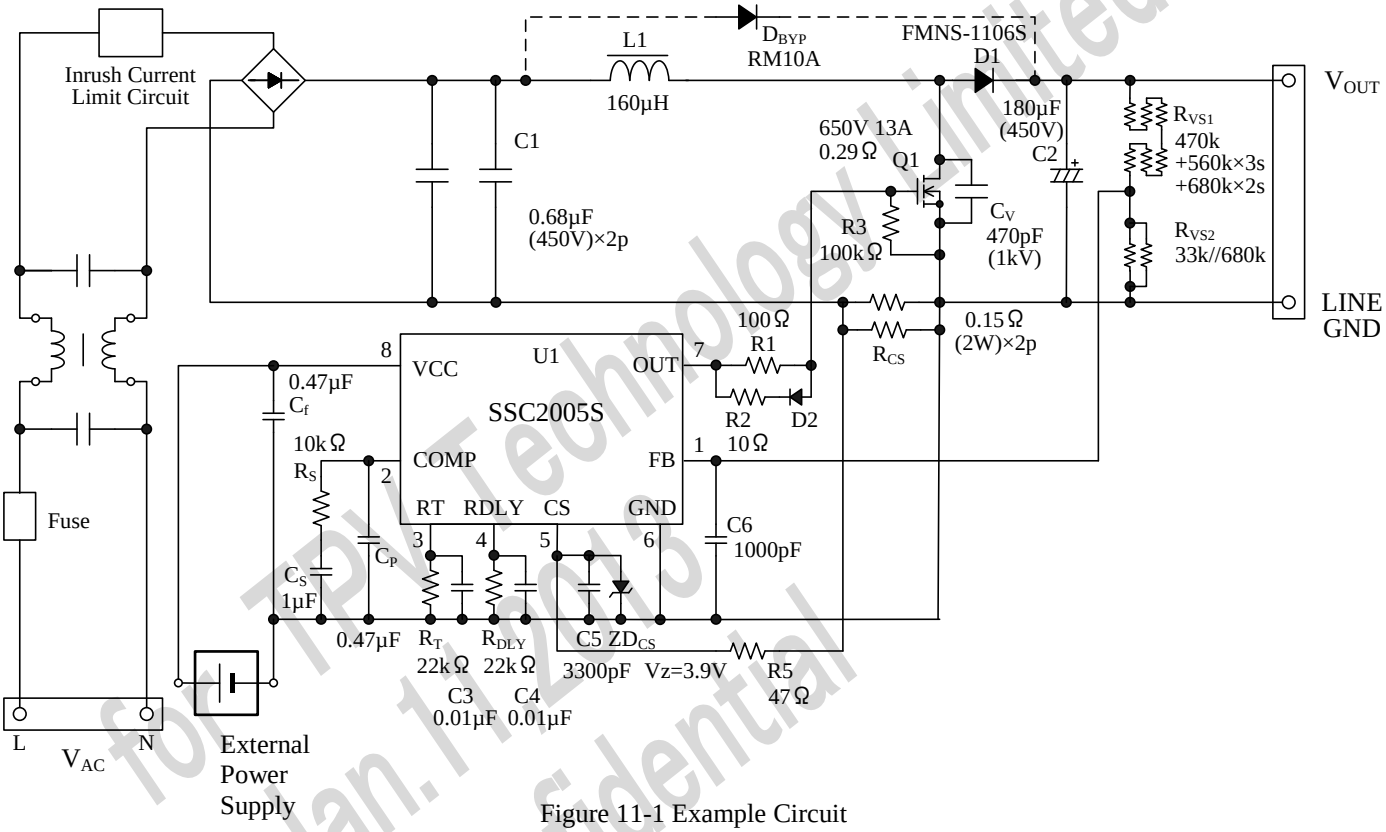


Figure 11-1 Example Circuit

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