SHARP

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To;

TENTATIVE SPECIFICATIONS

Product Type: Power Supply IC for LED Lighting

Model No.: IR3M92N4

※This tentative specifications contains 20 pages including the cover and appendix.
About the contents of this document, it may be changed for the characteristic improvement of the IC.

CUSTOMERS ACCEPTANCE

DATE:

BY:

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様式No.管7850-02

2. When using this product, please observe the absolute maximum ratings and the instructions for use outlined in these specification sheets, as well as the precautions mentioned below.
Sharp assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets, and the precautions mentioned below.

(Precautions)

(1) Please do verify the validity of this part after assembling it in customer's products, when customer wants to make catalogue and instruction manual based on the specification sheet of this part.

(2) This product is designed for use in the following application areas ;
- · OA equipment Audio visual equipment · Home appliances
- · Telecommunication equipment (Terminal) · Measuring equipment
- · Tooling machines · Computers

If the use of the product in the above application areas is for equipment listed in paragraphs (3) or (4), please be sure to observe the precautions given in those respective paragraphs.

(3) Appropriate measures, such as fail-safe design and redundant design considering the safety design of the overall system and equipment, should be taken to ensure reliability and safety when this product is used for equipment which demands high reliability and safety in function and precision, such as ;
- · Transportation control and safety equipment (aircraft, train, automobile etc.)
- · Traffic signals · Gas leakage sensor breakers · Rescue and security equipment
- · Other safety equipment

(4) Please do not use this product for equipment which require extremely high reliability and safety in function and precision, such as ;
- · Space equipment · Telecommunication equipment (for trunk lines)
- · Nuclear power control equipment · Medical equipment

(5) Please contact and consult with a Sharp sales representative if four are any questions regarding interpretation of the above four paragraphs.

3. Please contact and consult with a Sharp sales representative for any questions about this product.

Contents

1. General description

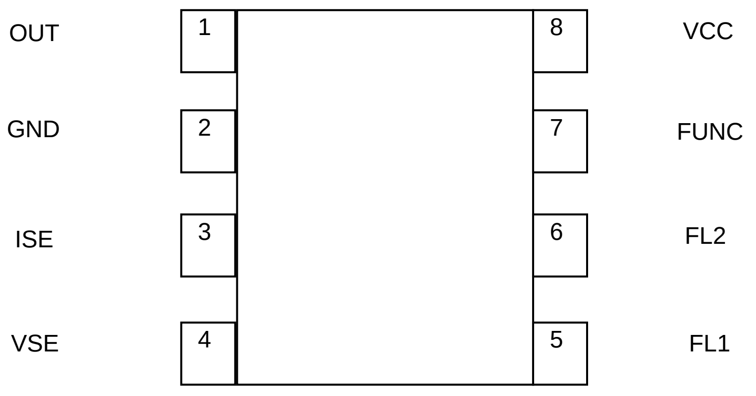
Model No. IR3M92N4 is a AC/DC power supply IC for LED lighting which built-in power factor improvement circuit, quasi-resonant operation circuit and PWM dimming circuit.

Primary-side control by transformer realizes the constant current operation suitable for LED lighting.

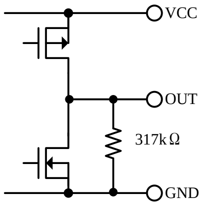
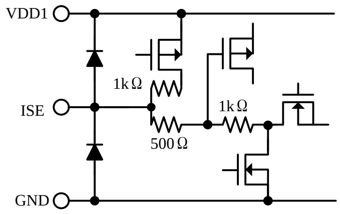
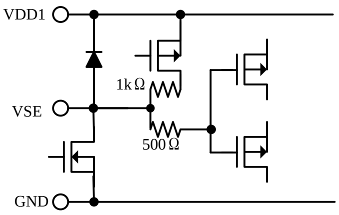
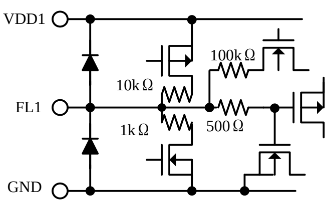
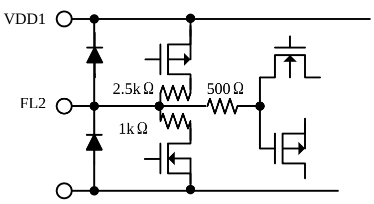
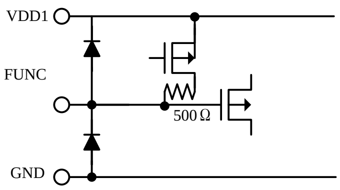
2. Features

(1) Input voltage range	:	10V to 18V *VCC=23V(Max.) at start up.
(2) Output current (LED current)	:	Constant current control
(3) Feature Function	:	Power factor improvement, quasi-resonant operation, PWM dimming operation and Stanby operation
(4) Error detection / Protection	:	VCC under voltage lock-out Output over voltage lock-out Over temperature protection Over current protection
(5) P-type silicon monolithic IC		
(6) Radiation-proof design	:	This product is not radiation-proof design.
(7) Lead finish	:	Lead Free
(8) 8 pin SOP plastic package		

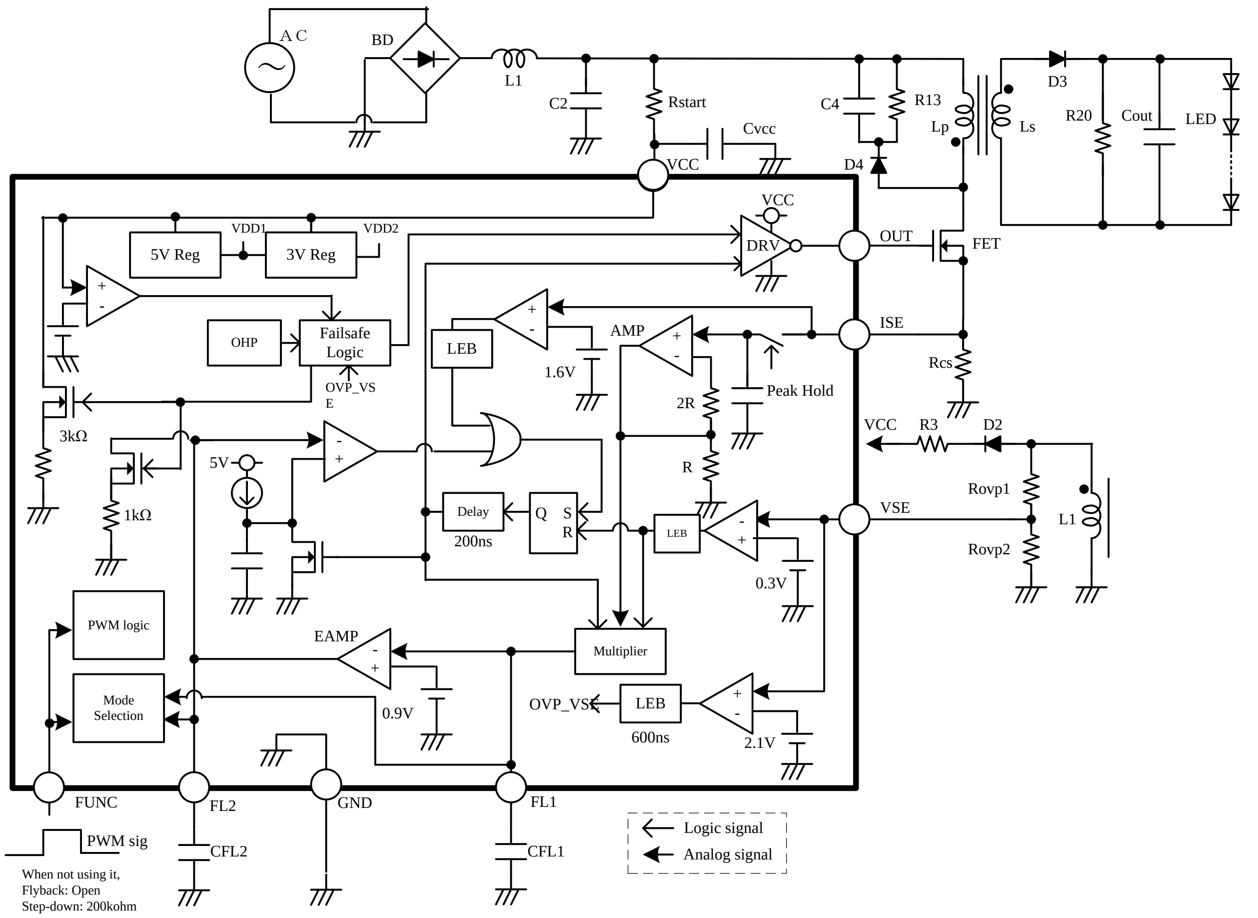
3. Pin assignment



4. Pin description

Pin name	Equivalent circuit	Pin description
①OUT		Gate drive for the external switching MOSFET
②GND		Ground terminal
③ISE		Current sense of the primary winding
④VSE		Voltage sense of the auxiliary winding
⑤FL1		The input terminal of error amplifier. Please connect capacitor CFL1 to this terminal.
⑥FL2		The output terminal of error amplifier. Please connect capacitor CFL2 to this terminal.
⑦FUNC		Mode setting terminal ・Flyback mode : Open ・Step-down mode : 200kohm ・PWM dimming input : pulse input ・Standby input terminal : GND
⑧VCC		Power Supply

5. Block diagram and basic connection diagram



6. Functional description

6-1 Constant current function

6-1-1 Concept of constant current operation (Flyback mode)

By monitoring VSE and ISE signals and controlling them, LED current (output current) can be controlled to be a constant level. Figure 6.2 shows FET Drain voltage, primary current and secondary current waveform during FET on and off. VSE signal is resistance-divided voltage of auxiliary winding output. Drain voltage waveform of FET and VSE waveform are same polarity and similar. As LED current (output current) is the average of secondary current, it is shown by equation (1).

$$\overline{Iout} = \frac{1}{2} \cdot Ipk2 \cdot \frac{Tres}{Tc} \qquad (1)$$

where Ipk2 : secondary peak current
Tres : period during secondary current flows
Tc : switching cycle

It is also shown by equation (2).

$$\overline{Iout} = \frac{1}{2} \cdot \frac{Np}{Ns} \cdot Ipk1 \cdot \frac{Tres}{Tc} \qquad (2)$$

where Np : primary winding turns
Ns : secondary winding turns
Ipk1 : primary peak current

As Np/Ns value is constant in equation(2), LED current (output current) can be controlled to be a constant value by keeping Ipk1・Tres/Tc constant. Ipk1 can be monitored by ISE terminal andTres can be monitored by VSE terminal.

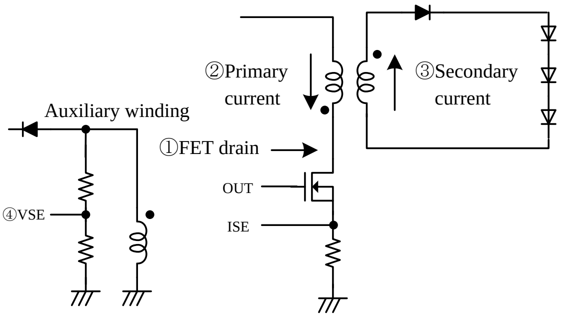


Figure 6.1 Circuit diagram

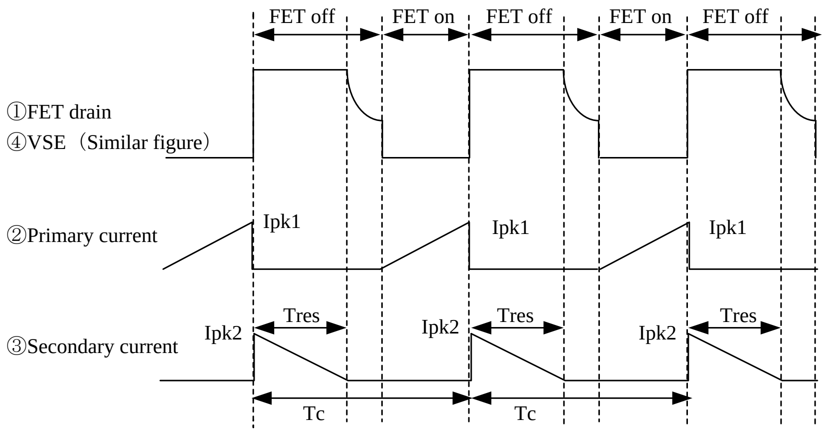


Figure 6.2 Waveform of each point of Figure 6.1 diagram

6-1-2 Constant current operation(Flyback mode)

IC operation, how to control LED current (output current) to be a constant value, is explained as below. Figure 6.3 shows block diagram relating constant current operation. As V_{ISE} is proportional to primary current and sensing resistance Rs, ISE terminal can monitor primary current. V_{PHOLD} is the output of peak hold circuit. It outputs the peak value of V_{ISE} every switching cycle, shown by equation (3).

$$V_{PHOLD} = Ipk1 \cdot Rs \qquad (3)$$

Multiplier divides Ipk1･Rs by Tres/Tc ratio.

$$V_{FL1} = Ipk1 \cdot Rs \cdot \frac{Tc}{Tres} \qquad (4)$$

Time constant of FL1 terminal should be set to much larger than switching period, where time constant of FL1 is decided by the resistance between the output of peak hold circuit and FL1 terminal (typ: 110 k ohm) and capacitor C_{FL1} connected to FL1 terminal. V_{FL1} shown by equation (4) is input of error amplifier, and is controlled to be equal to reference voltage Vref (0.9). FET on period is decided by the output of error amplifier.

In case of V_{FL1}< Vref , FET on period increases by VFL2 increase, which leads Ipk1 increase and V_{FL1} becomes to near Vref value. In case of V_{FL1}>Vref , FET on period decreases by VFL2 decrease, which leads Ipk1 decrease and V_{FL1} becomes to near Vref value. After all, V_{FL1} is controlled to be same value as Vref, and LED current (output current) is shown by equation (5), which is derived from equation (1), (2), (3), and (4).

$$\overline{Iout} = \frac{1}{2} \cdot \frac{Np}{Ns} \cdot \frac{Vref}{Rs} \qquad (5)$$

Equation (5) shows that LED current (output current) is decided by circuit constant value Np, Ns, and Rs.

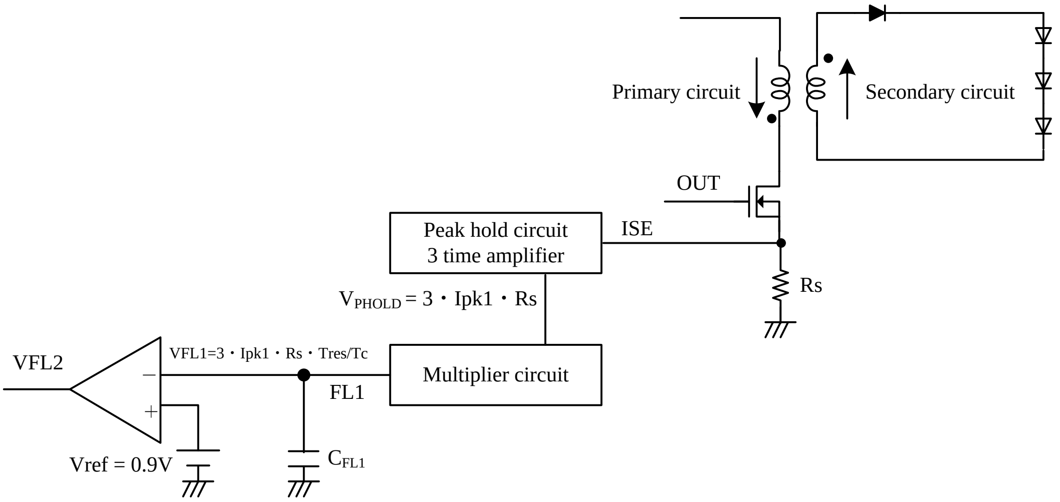


Figure 6.3 Block diagram relating constant current operation

6-2-1 Concept of constant current operation (Step-down mode)

Figure 6.4 shows FET Drain voltage, primary current and secondary current waveform during FET on and off. VSE signal is resistance-divided voltage of auxiliary winding output.

Drain voltage waveform of FET and VSE waveform are same polarity and similar. As LED current (output current) is the average of secondary current, it is shown by equation (6).

$$\overline{Iout} = \frac{1}{2} \cdot Ipk1 \qquad (6)$$

where Ipk1 : primary peak current

LED current (output current) can be controlled to be a constant value by keeping Ipk1 constant. Ipk1 can be monitored by ISE terminal andTres can be monitored by VSE terminal.

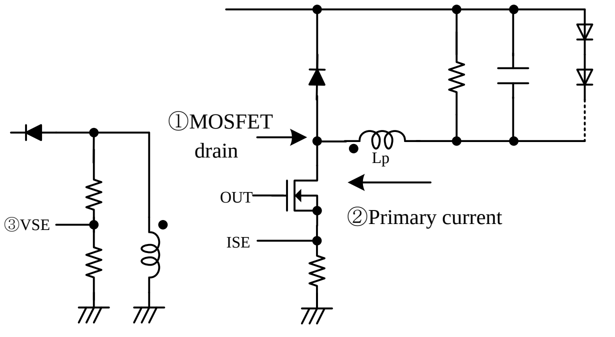


Figure 6.4 Circuit diagram

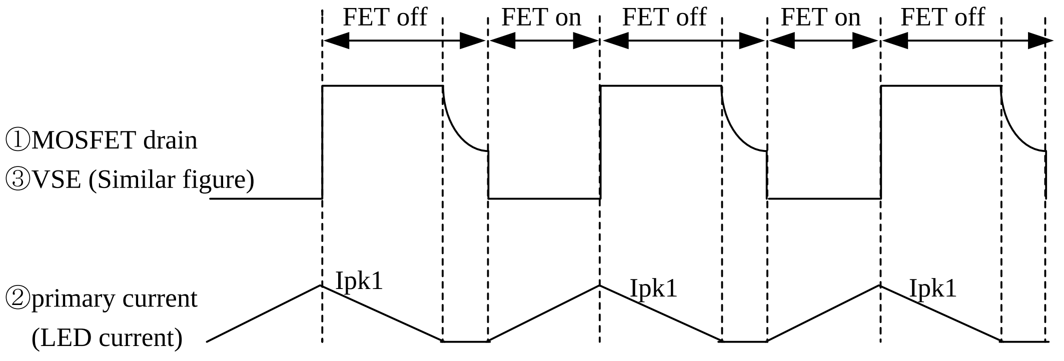


Figure 6.5 Waveform of each point of Figure 6.4 diagram

6-1-2 Constant current operation(Step-down mode)

IC operation, how to control LED current (output current) to be a constant value, is explained as below. Figure 6.6 shows block diagram relating constant current operation. As V_{ISE} is proportional to primary current and sensing resistance Rs, ISE terminal can monitor primary current. V_{PHOLD} is the output of peak hold circuit. It outputs the peak value of V_{ISE} every switching cycle, shown by equation (7).

$$V_{PHOLD} = Ipk1 \cdot Rs \qquad (7)$$

In Multiplier, VHOLD is outputted to FL1 terminal through internal 110kohm (TYP.).

$$V_{FL1} = Ipk1 \cdot Rs \qquad (8)$$

Time constant of FL1 terminal should be set to much larger than switching period, where time constant of FL1 is decided by the resistance between the output of peak hold circuit and FL1 terminal (typ: 110 k ohm) and capacitor C_{FL1} connected to FL1 terminal. V_{FL1} shown by equation (8) is input of error amplifier, and is controlled to be equal to reference voltage Vref (0.9). FET on period is decided by the output of error amplifier.

In case of V_{FL1}< Vref , FET on period increases by VFL2 increase, which leads Ipk1 increase and V_{FL1} becomes to near Vref value. In case of V_{FL1}>Vref , FET on period decreases by VFL2 decrease, which leads Ipk1 decrease and V_{FL1} becomes to near Vref value. After all, V_{FL1} is controlled to be same value as Vref, and LED current (output current) is shown by equation (9), which is derived from equation (6),(7) and (8).

$$\overline{Iout} = \frac{1}{2} \cdot \frac{Vref}{Rs} \qquad (9)$$

Equation (9) shows that LED current (output current) is decided by circuit constant value Rs.

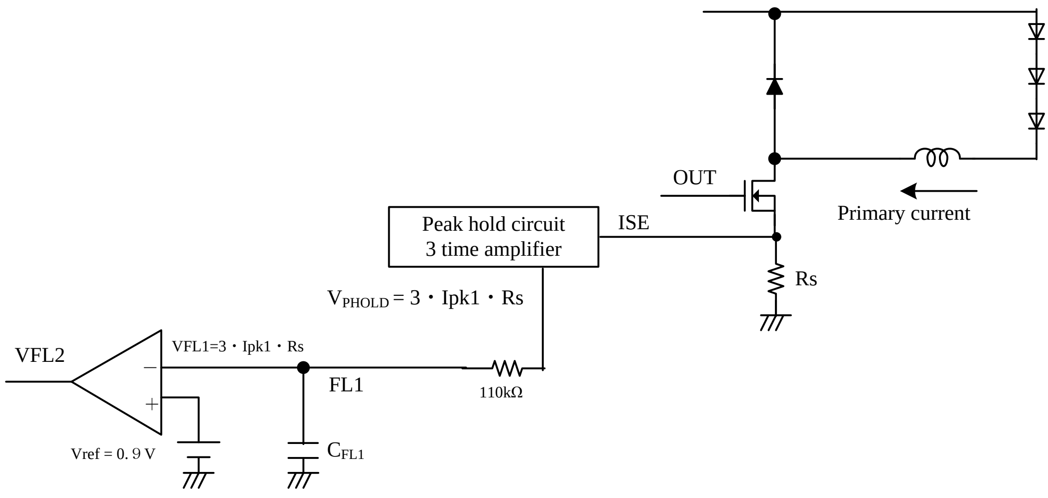


Figure 6.6 Step-down block diagram relation constant current operation

6-2 Power factor improvement by FET constant on-time control

Power factor improvement is explained as below. Changing period of FET on-time and flattery period of error amplifier are controlled to be much longer, compared to AC period (1/50Hz or 1/60Hz). As time constant of FL2 terminal shown by equation (10) is much larger than AC period, FET on-time can be considered to constant value during one AC cycle. where time constant of FL2 is decided by the output resistance of error amplifier 78kohm (TYP.) (@FL1=0.9V±0.3) and capacitor C_{FL2} connected to FL2 terminal (ex. 1uF).As Ton is constant value in equation (11), Ipk1 is proportional to Von.

$$\tau = R \cdot C = 78k\Omega \cdot 1uF = 0.078s \quad > 0.01s@AC50Hz \qquad (10)$$

$$Ipk1 = \frac{Ton}{L} \cdot Von = \alpha \cdot Von \qquad (11)$$

where L : primary winding inductance

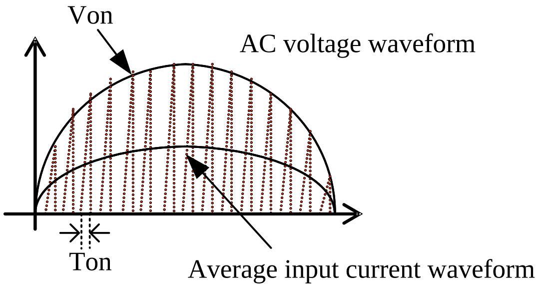


Figure 6.7 Power factor improvement

6-3 EMI improvement by quasi-resonant operation

EMI improvement by quasi-resonant operation is explained below. This IC operates in critical conduction mode. If it operates in discontinuous mode, after releasing transformer's energy, ringing occurs by parasitic inductance and capacitor of the transformer and FET, as shown in Figure 6.8. This ringing generates EMI noise. The moment when transformer release its energy completely is detected by VSE terminal, and this IC turns on FET at the bottom point of ringing waveform (quasi-resonant operation) as shown in Figure 6.9. Therefore this IC can minimizes EMI noise.

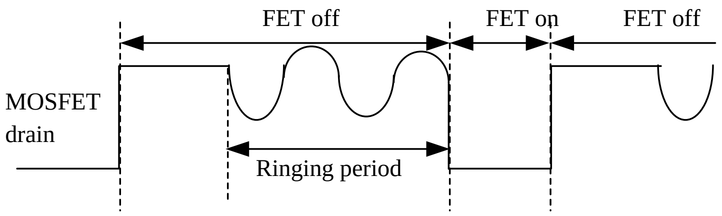


Figure 6.8 When FT is not driven on transition mode

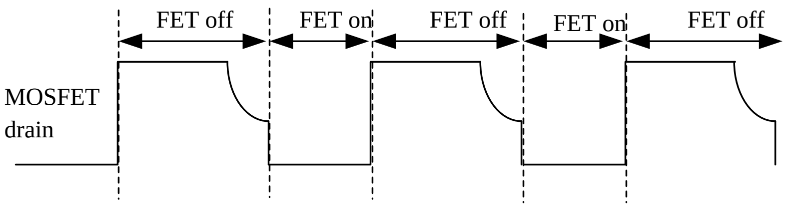


Figure 6.9 Quasi-resonant operation

6-5 Mode Judging Circuit

It is necessary to set up a FUNC terminal according to operational mode.
The input circuit of a FUNC terminal is shown in Fig. 6.10.
In the case of the flyback mode, please make a FUNC terminal open.
The example of connection of PWM dimming operation is indicated to Fig. 6.10.

Mode	FUNC terminal
Flyback	5V>FUNC>3.1V
Step-down	2.9V>FUNC>1.4V
Stanby	0.9V>FUNC（※）

（※） It is necessary to input the voltage beyond 1.3V into the return from standby mode at FUNC terminal.

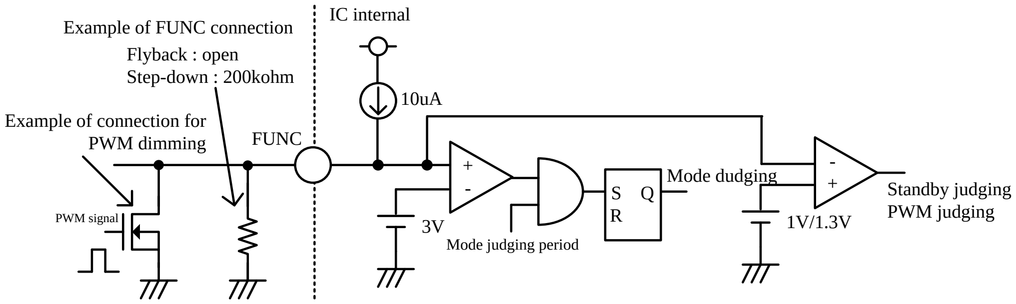


Figure 6.10 FUNC terminal input circuit diagram

A mode judging sequence is shown in Fig. 6.11.
In a-point, Va is starting voltage and it starts it by VCC=18V (TYP.).
MOSFET switching is started after a mode judging (a-point~b-point).
in FUNC terminal, PWM dimming becomes effective after a mode judging.

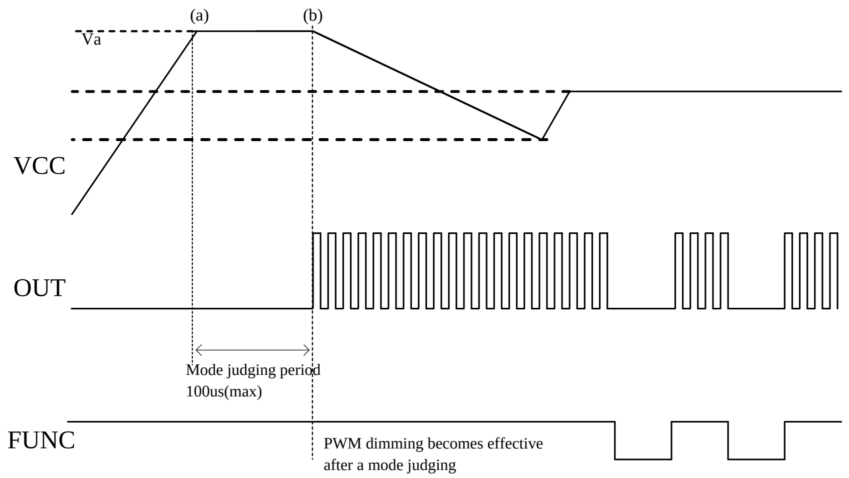


Figure 6.11 Mode judging sequence

A standby mode sequence is shown in Fig. 6.12.
When judged with standby mode in a mode judging period (a-point~b-point), a switching stop is kept.
operation is stopped at Vb(UVLO voltage 6.5V (TYP.)), and the operation which will restart
if the starting voltage 18V (TYP.) is reached ,is repeated.
The return from standby mode is carrying out a FUNC terminal more than 1.3V (e-point),
discharges the capacity connected to VCC and becomes normal operation from the following restart timing (g-point).

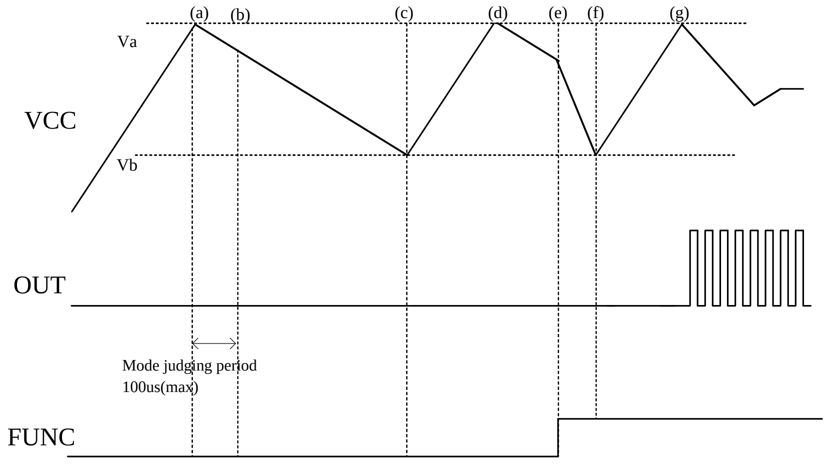


Figure 6.12 Standby mode sequence

6-6 PWM dimming Function

LED output current can be adjusted according to the PWM signal inputted into a FUNC terminal.
The input condition of the PWM signal of a FUNC terminal becomes as follows, and shows operation in Fig. 6.13.

FUNC terminal	
5V>FUNC>1.3V	OUT: switching
1V>FUNC	OUT: OFF(※)

(※) In FUNC < 1V , the value of FL1 and FL2 is kept and the switching-on pulse is kept constant.

When a PWM function is used, please use it after are satisfactory or checking enough with the system, since sound may occur with a transformer, a coil, etc.

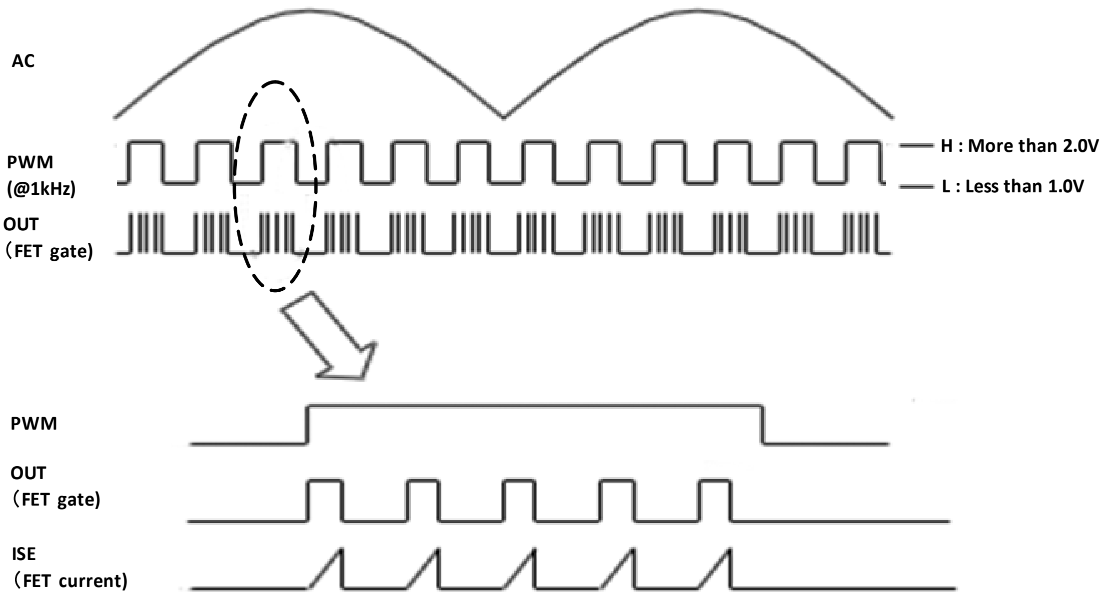


Figure 6.13 PWM dimming function

6-7 Error detection/Protection function

Over temperature protection, VCC under voltage lock-out, output Over voltage lock-out and Over current protection are built in this IC.

6-7-1 Over temperature protection

When junction temperature of this IC is over 150℃, thermal error is detected and following operation is performed.

- IC shut down
- Discharge CFL2 (Capacitor connected to CFL2)
- Discharge capacitor connected to VCC
- Discharge stops when VCC goes down to UVLO (6.5V)

6-7-2 VCC under voltage lock-out

IC operation stops when VCC voltage goes down to 6.5V(typ.) or less, because of VCC voltage down or short between VCC and GND. IC operation restarts when VCC voltage goes up to 18V or more (start up voltage).

6-7-3 Output over voltage lock-out

When VCC terminal and VSE terminal goes up to VOVP (Over voltage threshold voltage) or more, over voltage error is detected and following operation is performed.

- IC shut down
- Discharge CFL2 (Capacitor connected to CFL2)
- Discharge capacitor connected to VCC
- Discharge stops when VCC goes down to UVLO (6.5V).

Over voltage error is detected by VCC terminal voltage (typ. 23V) and VSE terminal voltage (typ. 2.1V). Over voltage threshold voltage is shown by equation (12).

$$V_{OVP\_VSE} \geqq 2.1V(TYP.) \ \& \ V_{OVP\_VCC} \geqq 23V(TYP.) \qquad (12)$$

where V_{OVP_VCC} : Over voltage threshold voltage for VCC
V_{OVP_VSE} : Over voltage threshold voltage for VSE

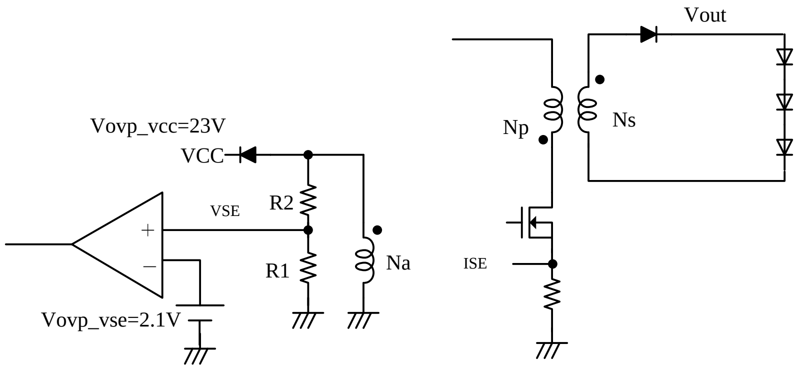


Figure 6.14 Circuit diagram

6-7-4 FET over current protection

When FET current goes up to VOCP (Over current threshold voltage) or more, over current error is detected and following operation is performed.

Cycle by cycle over current limit operation (default configuration).

- OUT turns Low and stops switching.
- IC do not shut down.
- OFF period will be more than 67us (typ.).

A waveform is shown in Fig. 6.16.

The voltage of ISE terminal at over-current detection is as follows .
The circuit configuration of over-current detecting is shown in Fig. 6.15.

Mode	over-current detection volgate
Flyback	ISE ≦ 1.6V(TYP.)
Step-down	ISE ≦ 0.8V(TYP.)

Over Current is detected by ISE terminal voltage(typ 1.6V). Over Current threshold voltage is shown as the figure below.

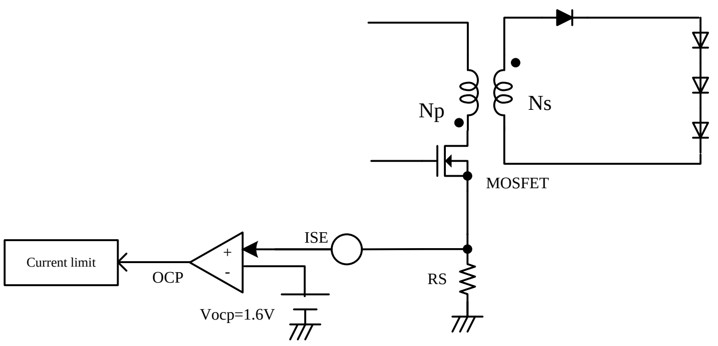


Figure 6.15 Circuit diagram relating over current protection

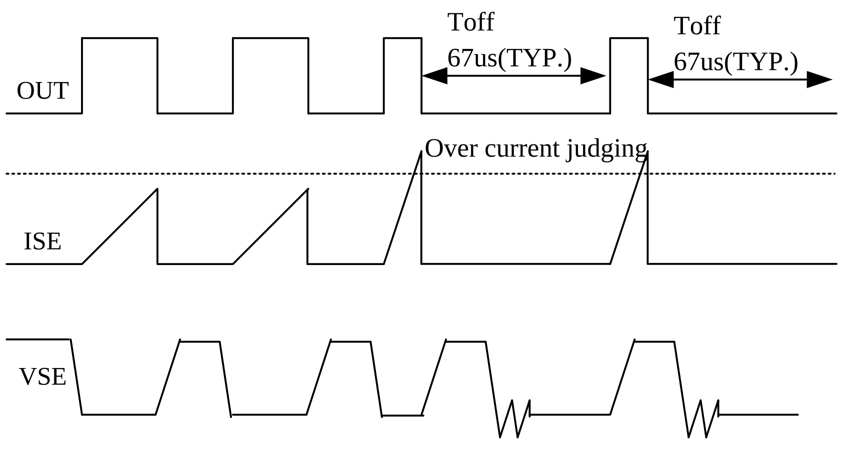


Figure 6.16 Over current judging waveform

6-8 Start-up sequence

Figure 6.17 shows start-up sequence waveform. This IC starts up at point (a) in Figure 6.9 and Va is start up voltage, typ. 18V. MOSFET switching is started after a mode judging (a-point~b-point).
Then
auxiliary winding starts to supply power to IC. Capacitor CVCC which is connected between VCC and GND should be adjusted so that Vc, VCC voltage at point (c) ,does not go down below VCC undervoltage lock-out threshold (6.5V).
Example) Cvcc: 10uF @Vout35.5V, Iout700mA

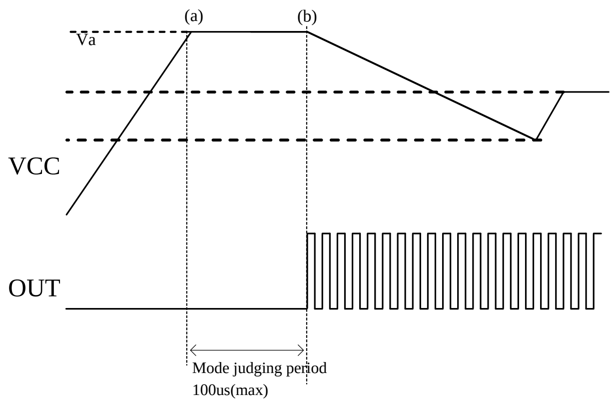


Figure 6.17 Start-up sequence

7. Precautions

7-1 FL1 and FL2 terminal

The value shown below is recommended for capacitor connected to FL1 and FL2.

- CFL1 = 0.1uF ～ 1uF
- CFL2 = 0.2uF ～ 2uF
- CFL1 ≦ CFL2 * 0.5

8. Absolute maximum ratings

Absolute maximum ratings are values or ranges which can cause permanent damage. Please do not exceed this range even when start up or shut down.

Ta=25℃

Parameter	Symbol	Rating	unit	Applied terminal	Conditions
Power Supply Voltage	Vcc	-0.3 ～ 28.0	V	VCC	
Input Terminal Voltage	VI1	-0.3 ～ 6.0	V	FL1, FL2, ISE, VSE, FUNC	
Output Terminal Voltage	VO1	-0.3 ～ 20.0	V	OUT	
Power Dissipation *	PD	T.B.D.	mW		Ta =25℃
Thermal Resistance *	θa	T.B.D.	℃/W		
Operating Temperature	TOPR	-30 ～ 100	℃		
Storage Temperature	TSTG	-40 ～ 150	℃		

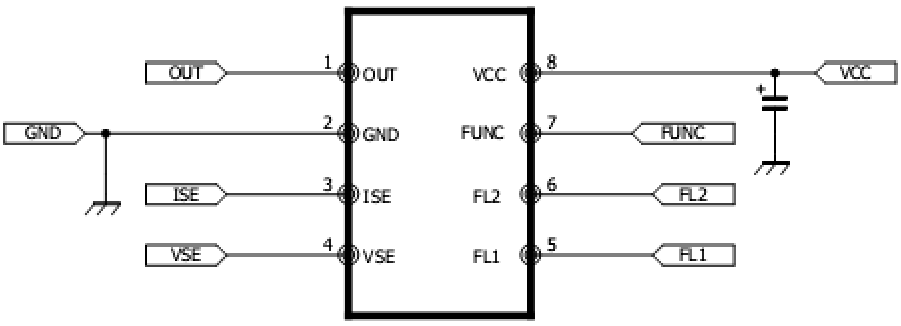
*Measured on JEDEC-JESD51-7 4-layer board.

9. Electrical characteristics

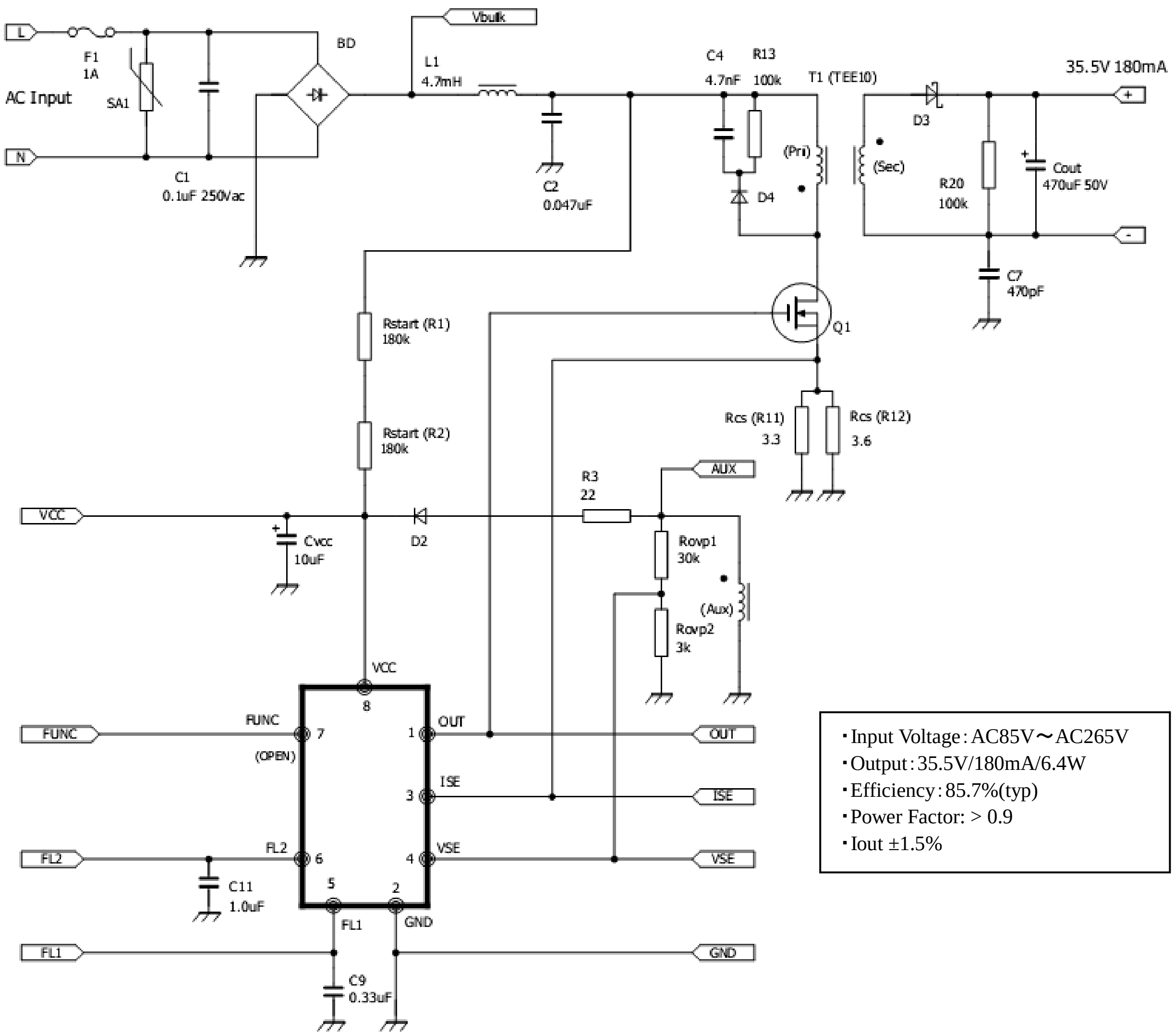
Unless otherwise specified, condition shall be GND=ISE=VSE=0V,VCC=12V, Ta=25℃.

Parameter	Symbol	MIN	TYP	MAX	Unit	Conditions
VCC section						
VCC Input Voltage	VCC1	10	12	18	V	
VCC Startup Current	ICC1	—	30	100	uA	VCC=Startup voltage – 0.1V
VCC Operating supply current	ICC2	—	1.0	2.0	mA	
VCC Turn on threshold	Vst	15.5	18	19.5	V	
VCC Turn off threshold	Vuvlo	5.5	6.5	7.5	V	
Gate driver section						
Output Low Resistance	RL	—	—	15	Ω	OUT-0.1V
Output High Resistance	RH	—	—	60	Ω	OUT+0.1V
Oscillator section						
Frequency	fosc	T.B.D.	210	T.B.D.	kHz	FL2=2.5V
Error Amplifier Section						
Reference Voltage	VREF	T.B.D.	3.00	T.B.D.	V	
Feedback Voltage	VFB	T.B.D.	900	T.B.D.	mV	VSE=1V,FL2=2.5V
Transconductance	Gm	—	43	—	uA/V	FL1=0.9V
FL2 Operating range	Vfl2	0.5	—	4.0	V	
Zero Cross Detect Section						
VSE Threshold Voltage	VVSE	0.2	0.3	0.4	V	FL2=2.5V
FUNC section						
Threshold Voltage of Flyback mode	VFLY	3.1		5.0	V	
Threshold Voltage of StepDown mode	VStepD	1.4		2.9	V	
Threshold Voltage of Stanby mode	Vstby			0.9	V	
Threshold High Voltage of PWM	VPWMH	1.4			V	
Threshold Low Voltage of PWM	VPWML			0.9	V	
FUNC Bias Current	IFUNC	T.B.D.	10	T.B.D.	uA	
Over Current Protection Section						
Threshold Voltage of Flyback	VOCP_FLY	1.4	1.6	1.8	V	FL2=2.5V
Threshold Voltage of StepDown	VOCP_StepD	0.7	0.8	0.9	V	FL2=2.5V
Minimum Off Time in OCP	tmin	T.B.D.	67	T.B.D.	us	
Leading edge blanking time	tleb1	—	200	—	ns	
Over Voltage Protection Section						
Threshold Voltage of VSE	VOVP_VSE	1.9	2.1	2.3	V	
Threshold Voltage of VCC	VOVP_VCC	22	23	24	V	
Leading edge blanking time	tleb2	—	600	—	ns	
Over Temperature Protection Section						
Threshold Temperature	TSD	135	150	165	℃	Junction temperature

10. Test Circuit

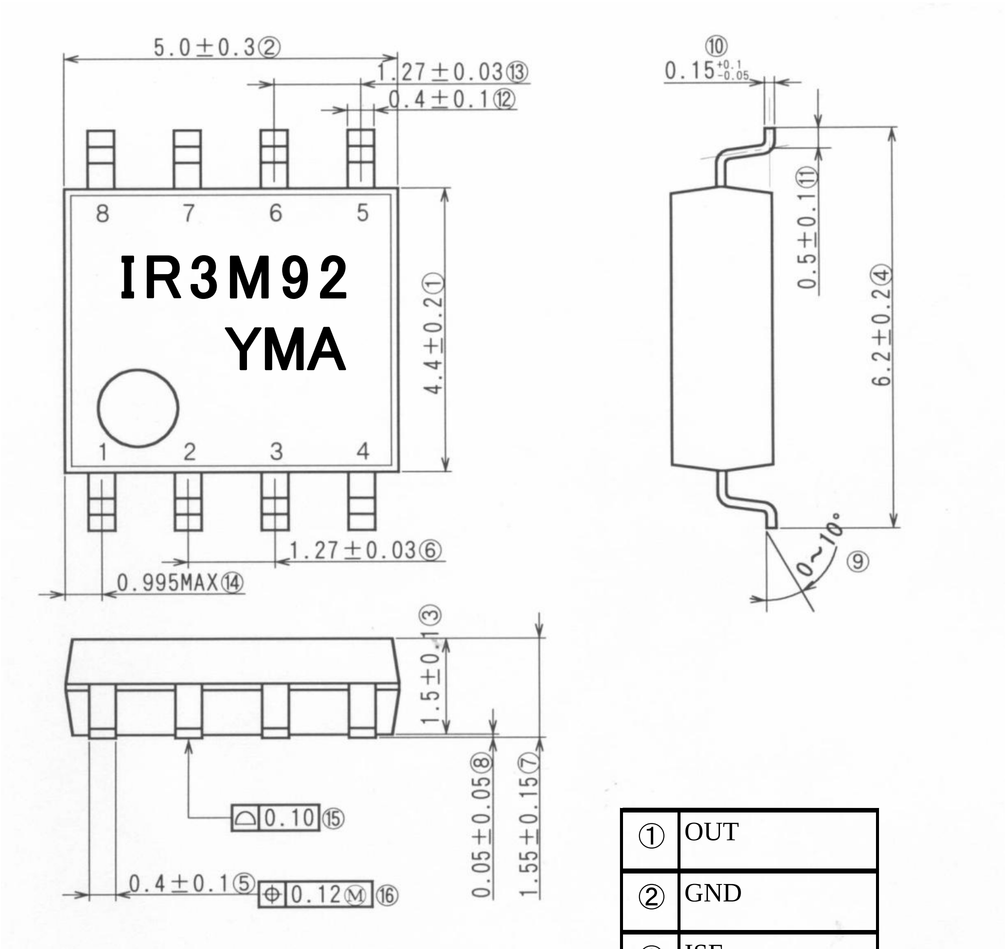


11. Application circuit example



- Input Voltage: AC85V～AC265V
- Output: 35.5V/180mA/6.4W
- Efficiency: 85.7%(typ)
- Power Factor: > 0.9
- Iout ±1.5%

12. Package



Date code:
Y:Year code
M:Month code
A:Ref code

①	OUT
②	GND
③	ISE
④	VSE
⑤	FL1
⑥	FL2
⑦	FUNC
⑧	VCC