The Application Note of AP3968/69/70

(Not open yet-bcd semi)

1. Introduction

The AP3968/69/70 series of power switcher circuits consist of a primary side regulation controller and a high voltage transistor, and is specially designed for offline power supplies within 12W output power. Typical applications include charger for mobile phone, adapter for ADSL and special power supplies of small appliance for linear replacement. The AP3968/69/70 operates at pulse frequency modulation (PFM), AP3968/69/70 solution has fewer component numbers, smaller size, and lower total cost.

The main difference among AP3968, AP3969 and AP3970 are package types, high voltage transistor and power stage.

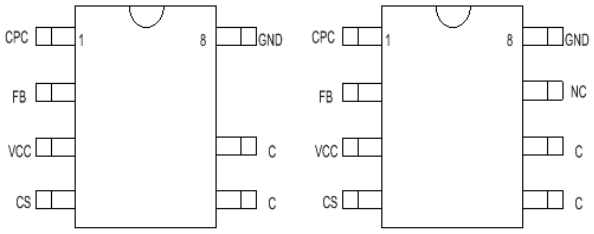
Types	Package	VCES	ICDC	85V~264VAC	195V± 264V
AP3968	SOP-7L	700	1.5A	4.5W	6W
AP3969	DIP8	700	1.5A	7.5W	11W
AP3970	DIP8	700	4.0A	12W	15W

This application note describes features of the PSR switchers, and a design example with detailed parameters is presented.

2. Features

- Power switcher with primary side control
- Built-in NPN Transistor with 700VCBO
- Built-in line compensation for ± 7% current tolerance
- Built-in cable compensation for ± 5% voltage tolerance
- 100mW less standby power
- EPS 2.0 compliant with higher margin
- Built-in OVP/OTP/OCP/SCP functions
- Meet HV creepage requirements
- Audible noise free solution under whole operating range.
- Low cost solution for its less component count
- Applications: Charger/Adapters/STB/Home appliances

3. Pin Configurations



AP3968 (SOP-7L) AP3969/70 (DIP8)

Figure 1, the Pin Description of AP3968/69/70

4. Pin Description

Pin No.	Symbol	Description
1	**CPC**	This pin is connected a capacitor to GND to serve as cable compensation.
2	**FB**	The voltage feedback is from auxiliary winding
3	**VCC**	This pin receives rectified voltage from the auxiliary winding of the transformer. The voltage range is from 6V to 22V during normal operation
4	**CS**	Current sense for primary side of transformer
5,6	**C**	This pin is connected with an internal power BJT's collector
7	**NC**	Not connected
8	**GND**	This pin is the signal reference ground

5. Function Blocks

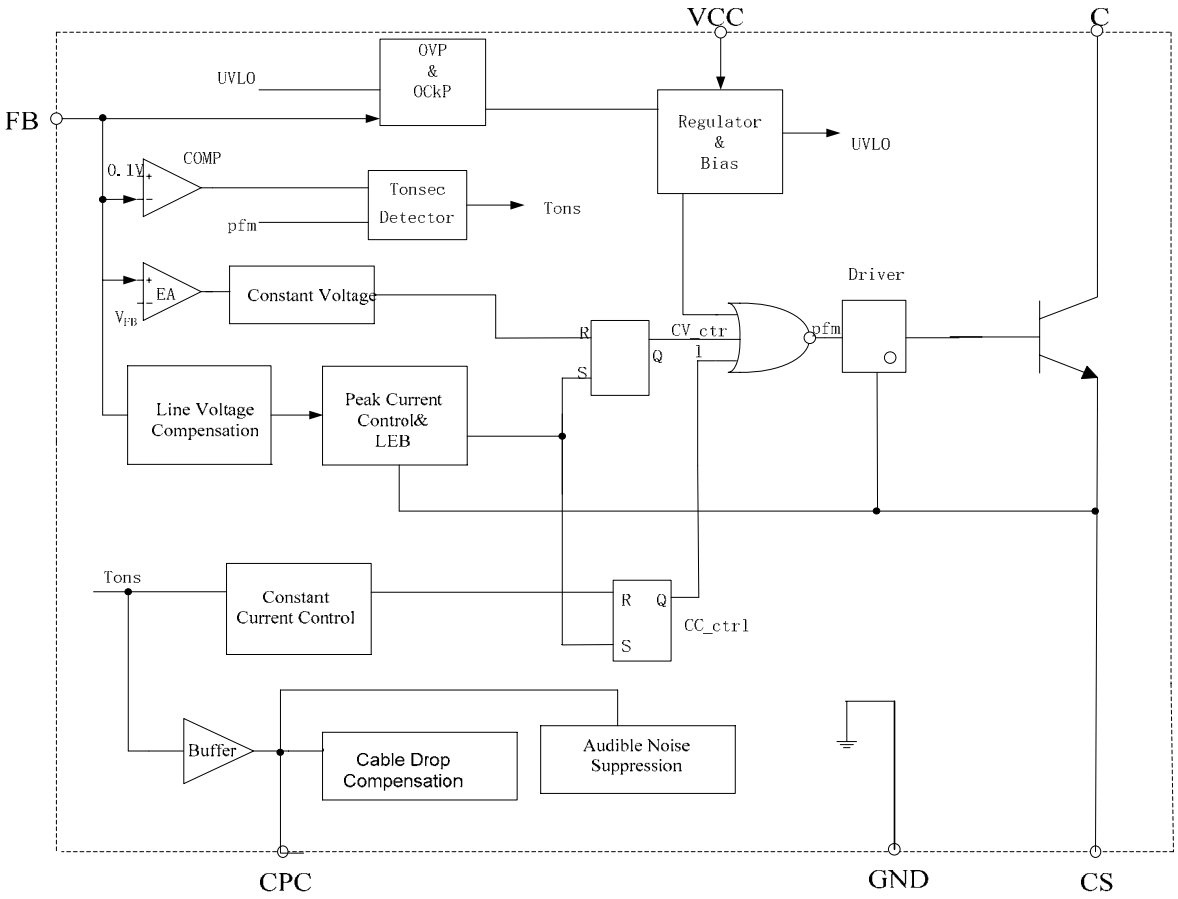


Figure 2, Function Block Diagram of AP3968/69/70

3, Design Considerations

3.1 Constant Voltage Design

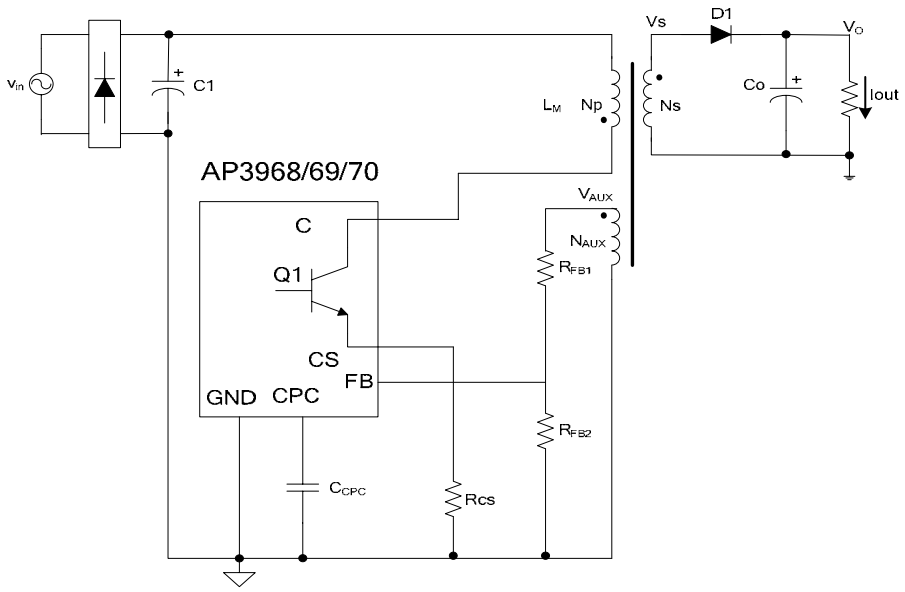


Figure 3 illustrates a simplified flyback converter with AP3968/69/70.

The feedback resistors consist of R_{FB1} and $R_{FB2,}$ as shown in figure 3, Constant Voltage

$Vo=V_{FB}\cdot(1+R_{FB1}/R_{FB2})\cdot N_S/N_{AUX}-Vd$ (1)

3.2. Constant Current Design

$$Ipk = \frac{0.5V}{R_{CS}} \quad (2)$$

$$Iout = \frac{2}{7}\cdot\frac{N_P}{N_S}\cdot Ipk \quad (3)$$

3.3 The feedback resistor selection for the tradeoff between Line Voltage Compensation and Cable compensation

The pull up resistor R_{FB1} is related with line and cable compensation.

The higher R_{FB1} will enhance line compensation (Lower deviation of CC between 85VAC and 264VAC); otherwise, maximal current under higher voltage is probably lower than the value under lower voltage if the resistor is too lower. The lower value of R_{FB1} is benefit for cable compensation (better CV).

15K-36K of RFB1 is usually recommended for most applications.

3.4 Thermal Design

The power loss of AP3968/69/70 mainly includes operating loss of control device, conduction loss (marked as Pcon) and switching loss (marked as Psw) of power device.

The ON state voltage includes a junction voltage VO and the voltage across the drift region which is characterized by the dynamic resistance RO. VO and RO can be obtained from the manufacturer's datasheet or through sample testing. The conduction loss can be calculated as follows:

$Pcon=Iavg*Vo+I^2*Ro$ (4)

Switching loss contains turn on and turn off loss,

Psw=(Eon+Eoff)*frequency. (5)

3.5 PCB layout consideration.

Larger area of copper for "GND" and "C" pin are used as heatsink. Figure 4 is a actual example using AP3969, the higher area of both the Collector "C" and ground "GND" are required.

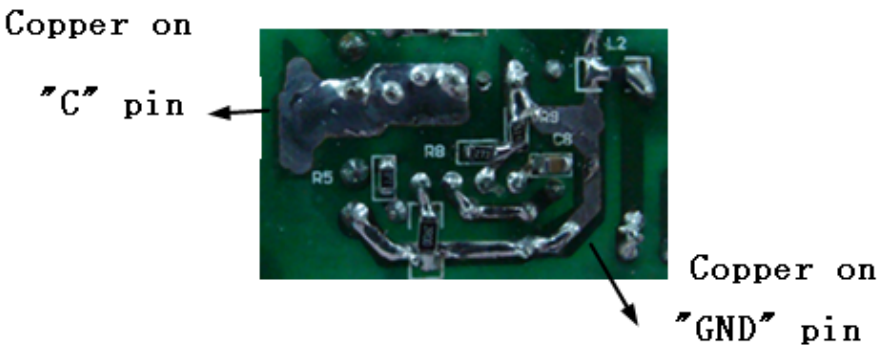


Figure 4, the PCB ofAP3969

3.6 Tons consideration.

The recommended sample time that is defined as Ts, and the waveform on the two side of transformer's secondary winding is shown in Figure 5.

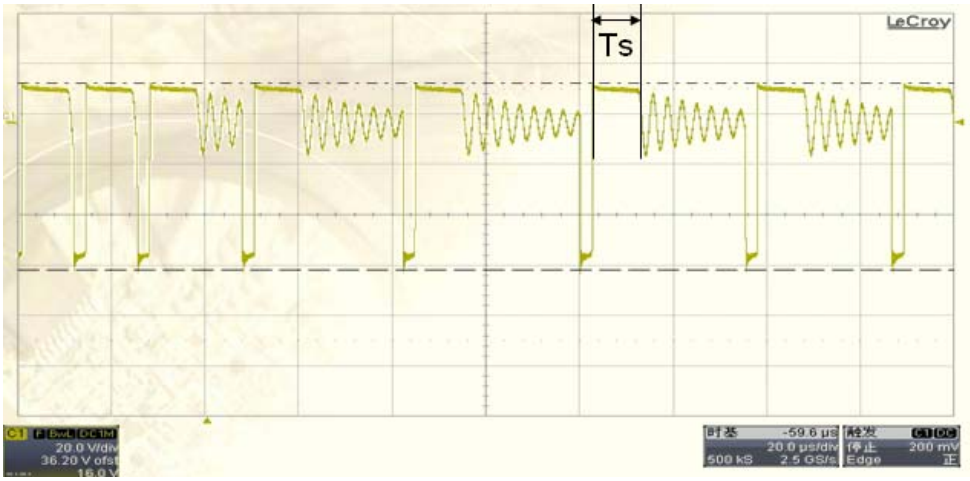


Figure 5. The waveform on the two side of transformer's secondary winding.

It is required that the minimal Tons is 9.5uS under full load.

3.7. Audible Noise suppression of the system solution.

The power supply system with AP3968/69/70 can have lower audible noise that is acceptable by most people. Compared with controller employing common pulse frequency modulation, the built-in noise suppression module in AP3968/69/70 will help to double switching frequency when load decreases below a given level.

A power supply system with AP3968/69/70 easily pass audible noise test when its transformer is dipped paint.

4. Design Example-transformer design

4.1 Table 1, the spec of a 6.3W adapter is designed as follows:

	Symbols		Unit
Input Line Voltage Range	V_{ac-rms}	90 ~264	VAC
Ac Line frequency	f_{ac}	47~63	HZ
Maximum output power	P_{OM}	6.3	W
Output Voltage	Vo	9	V
Output Current	Io	0.7	A
Conversion Efficiency	η	73.8	%
Load Regulation	$\Delta V_{OUT}/V_{OUT}$	±5	%
Line Regulation	$\Delta V_{OUT}/V_{OUT}$	±5	%
Standby Power Dissipation	P_{ST}	0.3	W

4.2 DC link capacitor

Except for table 1, there are other symbols as follows:

Table 2, the partly symbols and their meaning in this paper

Symbols	Meaning
V_{ac-rms}	RMS value of input voltage
V_{ac-min}	Minimal value of line voltage
V_{dc-min}	Minimal value of rectified line voltage by bridge diode
C_{DC}	DC link capacitor
η	Conversion efficiency of adapter system

AC line voltage is rectified by bridge diode and filter by the DC link capacitor. The DC link capacitor can be calculated by:

$$C_{DC} \geq \frac{P_{OM}}{\eta \bullet f_{ac} \bullet (2V_{ac\text{-}min}^2 - V_{dc-min}^2)} \quad (6)$$

In general, we can suppose that $V_{ac\_min}=0.71 \bullet V_{ac\_rms}$, $V_{dc\_min}=1.4 \bullet V_{ac\_rms}$, then C_{DC} value can be calculated.

In this design, select two 10μF capacitor in parallel as C_{DC}.

4.3 Duty cycle

When the switch turns off, the reflected output voltage added to the transformer primary side is calculated by:

$$V_{RO} = \frac{D_{MAX}}{1 - D_{MAX}} \cdot V_{DCMIN} \quad (7)$$

When V_{DC} is at its minimum value, D_{MAX} is at its maximum value. It is suggested that the maximum duty cycle is less than 0.5.

The internal transistor CE junction voltage in off state is:

$$V_{CE} = V_{DC} + V_{RO} \quad (8)$$

By reducing D_{MAX}, V_{CE} can be lower. The typical D_{MAX} is 0.45. Figure 6 shows the transistor CE junction voltage when turns off.

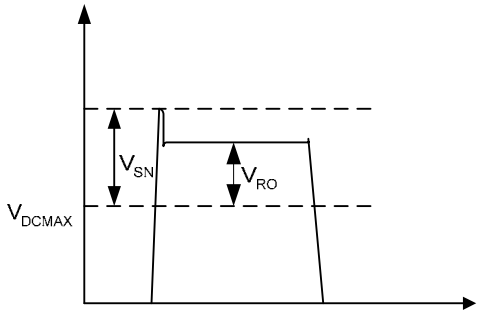


Figure 6. Internal Transistor CE junction voltage when turns off

4.4 Transformer design

The Flyback topology can works in DCM or CCM mode. When working in DCM mode, the transistor peak conduction current is:

$$I_{C(PK)} = \frac{2P_{IN}}{V_{DCMIN} \cdot D_{MAX}} \quad (9)$$

The maximum RMS current through transformer primary winding is:

$$I_{PRMS(MAX)} = I_{C(PK)} \cdot \sqrt{\frac{D_{MAX}}{3}} \quad (10)$$

Figure 7 shows the transistor conduction current during a switching cycle.

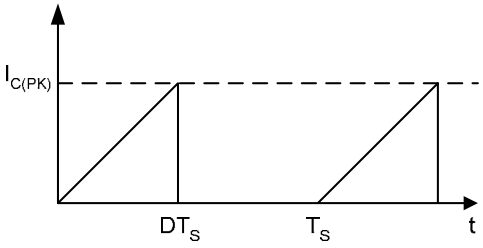


Figure 7. Transistor conduction current during a switching cycle

The transformer primary inductance is defined by:

$$L_P = \frac{(V_{DCMIN} \cdot D_{MAX})^2}{2P_{IN} \cdot f_{SW}} \quad (11)$$

After calculated the transformer primary inductance, we can select a proper core for the transformer. There are many design guidelines to select the core type like AP method. Here we omit this procedure.

Then the minimum turns of transformer primary can be calculated by

$$N_{PMIN} = \frac{L_P \cdot I_{C(PK)}}{B_S \cdot A_E} \quad (12)$$

Here B_S is the saturation flux density and A_E is the core effective area.

The turn's ratio of the transformer primary winding to the first output winding is:

$$n = \frac{N_P}{N_{S1}} = \frac{V_{RO}}{V_{O1} + V_{F1}} \quad (13)$$

Where V_{O1} is the first output voltage, V_{F1} is its diode conduction voltage.

We can first define N_{S1}, and then according to (8), N_P is calculated. N_P should be larger than N_{PMIN} to ensure the core not saturated.

The VCC winding turns is calculated by:

$$N_{VCC} = \frac{V_{CC} + V_{F2}}{V_{O1} + V_{F1}} \cdot N_{S1} \quad (14)$$

V_{F2} is the VCC output diode conduction voltage. The VCC voltage is set 12V in (10).

The first output winding RMS current is:

$$I_{O1RMS} = I_{PRMS} \cdot \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \cdot \frac{V_{RO} \cdot P_{O1}}{(V_{O1} + V_{F1}) \cdot P_O} \quad (15)$$

The suggested current density is 6~10A/mm^2 and use litz wire to minimize skin effect for high current output.

4.5 Output Rectify Diode

The maximum voltage and RMS current of the output rectify diode are:

$$V_{D1} = V_{O1} + \frac{V_{DCMAX} \cdot (V_{O1} + V_{F1})}{V_{RO}} \quad (16)$$

$$I_{DRMS} = I_{O1RMS} = I_{PRMS} \cdot \sqrt{\frac{1 - D_{MAX}}{D_{MAX}}} \cdot \frac{V_{RO} \cdot P_{O1}}{(V_{O1} + V_{F1}) \cdot P_O} \quad (17)$$

4.6 Output Capacitor

The ripple current of the output capacitor is:

$$I_{CORMS} = \sqrt{(I_{DRMS})^2 - I_O{}^2} \quad (18)$$

The voltage ripple on the output 1 is:

$$\Delta V_{O1} = \frac{I_{O1} \cdot D_{MAX}}{C_{O1} \cdot f_{SW}} + \frac{I_{C(PK)} \cdot V_{RO} \cdot ESR_{CO} \cdot P_{O1}}{V_{O1} + V_{F1}} \quad (19)$$

5. Typical Application Circuit -9V/0.7A Adapter

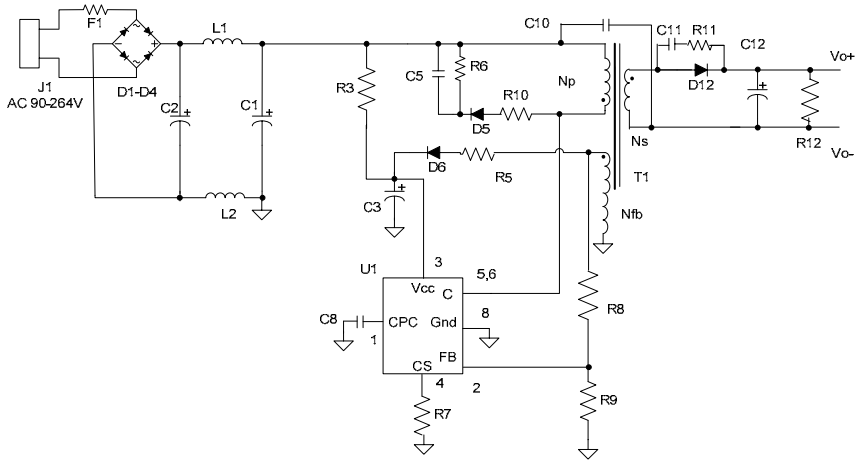


Figure 8. Typical Adapter Application with 9V/0.7A Output

Table 3, Bill of the 9V/0.7A Adapter

Item	Description	QTY	Item	Description	QTY
C1	10.0uF/400V, electrolytic	1	U1	AP3969, DIP-8	1
C2	4.7uF/400V, electrolytic	1	F1	11 ohm,2W	1
C3	3.3uF/50V, electrolytic	1	R3	3.3M ohm /0.25W	1
C5	1nF/1kV, ceramic	1	R5	3.9 ohm ,0805	1
C8	0.68uF, 0805	1	R6	150 Kohm, 1206	1
C10	1nF/250Vac, Y1 capacitor	1	R7	0.91 ohm,1206	1
C11	1nF, 0805	1	R8	27K, 0805	1
C12,C13	470uF/16V	2	R9	16K, 0805	1
D1~D6	1N4007, rectifier diode	6	R10	360 ohm, 0805	1
D12	APD3100	1	R11	27 ohm, 0805	1
L1	470 uH, inductor	1	R12	1.2kohm, 0805	1
L2	Bead, 0805	1	T1	EE16 core, PC40	1

6. The test result of typical characteristics (9V/0.7A Demo Board)

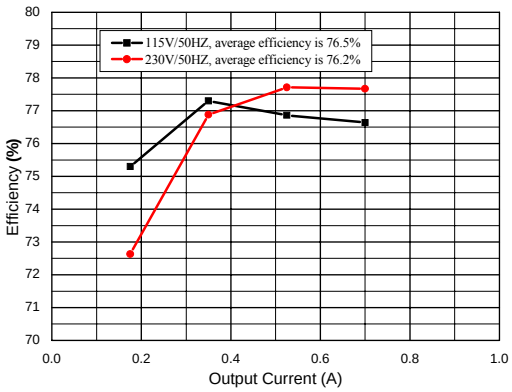


Figure 9, Conversion Efficiency of can meet energy star 2.0 norm of 73.8%.

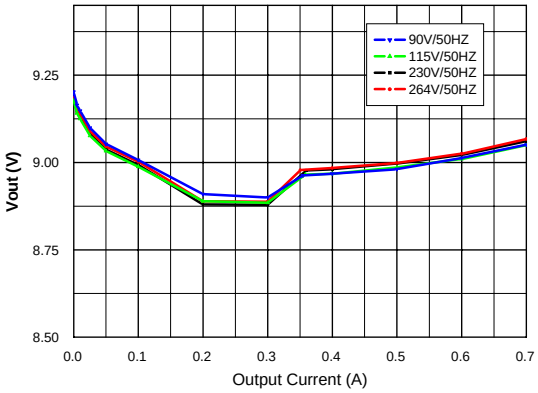


Figure 10, I-V curve, output voltage tolerance is 1.8%.

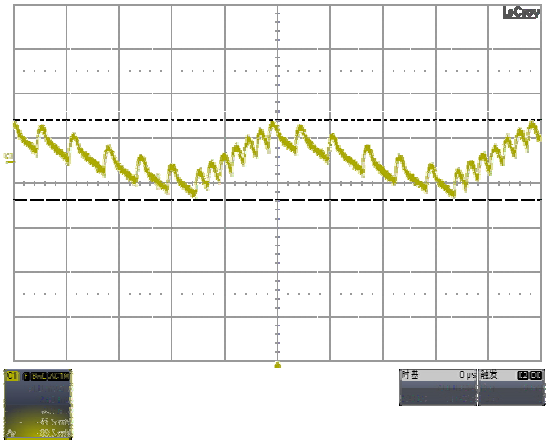


Figure 11, Output Ripple under 230Vac /whole operating range is within 100mV.

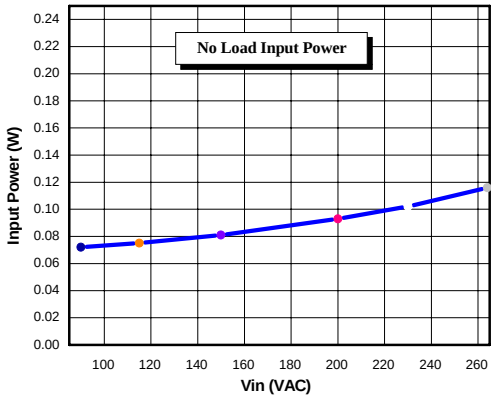
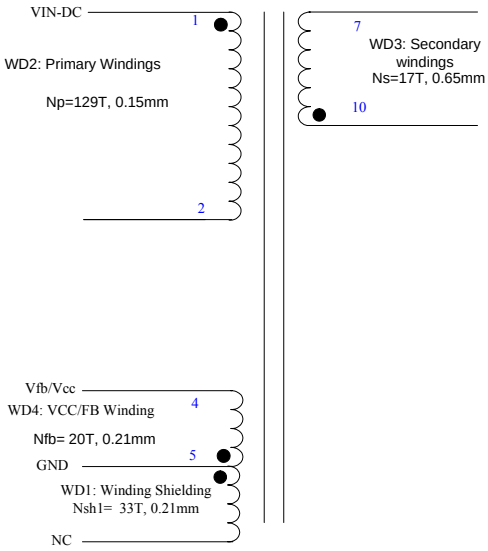


Figure 12, input power under no load is within 0.1Watt.

7. Transformer Spec



Primary Inductance	Pin 1-2,all other windings open, measured at 1kHz, 0.4VRMS	1.25mH, ±7%
Primary Leakage Inductance	Pin 1-2, all other windings shorted, measured at 10kHz, 0.4VRMS	180 uH (Max.)