STM8 Core & Architecture

STM8 Technical Training

Direct Memory Access (DMA)

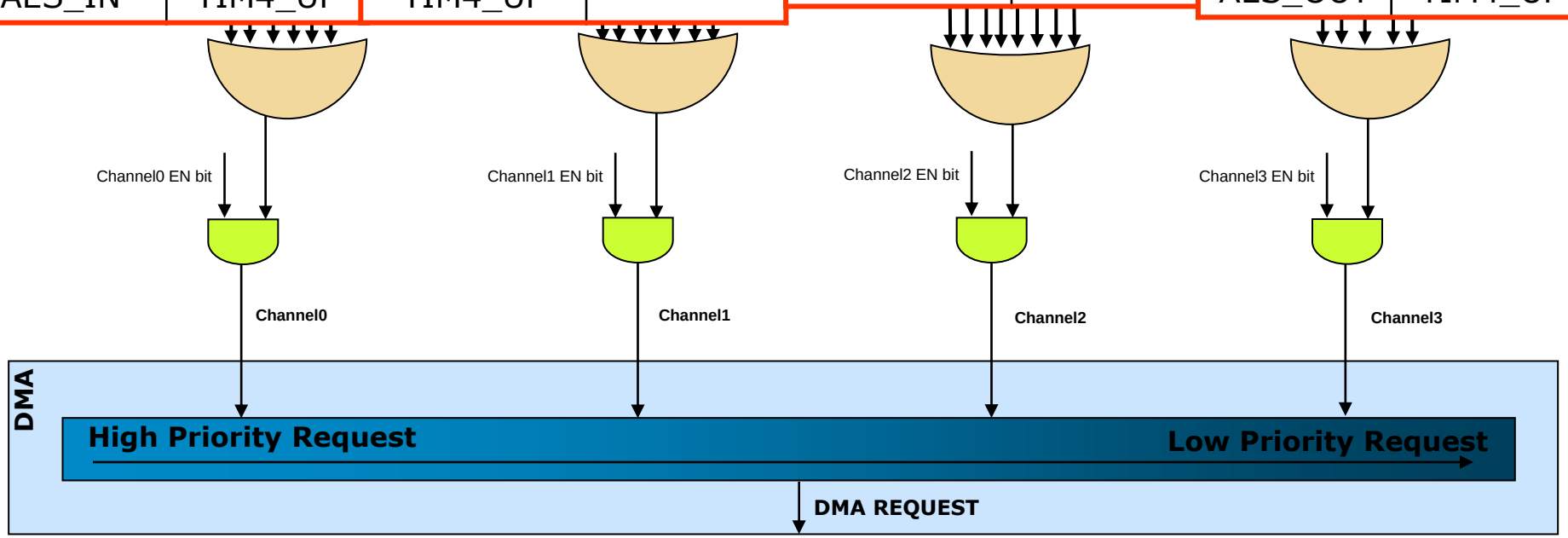
DMA Features

- **4 independently configurable channels** (channel 0..3)
- **4 Software programmable priority levels:** Very high, High, Medium or Low. Hardware priority in case of equality (channel0 has higher priority vs. channel1).
- **Circular mode (auto-reload mode)** is available to handle circular buffers and continuous data flows (e.g. ADC1 scan mode).
- **Programmable transfer data size**: Byte or Half word (16bit) with **Programmable number of data to be transferred** up to 255.
- **Can operate in low power Waite mode**
- **2 event flags for each channel with Interrupt capability**
  - DMA Half Transfer,
  - DMA Transfer complete
- **Programmable and Independent source and destination**:
  - **Memory-to-memory** (only on channel 3),
  - **peripheral-to-memory** and
  - **memory-to-peripheral** transfers

DMA Request Mapping (medium+ devices)

- The DMA controller provides access to 4 channels

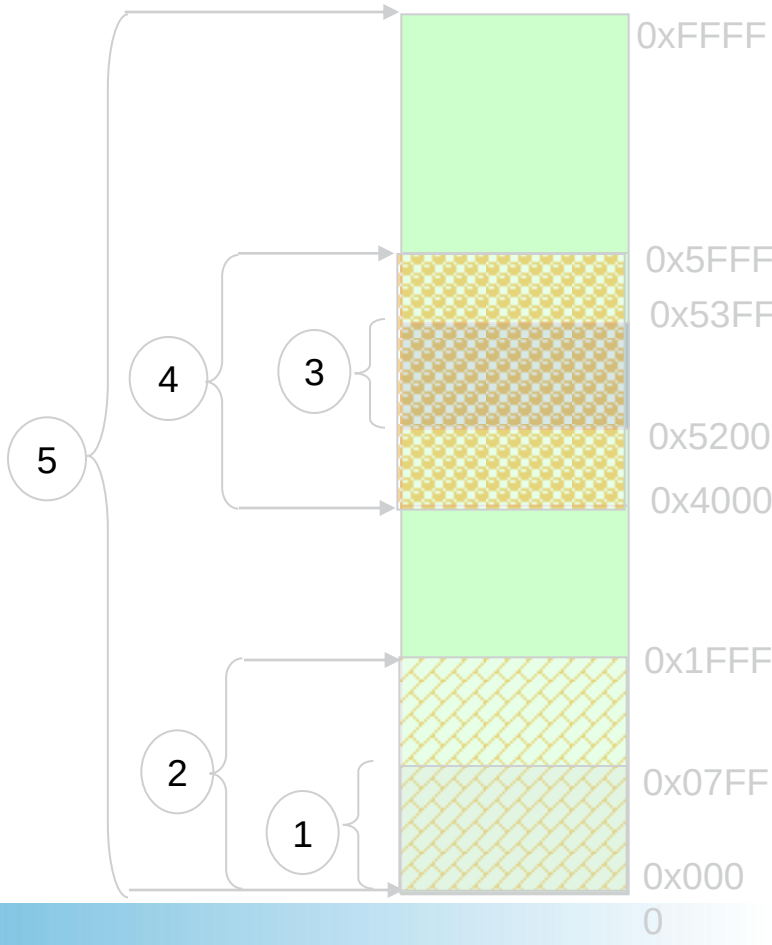
ADC	I2C_RX	ADC	SPI1_RX	ADC	SPI1_RX	ADC	I2C_TX
TIM2_CC1	TIM3_UP	USART1_TX	DAC_CH2	USART1_TX	TIM3_CC2	DAC_CH1	TIM2_CC2
TIM1_CC3	USART2_TX	TIM2_UP	TIM3_CC1	TIM1_UP, _CC1, _COM	USART3_ RX	TIM1_CC2	USART2_RX
SPI_2RX	TIM5_UP	TIM1_CC4	USART3_TX			SPI_2RX	TIM5_CC2
AES_IN	TIM4_UP	TIM4_UP		TIM5_CC1	TIM4_UP	AES_OUT	TIM4_UP



DMA Source and destination addresses

- **4 independently configurable channels** are available**:**
  - 3 regular channels (channel 0, channel 1 and channel 2)
  - 1 memory channel (channel 3).

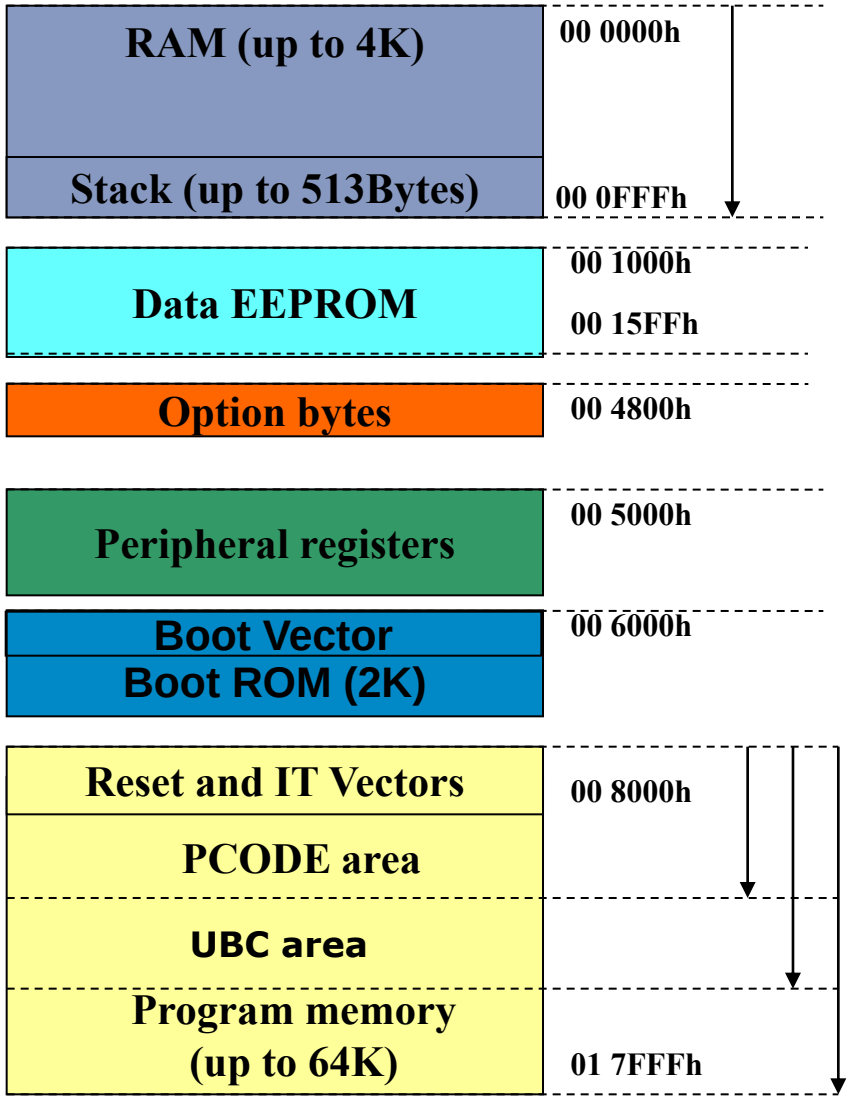
Channels	Transfer direction	Source address range	Destination address range
Regular channels	Peripheral to memory	Zone 3	Zone 1
	Memory to peripheral	Zone 1	Zone 3
Memory channel	Peripheral to memory	Zone 4	Zone 5
	Memory to peripheral	Zone 5	Zone 4
	Memory to Memory	Zone 5	Zone 2



Flash and Data EEPROM

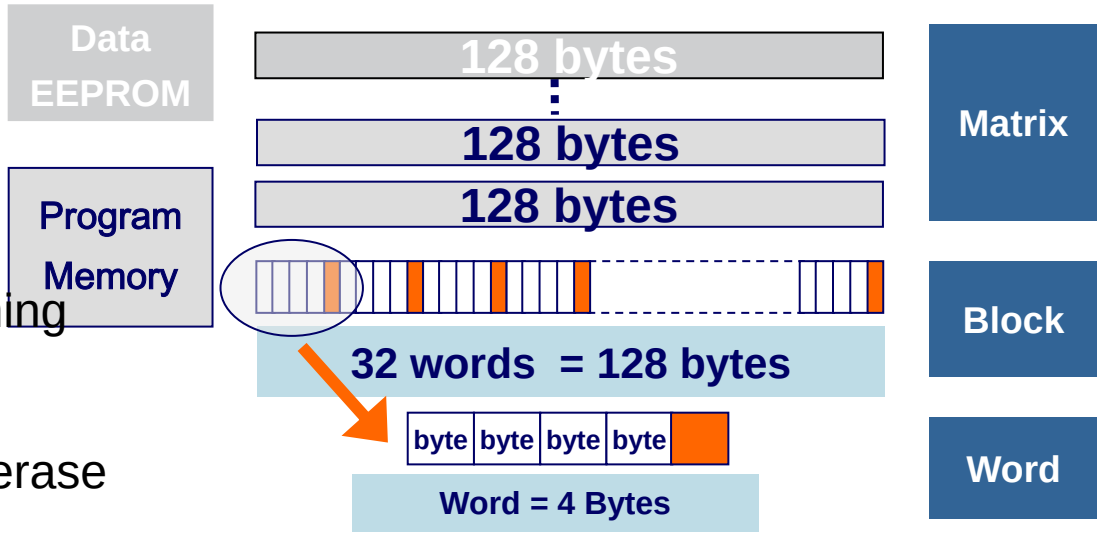
Memory mapping and main features L15x / L16x

- Up to 64kbyte Program memory (flash) based on EEPROM technology and up to 2k Data EEPROM memory
- Write protection with Memory Access Security System (MASS keys)
- Programmable write protected User Boot Code area (UBC)
- Automatic read-out protection of Proprietary code area (PCODE)
- Boot ROM embedding ST proprietary boot loader code
- One Interrupt vector dedicated to end of program/erase operation and on illegal program operation



Memory mapping and main features

- Read While Write capability (L15x / L16x)
- Read Out Protection (ROP)
- Byte, word or block programming capabilities
- 6ms programming time (3ms erase + 3ms write)



- In Circuit Programming (ICP) and In Application Programming (IAP) capabilities
- Memory state configurable to operating or power-down mode (IDDQ) in the device low power modes for STM8L15x / STM8L16x
- 128B per page − medium density devices
- 256B per page − medium+ / high density devices

Proprietary code protection

- Available on medium+ and high density devices
- Allowing to protect software libraries
- PCODE is accessible only by TRAP or TLI interrupts
- It is read protected for any other access
- Up to 255 pages
  - 256B each
- Interrupt vector table included in PCODE area

ROM bootloader

What is Bootloader in STM8L - requirements

- **Bootloader required properties:**

1) Able to program Flash, EEPROM, RAM memory in final user application
   - IAP programming feature in STM8
2) Communicate with host by built-in interfaces
   - UART1..3, SPI1, I2C1
   - Protected against self-rewrite (e.g. by accident)
   - location in ROM memory (address 0x6000)
3) Easy and safe to activate it
   - activated after each device reset
   - activation timeout – 1 second waiting for host command
   - can be disabled by option byte

Clock Control (CLK)

On Chip Oscillators

- Multiple clock sources for full flexibility in RUN/Low Power modes
  - HSE (High Speed External oscillator): 1MHz to 16MHz main osc
    → Can be bypassed with external clock
  - HSI (High Speed Internal RC): factory trimmed internal RC oscillator 16MHz calibrated in factory +/-2% max at ambient temperature
    - Feeds System clock after reset or exit from HALT/Active HALT mode for fast startup
    - Backup clock HSI/8 in case HSE failure
  - LSI (Low Speed Internal RC): 38 kHz internal RC for IWDG and optionally for the RTC/LCD and BEEP used for Auto Wake-Up (AWU) from Active HALT mode
  - LSE (Low Speed External oscillator): 32.768 kHz osc provides a precise time base with very low power consumption (max 06µA). Optionally drives the RTC/LCD for Auto Wake-Up (AWU) from Active HALT mode.
    → Can be bypassed with external clock

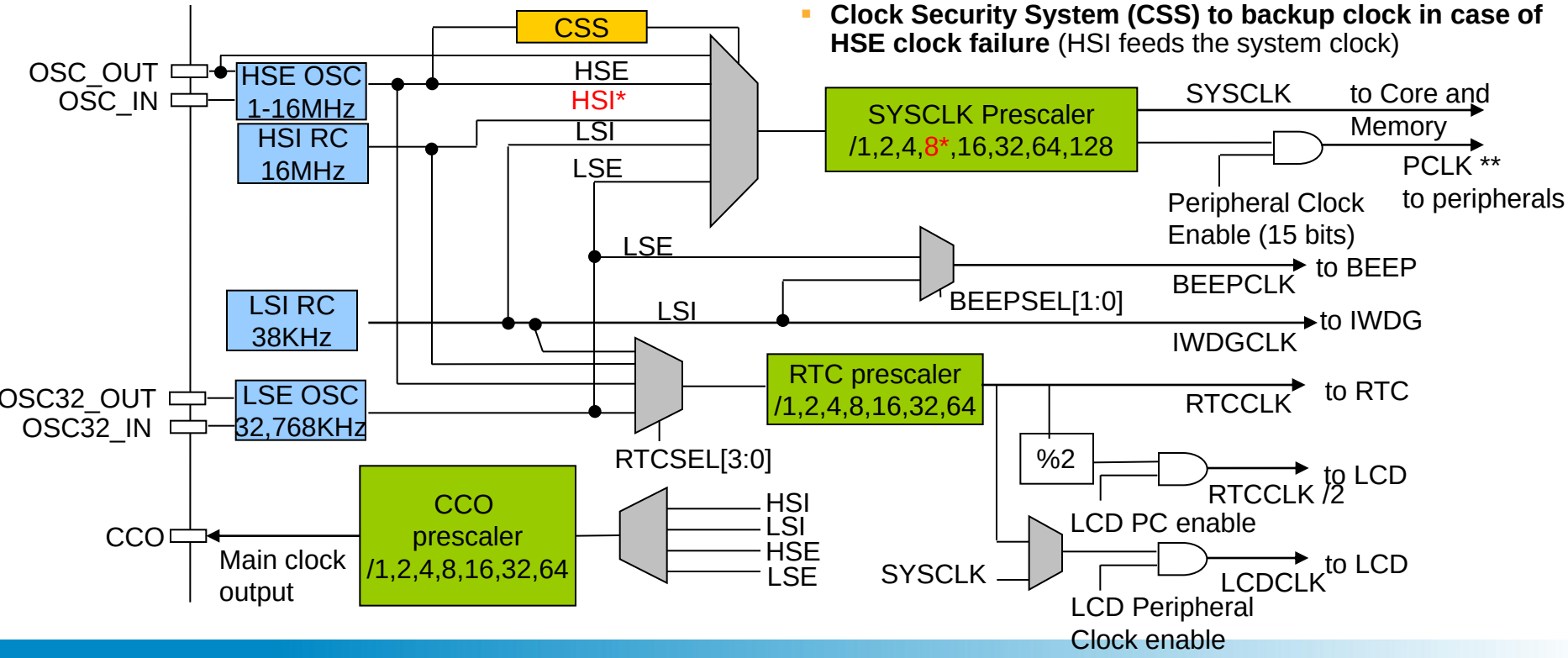
➔ ***Each clock source is enabled by Hardware when its selected to be used as source for: System clock, RTC clock, CCO output, IWDG (LSI) or BEEP (LSI/LSE) and can't be disabled while its being used.***

Clock Scheme & Features L15x

- **System clock sources**
  - HSI
  - HSE
  - LSI
  - LSE

HSI/8 default after reset*

- **Configurable dividers to provide CPU and peripherals clocks**
- **Peripheral clock gating (PCG)****
  - Enable or disable the clock for each peripherals to reduce power consumption
- **RTC/LCD Clock sources**
  - HSI
  - HSE with CSS
  - LSI
  - LSE with CSS
- **Fast and efficient System clock switching**
  - Clock sources can be changed safely on the fly in run mode through a configuration register
- **Configurable clock output on CCO Pin (PC4)**
- **Clock Security System (CSS) to backup clock in case of HSE clock failure** (HSI feeds the system clock)



(**) PCLK, clock gating for peripherals

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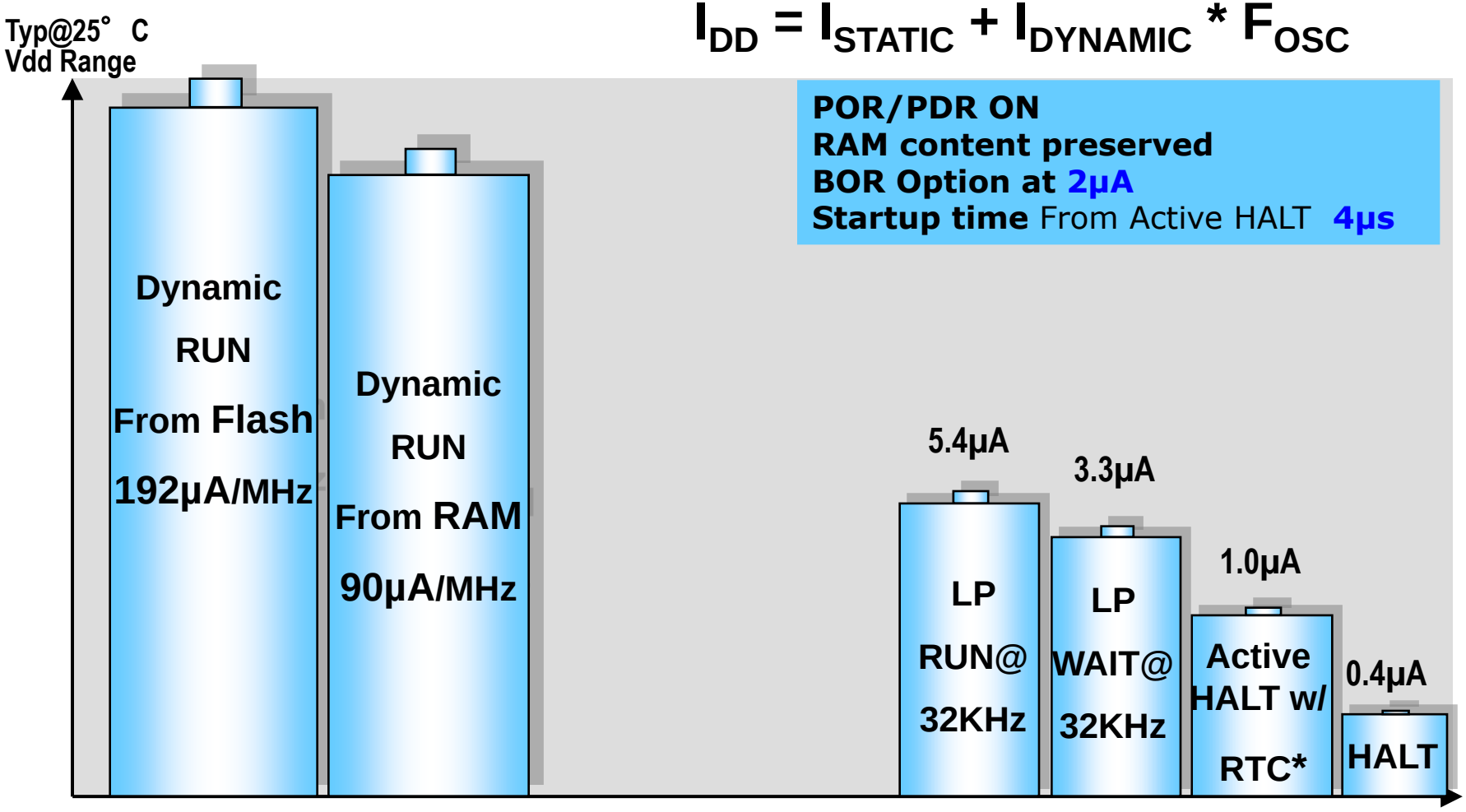
RTC and LCD clock L15x

- The RTC has two clock sources
  - **RTCCLK** used for RTC timer/counter.
    - When the HSE or HSI clock is selected as RTCCLK source, this clock must be divided to have a maximum of 1 MHz as input for the RTCCLK.
  - **SYSCLK** used for RTC register read/write access. This clock is gated by bit2 in the Peripheral clock gating register 2 (CLK_PCKENR2)
  - HSE and LSE source for RTC is covered by CSS (on medium+ devices)

- The LCD has two clock sources
  - **RTCCLK** divided by 2 used to generate the LCD frame rate. This clock is gated by bit3 in the Peripheral clock gating register 2 (CLK_PCKENR2).
    - Consequently, even if the RTC is not used in the application the RTCCLK must be configured to drive the LCD.
  - **LCDCLK** used for LCD register read/write access. This clock is derived from SYSCLK by setting the bit3 in the Peripheral clock gating register 2 (CLK_PCKENR2).
    - In Active Halt mode the LCDCLK source is RTCCLK instead of SYSCLK.

Power and Reset

Low Power consumption values



- **LP Wait mode:** LSI/LSE ON, peripherals can be activated
- **ACTIVE HALT mode:** All clocks OFF, RTC ON
- **HALT mode:** All clocks OFF, RTC OFF

- ***Also possible: RTC on LSI:** RTC feed by low speed internal RC, periodic wake up but no accurate calendar function*

Low Power modes: summary

Low Power Modes	Entry	Functions							Low power modes names and consumptions	
		CPU	Periphs	High Speed Osc	RTC Calendar	LSI LSE	FLASH	RAM	STM8L Typical values @ 3V / 25° C	STM8L Typical values @ 3V / 85° C
LP RUN	**SW Sequence**	ON	Can be enabled	OFF	ON	ON	OFF	ON	**5.4µA**	
LP WAIT	**SW Sequence + WFE**	OFF	Can be enabled	OFF	ON	ON	OFF	ON	**3.3µA**	
ACTIVE Halt w/ full RTC	**HALT**	OFF			ON	ON	OFF	ON	**1.0µA***	**1.4µA**
ACTIVE Halt w/ RTC on LSI					OFF	ON	OFF	ON	**0.8µA***	**1.2µA**
Halt					OFF	OFF	OFF	ON	**0.4µA***	**1µA**

*** Internal reference voltage + BOR OFF**