

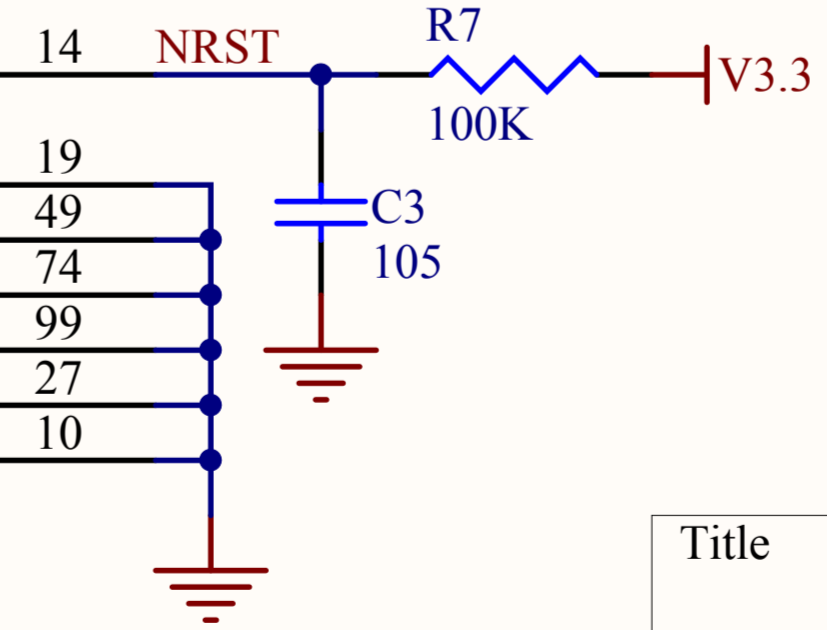
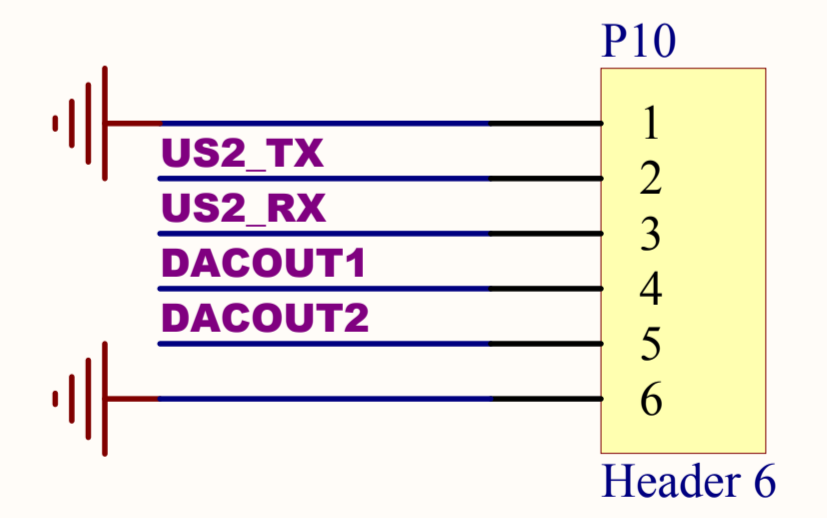
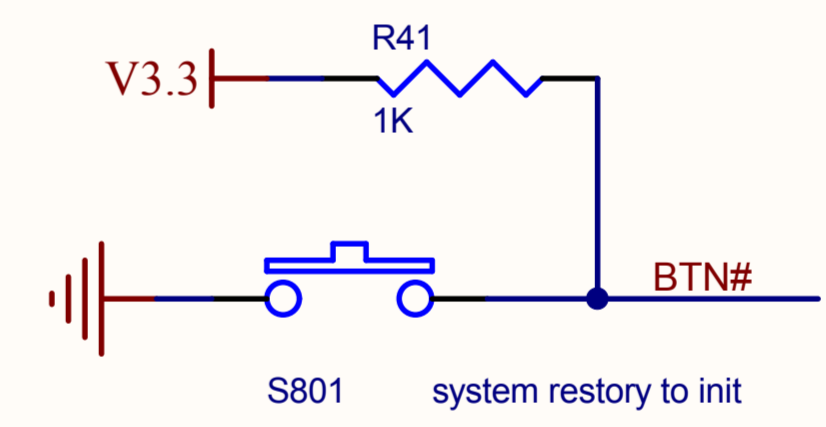
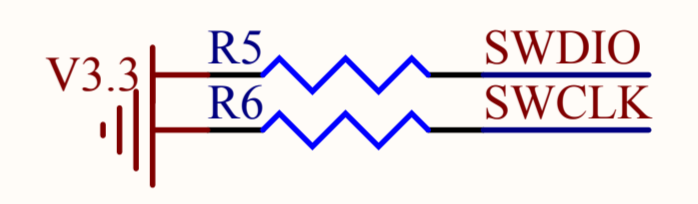
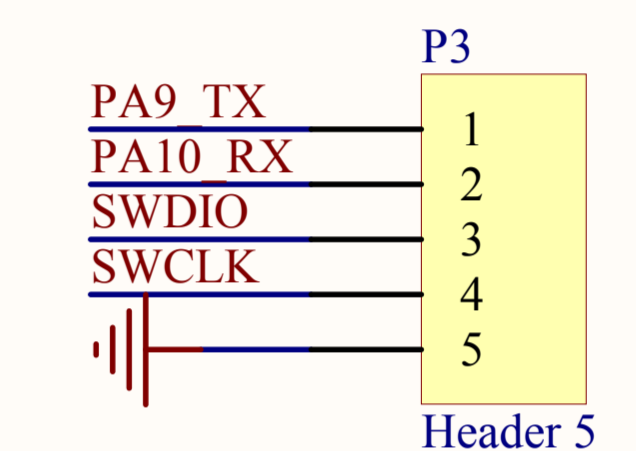
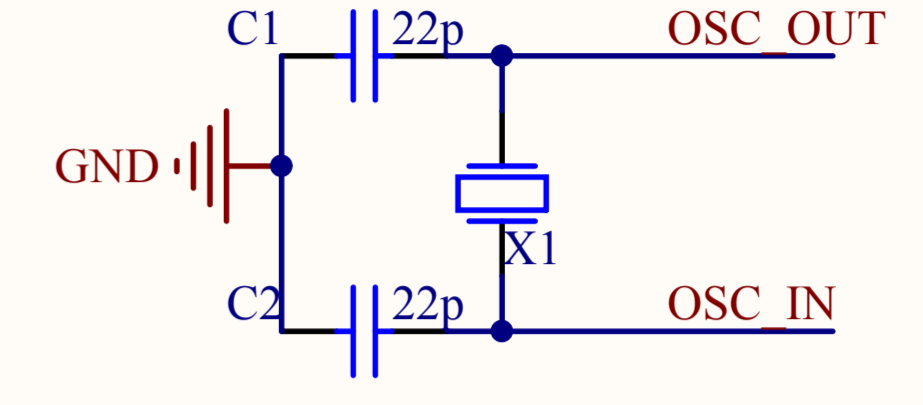
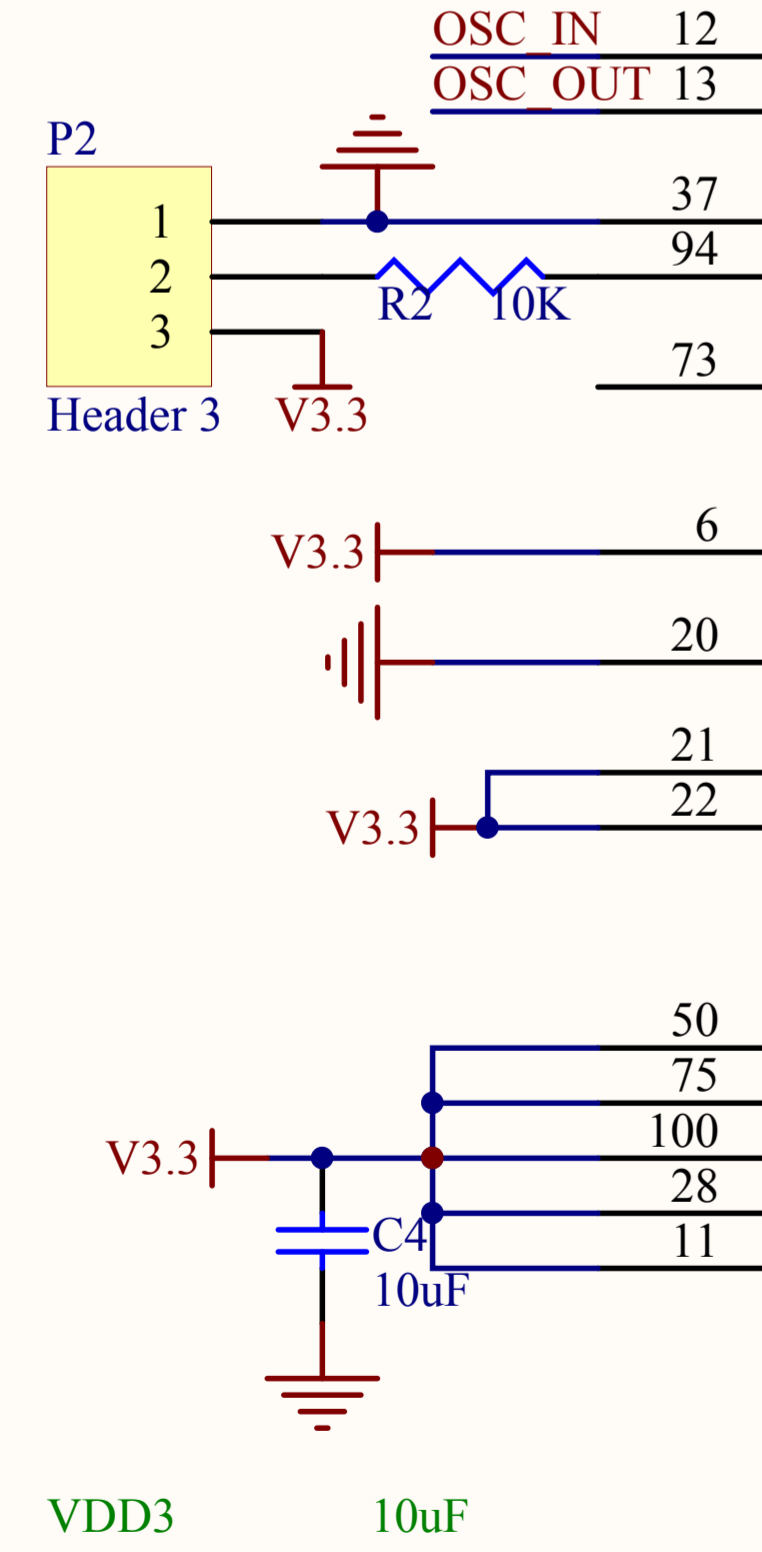
Title		
Size	Number	Revision
A4		
Date:	2012/6/26	Sheet of
File:	E:\ \.DAC.SchDoc	Drawn By:

U1

**BTN#** 23 PA0/WKUP/US2\_CTS/ADC123\_IN0/T2\_CH1\_ETR/T5\_CH1/T8\_ETR  
**USB\_M** 24 PA1/US2\_RTS/ADC123\_IN1/T5\_CH2/T2\_CH2  
**US2\_TX** 25 PA2/US2\_TX/ADC123\_IN2/T5\_CH3/T2\_CH3  
**US2\_RX** 26 PA3/US2\_RX/ADC123\_IN3/T5\_CH4/T2\_CH4  
**DACOUT1** 29 PA4/SPI1\_NSS/USART2\_CK/DAC\_OUT1/ADC12\_IN4  
**DACOUT2** 30 PA5/SPI1\_SCK/DAC\_OUT2/ADC12\_IN5  
 31 PA6/SPI1\_MISO/TIM8\_BKIN/ADC12\_IN6/TIM3\_CH1/TIM1\_BKIN  
 32 PA7/SPI1\_MOSI/TIM8\_CH1N/ADC12\_IN7/TIM3\_CH2/TIM1\_CH1N  
  
 67 PA8/USART1\_CK/TIM1\_CH1/MCO  
**PA9\_TX** 68 PA9/USATR1\_TX/TIM1\_CH2  
**PA10\_RX** 69 PA10/USART1\_RX/TIM1\_CH3  
**USBDM** 70 PA11/USART1\_CTS/USBDM/CAN\_RX/TIM1\_CH4  
**USBDP** 71 PA12/USART1\_RTS/USBDP/CAN\_TX/TIM1\_ETR  
**SWDIO** 72 PA13/JTMS-SWDIO  
**SWCLK** 76 PA14/JTCK/SWCLK  
 77 PA15/JTDI/I2S3\_WS/TIM2\_CH1\_ETR/PA15/SPI1\_NSS  
  
 35 PB0/ADC12\_IN8/TIM3\_CH3/TIM8\_CH2N/TIM1\_CH2N  
 36 PB1/ADC12\_IN9/TIM3\_CH4/TIM8\_CH3N/TIM1\_CH3N  
  
 89 PB3/JTDO/SPI3\_SCK/I2S3\_CK/TRACESWO/TIM2\_CH2/SPI1\_SCK  
 90 PB4/NJTRST/SPI3\_MISO/TIM3\_CH1/SPI1\_MISO  
 91 PB5/I2C1\_SMBA/SPI3\_MOSI/I2S3\_SD/TIM3\_CH2/SPI1\_MOSI  
**FPGA\_CTR** 92 PB6/I2C1\_SCL/TIM4\_CH1  
**FPGA\_NADV** 93 PB7/I2C1\_SDA/FSMC\_NADV/TIM4\_CH2/USART1\_RX  
  
**LED\_CTRL** 95 PB8/TIM4\_CH3/SDIO\_D4/I2C1\_SCL/CAN\_RX  
**LED\_CTRL** 96 PB9/TIM4\_CH4/SDIO\_D5/I2C1\_SDA/CAN\_TX  
**UART3\_TX** 97 PB10/I2C2\_SCL/USART3\_TX/TIM2\_CH3  
**UART3\_RX** 98 PB11/I2C2\_SDA/USART3\_RX/TIM2\_CH4  
 51 PB12/SPI2\_NSS/I2S2\_WS/I2C2\_SMBA/USART3\_CK/TIM1\_BKIN  
 52 PB13/SPI2\_SCK/I2S2\_CK/USART3\_CTS/TIM1\_CH1N  
 53 PB14/SPI2\_MISO/TIM1\_CH2N/USART3\_RTS  
**FPGA\_RST** 54 PB15/SPI2\_MOSI/I2S2\_SD/TIM1\_CH3N

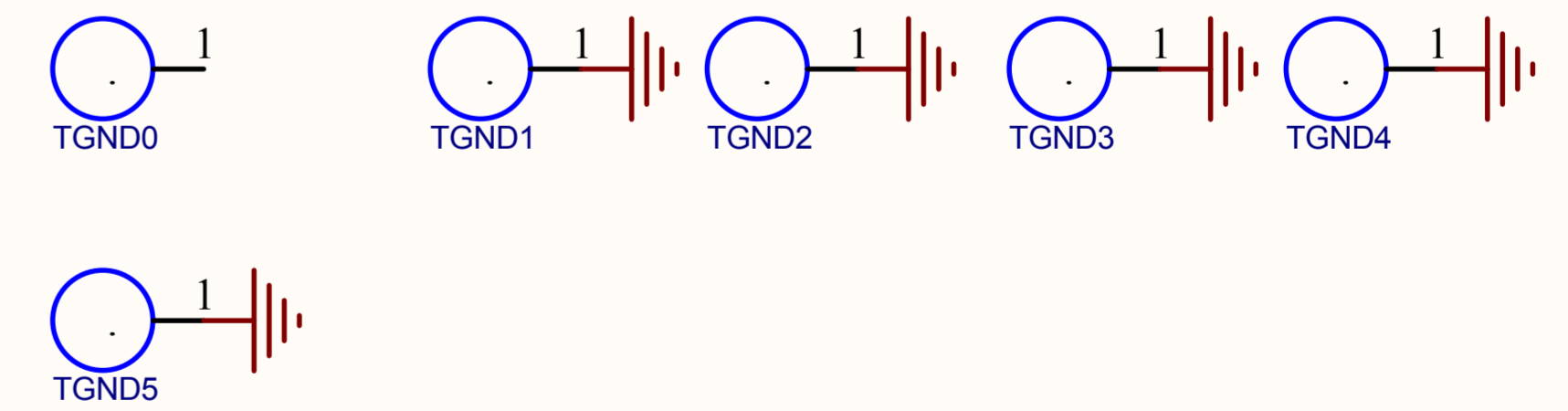
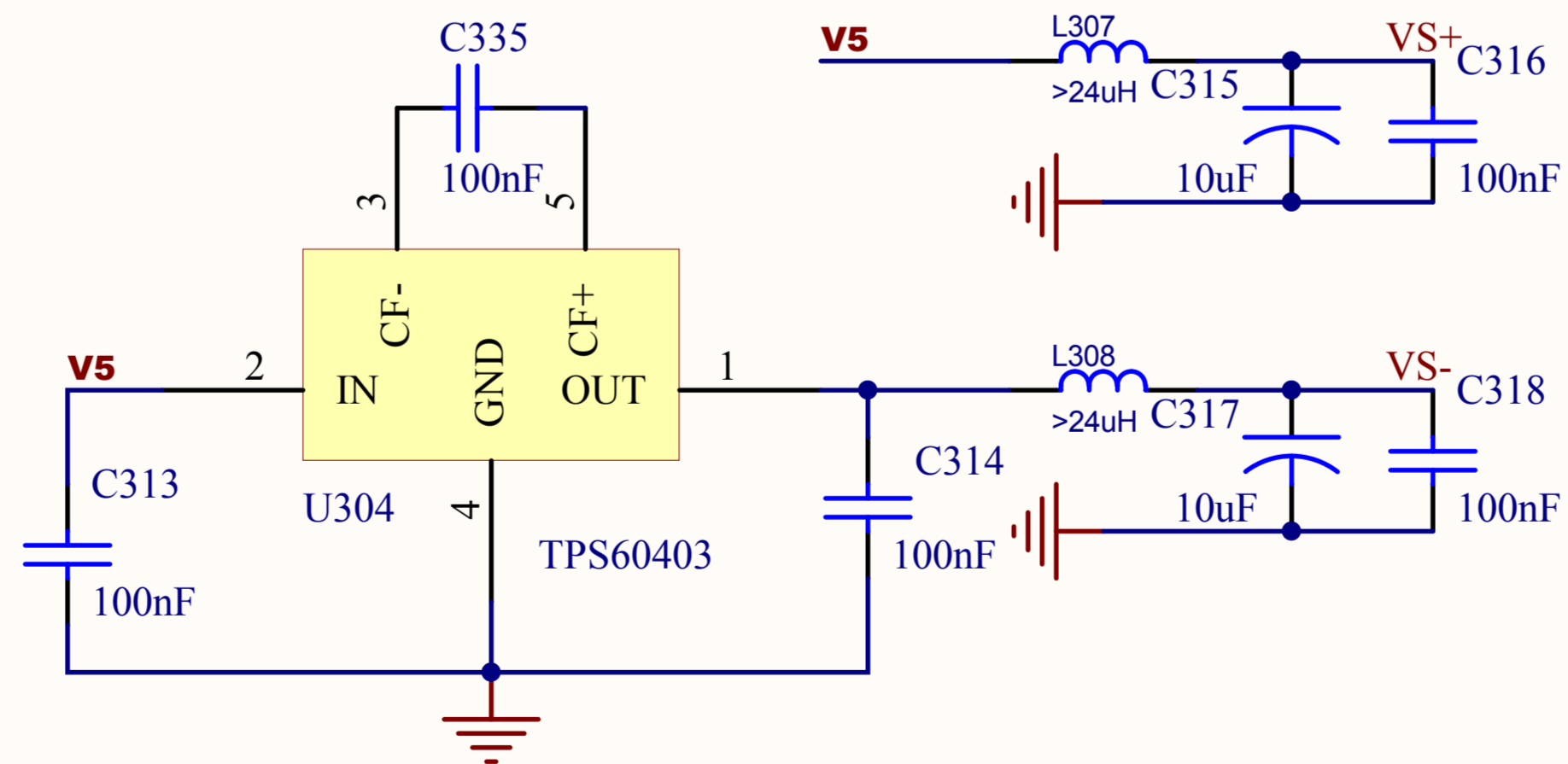
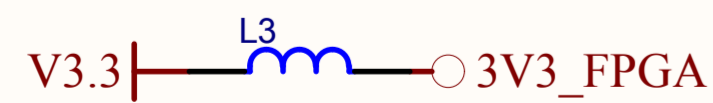
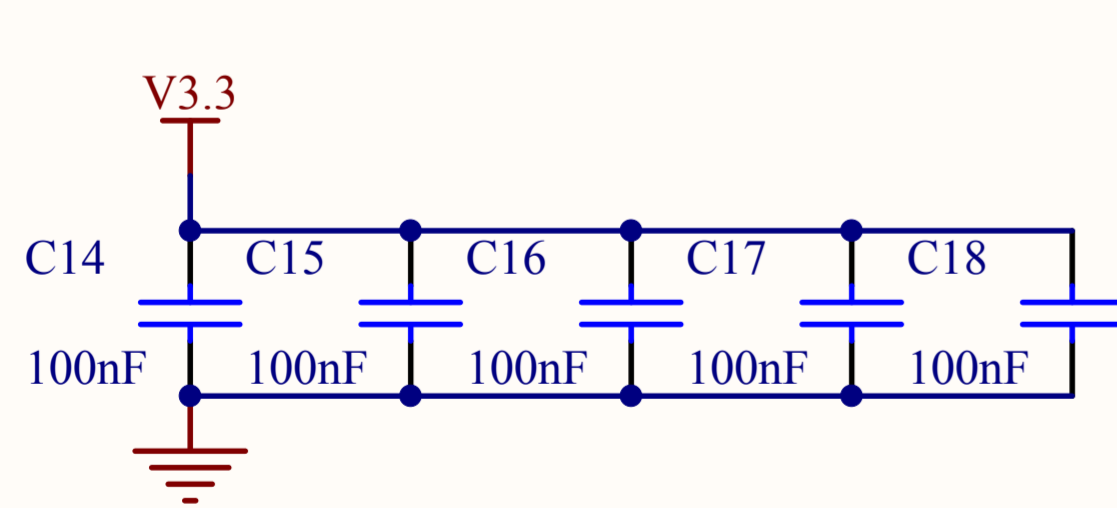
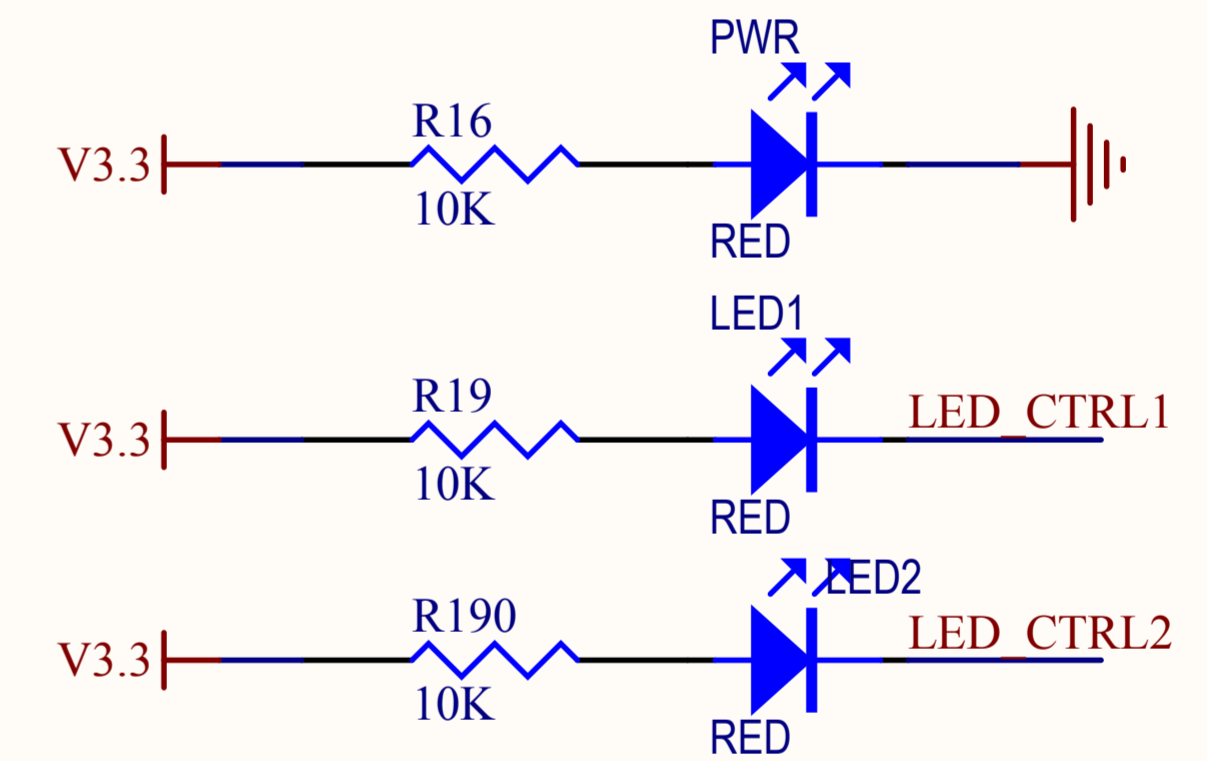
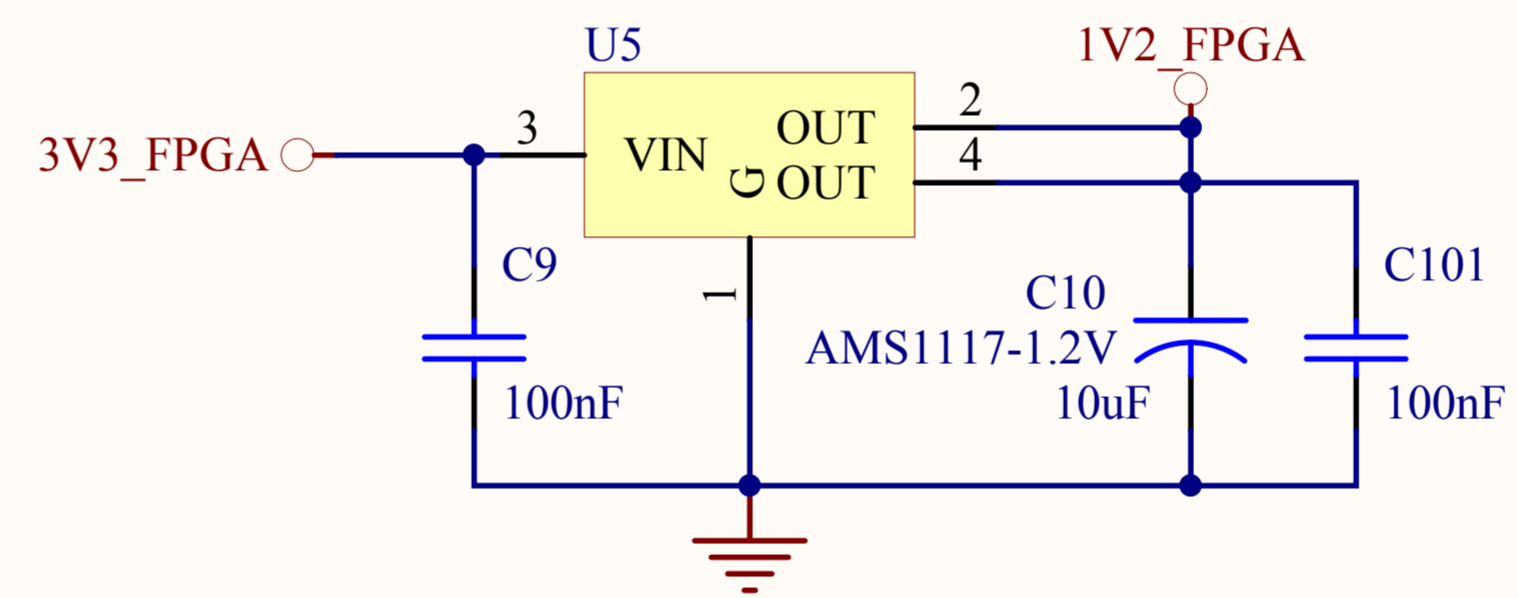
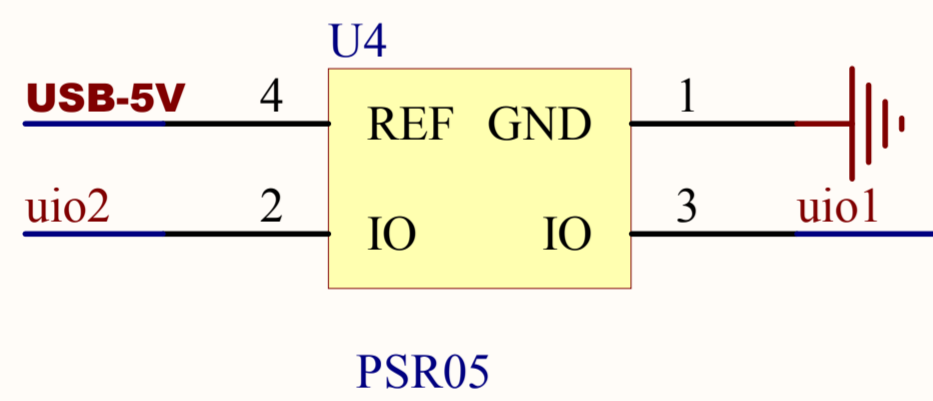
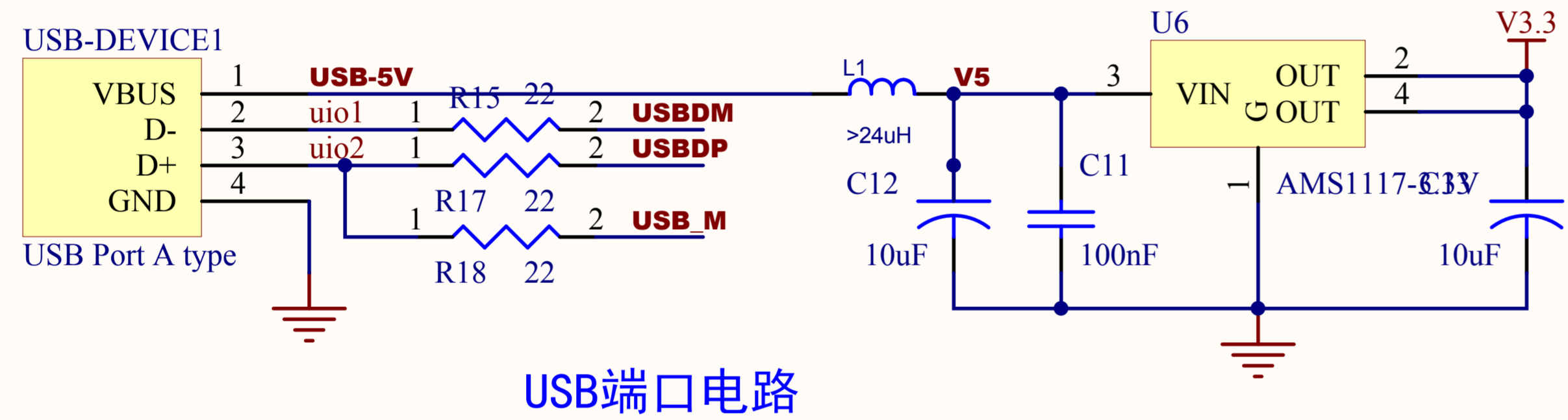
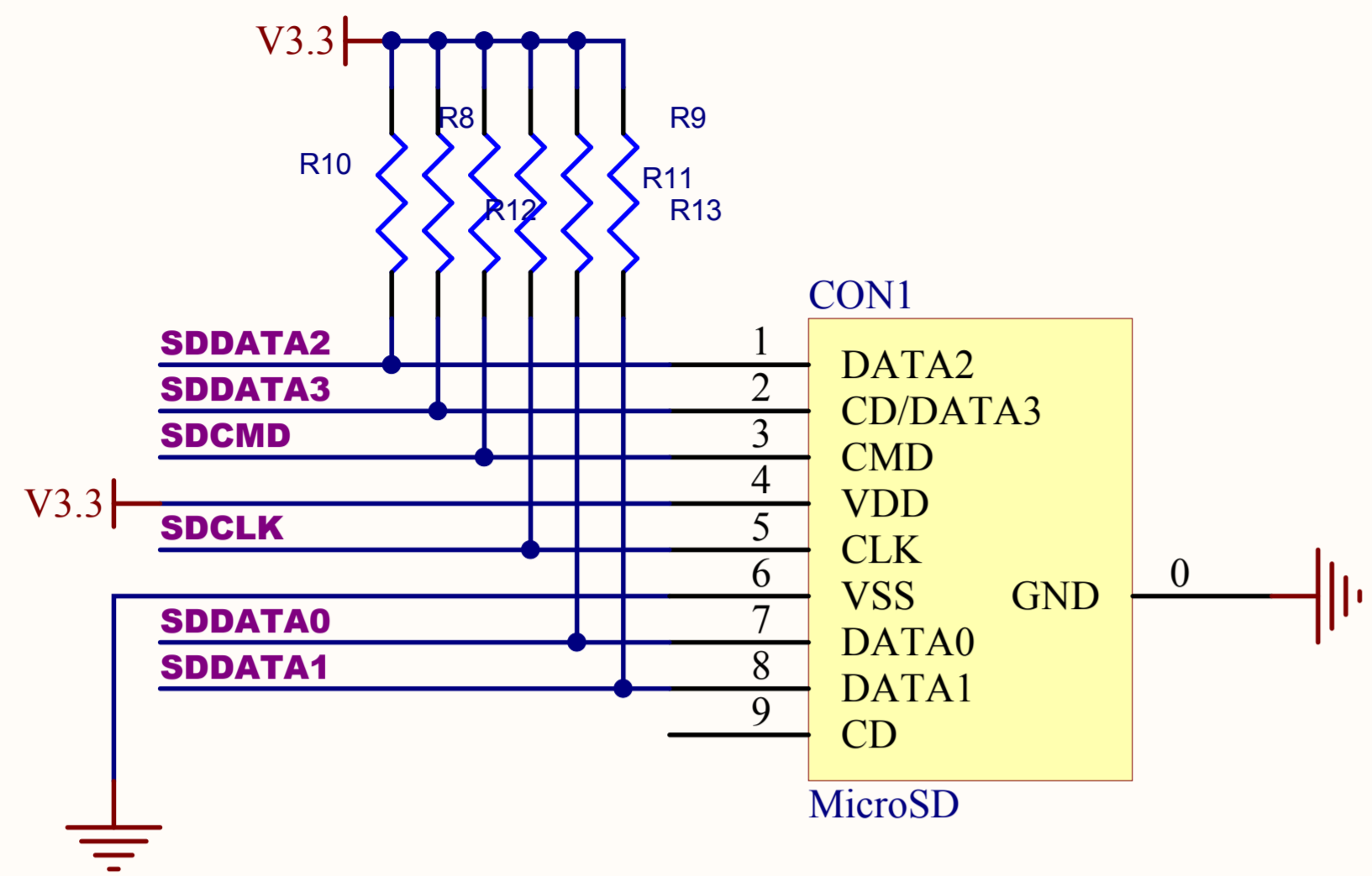
PC15-OSC32\_OUT 9  
 PC14-OSC32\_IN 8  
 PC13-TAMPER-RTC 7  
**SDCLK** 80  
**SDDATA3** 79  
**SDDATA2** 78  
**SDDATA1** 66  
**SDDATA0** 65  
 64  
 63  
 34  
 33  
 18  
 17  
 16  
 15  
  
 62 FSMC D1  
 61 FSMC D0  
 60 FSMC A18  
 59 FSMC A17  
 58 PD11\_RS  
 57 FSMC D15  
 56 FSMC D14  
 55 FSMC D13  
 88 PD7\_CS  
 87  
 86 PD5\_WR  
 85 PD4\_RD  
 84 FSMC\_CLK  
 83 SDCMD  
 82 FSMC D3  
 81 FSMC D2  
  
 46 FSMC D12  
 45 FSMC D11  
 44 FSMC D10  
 43 FSMC D9  
 42 FSMC D8  
 41 FSMC D7  
 40 FSMC D6  
 39 FSMC D5  
 38 FSMC D4  
 5  
 4  
 3  
 2  
 1  
 98  
 97  
 PE15/FSMC\_D12/TIM1\_BKIN  
 PE14/FSMC\_D11/TIM1\_CH4  
 PE13/FSMC\_D10/TIM1\_CH3  
 PE12/FSMC\_D9/TIM1\_CH3N  
 PE11/FSMC\_D8/TIM1\_CH2  
 PE10/FSMC\_D7/TIM1\_CH2N  
 PE9/FSMC\_D6/TIM1\_CH1  
 PE8/FSMC\_D5/TIM1\_CH1N  
 PE7/FSMC\_D4/TIM1\_ETR  
 PE6/TRACED3/FSMC\_A22  
 PE5/TRACED2/FSMC\_A21  
 PE4/TRACED1/FSMC\_A20  
 PE3/TRACED0/FSMC\_A19  
 PE2/TRACECK/FSMC\_A23  
 PE1/FSMC\_NBL1  
 PE0/TIM4\_ETR/FSMC\_NBL0

9  
 8  
 7  
**SDCLK** 80  
**SDDATA3** 79  
**SDDATA2** 78  
**SDDATA1** 66  
**SDDATA0** 65  
 64  
 63  
 34  
 33  
 18  
 17  
 16  
 15  
  
 62 FSMC D1  
 61 FSMC D0  
 60 FSMC A18  
 59 FSMC A17  
 58 PD11\_RS  
 57 FSMC D15  
 56 FSMC D14  
 55 FSMC D13  
 88 PD7\_CS  
 87  
 86 PD5\_WR  
 85 PD4\_RD  
 84 FSMC\_CLK  
 83 SDCMD  
 82 FSMC D3  
 81 FSMC D2  
  
 46 FSMC D12  
 45 FSMC D11  
 44 FSMC D10  
 43 FSMC D9  
 42 FSMC D8  
 41 FSMC D7  
 40 FSMC D6  
 39 FSMC D5  
 38 FSMC D4  
 5  
 4  
 3  
 2  
 1  
 98  
 97



STM32VET6

Title		
STM32F103VET6 CPU Interface		
Size	Number	Revision
A4		
Date:	2012/6/26	Sheet of
File:	E:\...\DsoCpu.SchDoc	Drawn By:



Title		
Power Manange		
Size	Number	Revision
A4		
Date:	2012/6/26	Sheet of
File:	E:\...\DsoPower.SchDoc	Drawn By:

1

2

3

4

A

A

B

B

C

C

D

D

DsoPower.SchDoc



DsoCpu.SchDoc



Spartan3.SchDoc



DAC.SchDoc



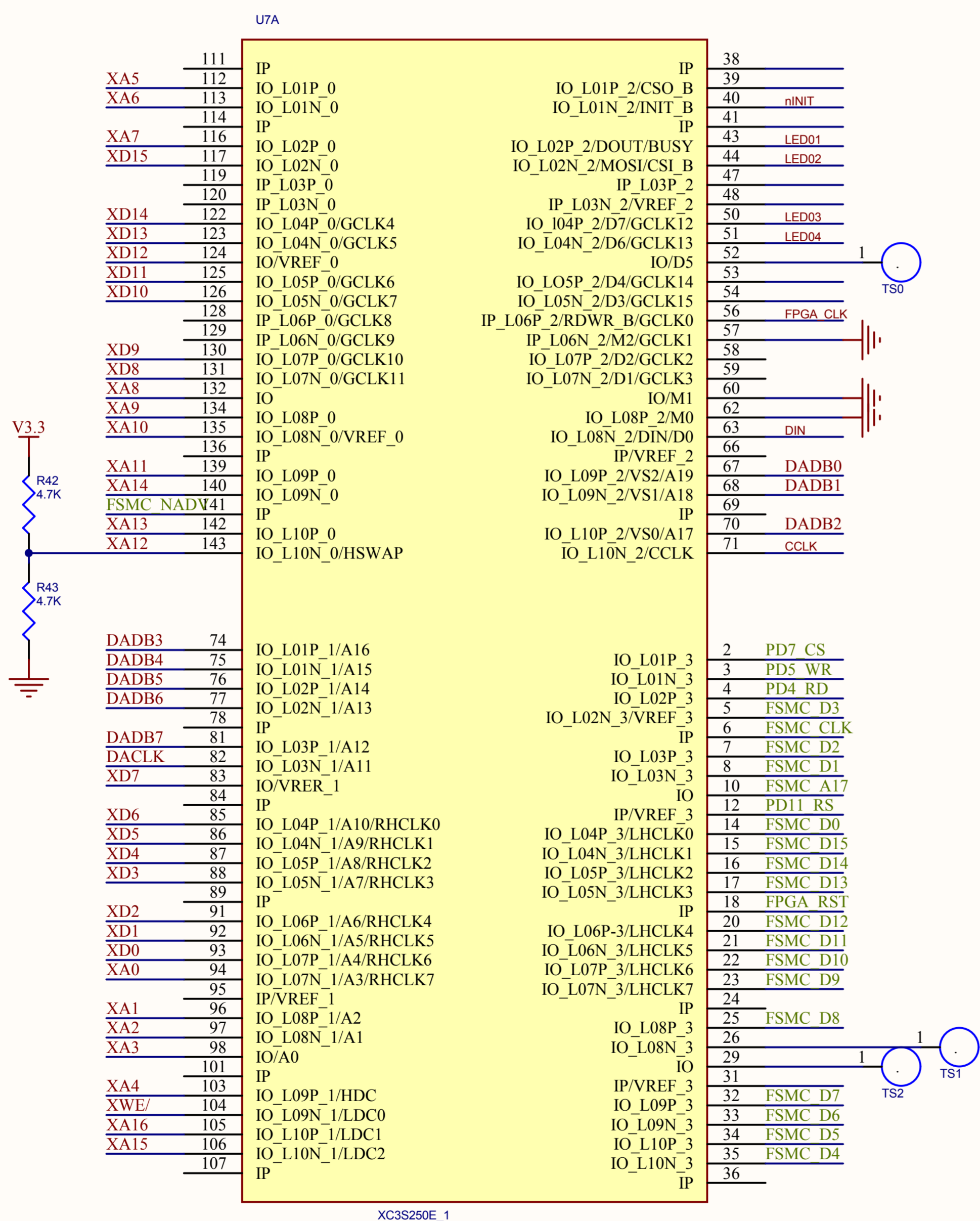
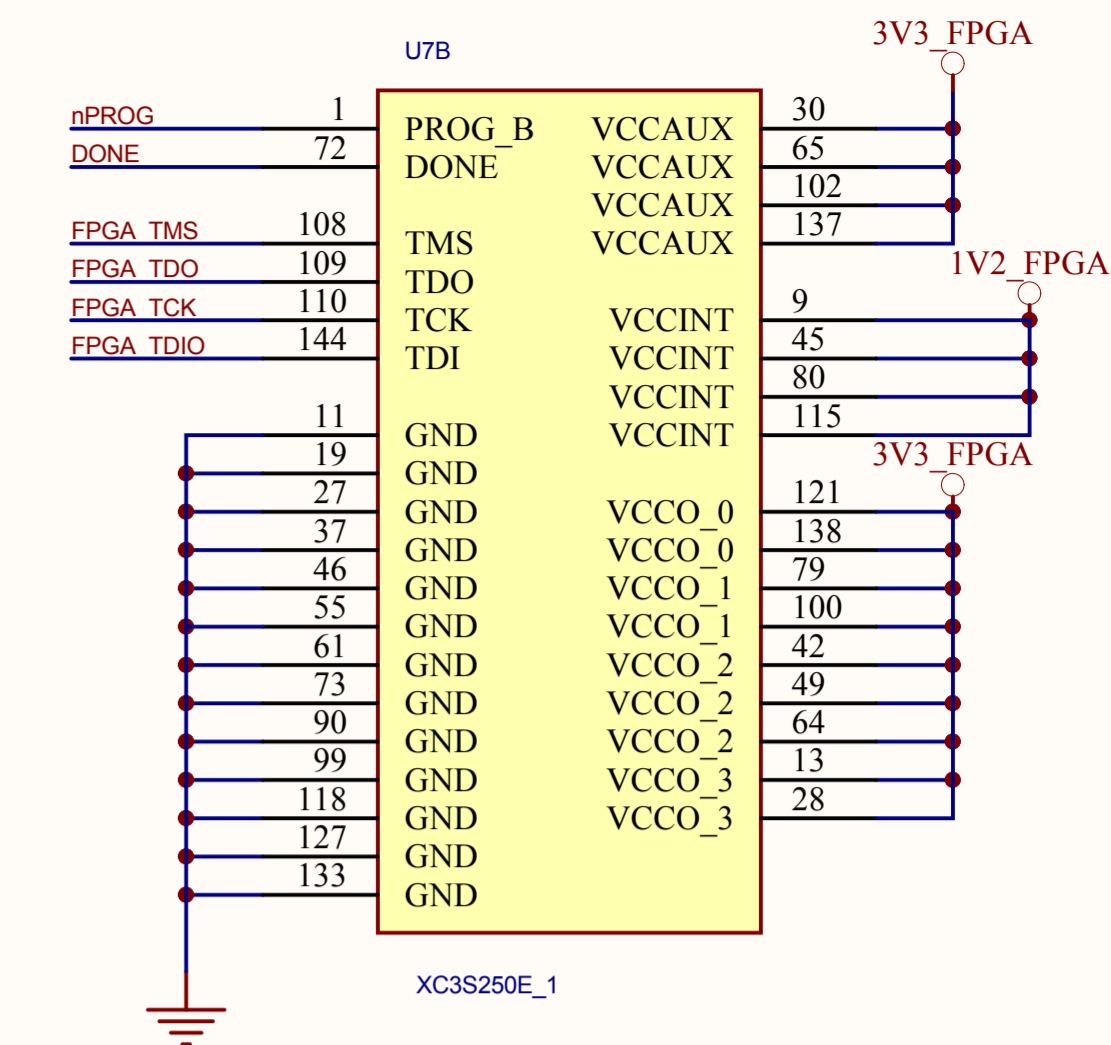
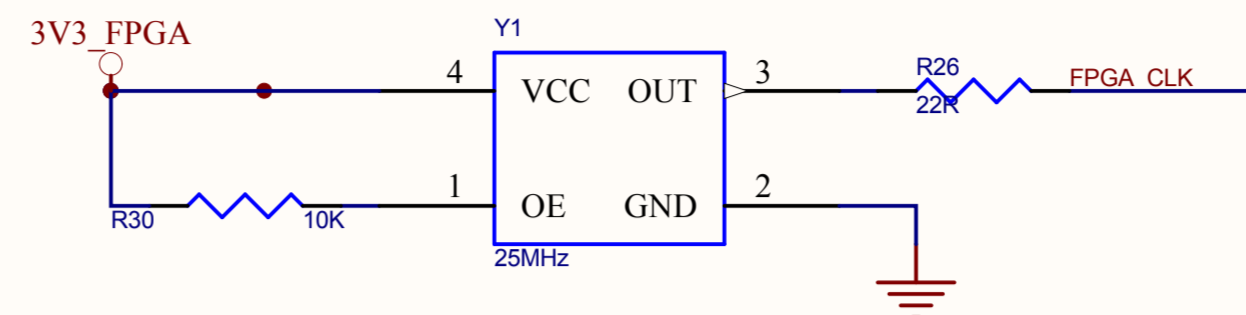
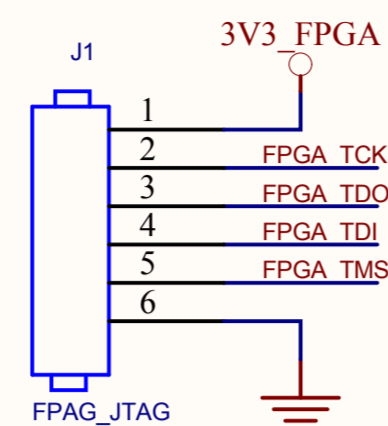
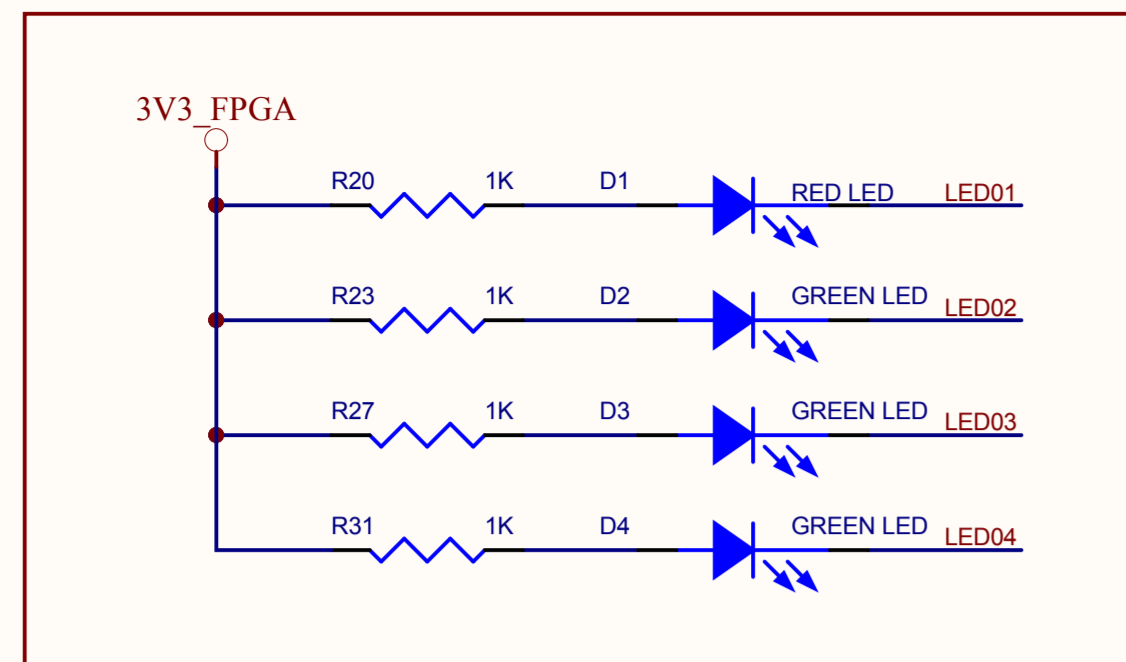
Title			
Size	Number		Revision
A4			
Date:	2012/6/26		Sheet of
File:	E:\ \.\MyDSOAll.SchDoc		Drawn By:

1

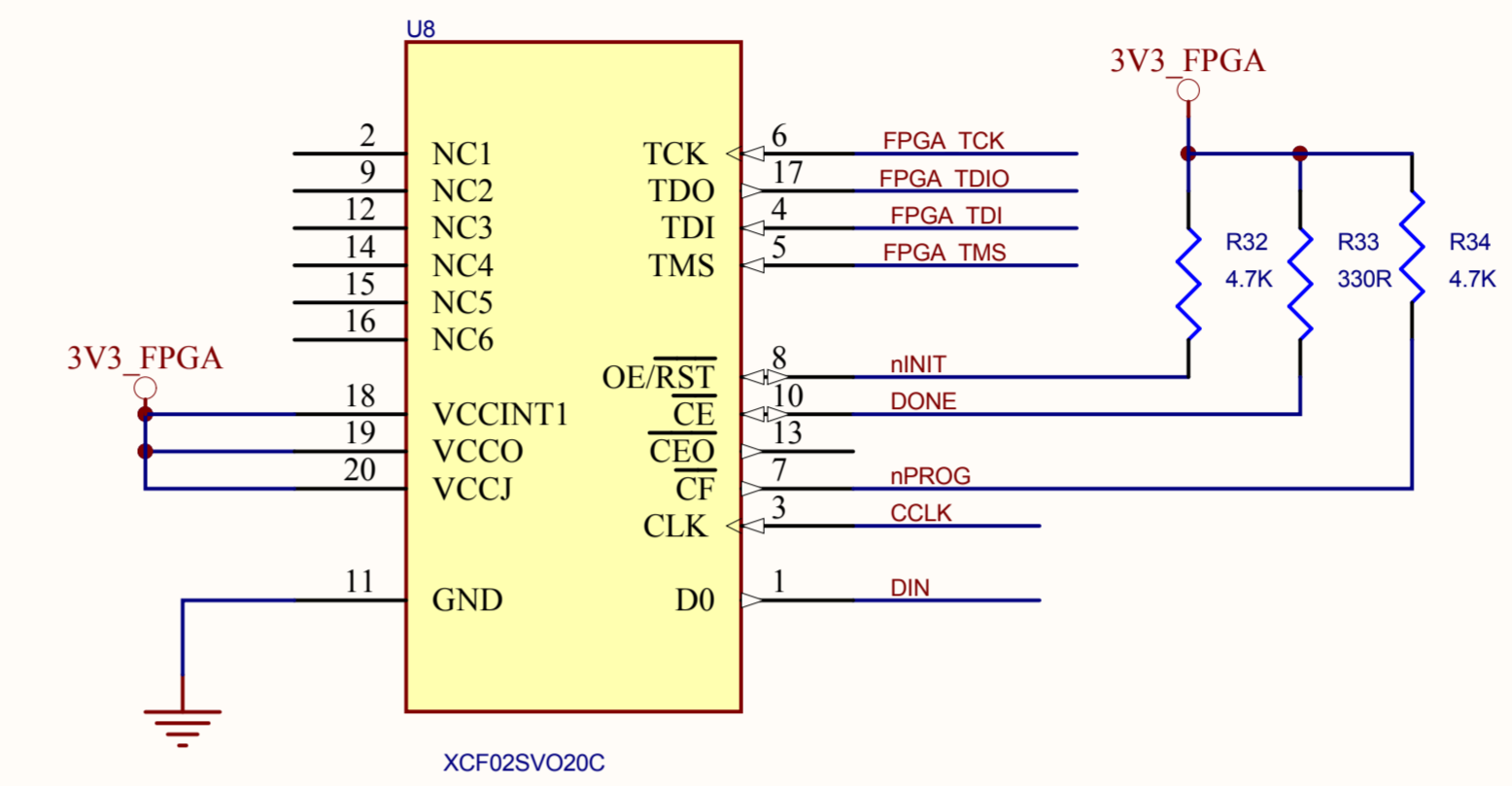
2

3

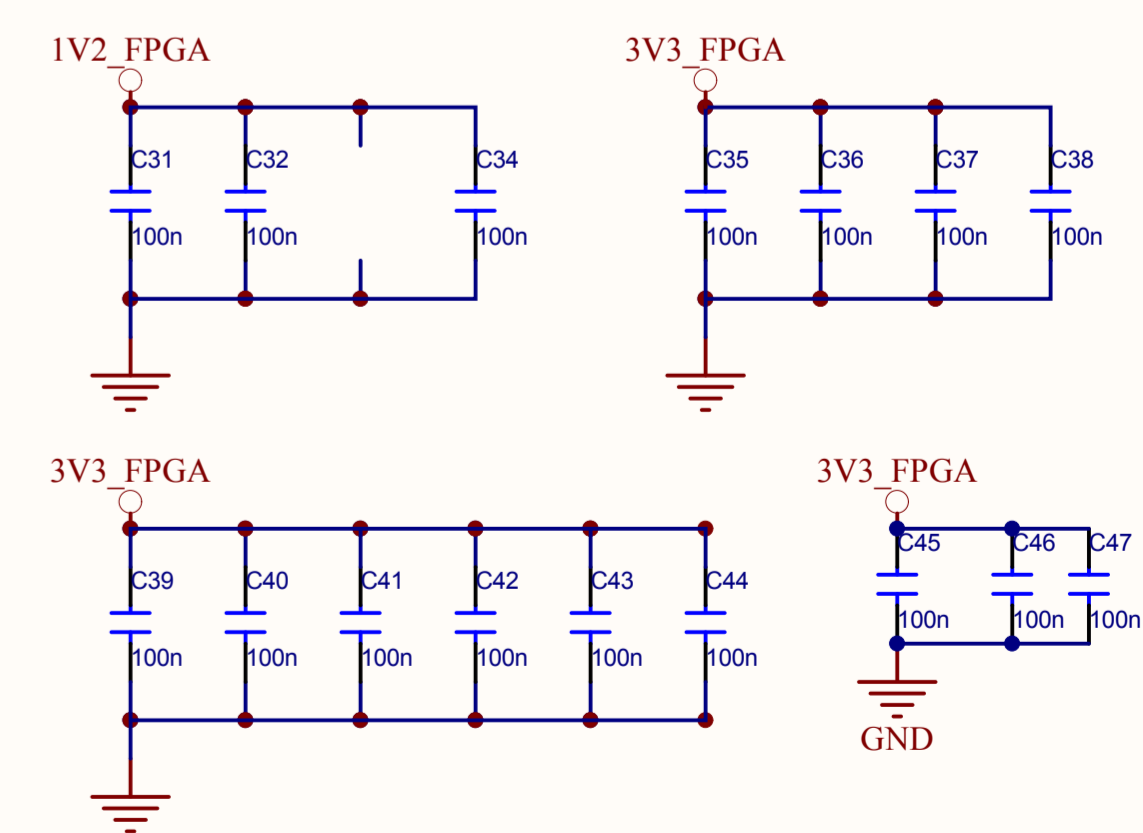
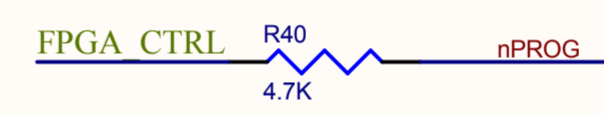
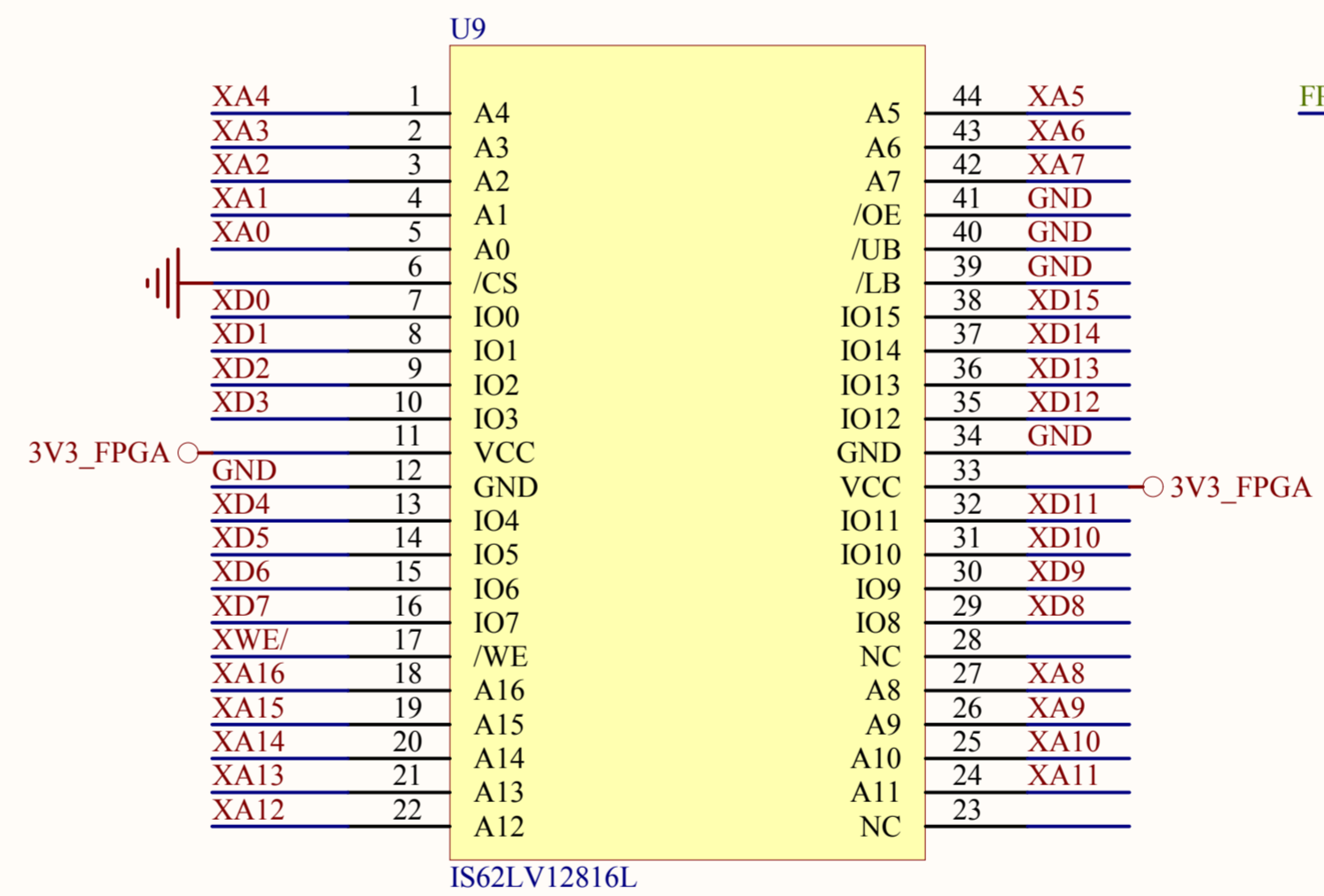
4



凡是以IP开头的均只能做输入



Master Serial Mode



Title		
Size	Number	Revision
A4		
Date:	2012/6/26	Sheet of
File:	E:\...\Spartan3.SchDoc	Drawn By:

